A New DAC Mismatch Shaping Technique for Sigma–Delta Modulators

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***Abstract*—A new ΣΔ modulator architecture that shapes digital-to-analog converter (DAC) mismatches in a manner similar to quantization noise shaping is proposed, allowing operation with low oversampling ratios, high-resolution quantizers, and compact logic. It is shown that the proposed architecture entails a smaller feedback logic delay than data-weighted-averaging techniques, providing a fourfold delay reduction for a 6-bit feedback DAC. The front-end integrator implementation also exhibits 25% less kT/C noise than conventional architectures.**

***Index Terms*—Digital-to-analog converter (DAC) mismatch shaping, high-speed analog-to-digital converter (ADC), sigma–delta modulators.**

I. Introduction

THE USE of multibit quantizers in oversampling analog-to-digital converters (ADCs) offers several important benefits, including wider dynamic range (DR), faster integrator settling, and greater stability. While most oversampling converters have employed quantizer resolutions no higher than 4 bits, recent advances in flash ADCs suggest the possibility of reaching a resolution of 6 bits with a small input capacitance, fast conversion, and low power dissipation. For example, the offset-canceling 4-bit 1.25-GHz ADC in [1] can be projected to reach 6 bits with an input capacitance of less than 300 fF and a power dissipation of about 10 mW. However, the correction of the multibit digital-to-analog converter (DAC) nonlinearity in a ΣΔ modulator becomes more difficult, particularly if a low oversampling ratio (OSR) is used to achieve high speed.

This brief introduces a DAC mismatch shaping technique that lends itself to high speeds and high resolutions. The technique also lends itself to compact logic. The feasibility of the concept is demonstrated in a 90-nm CMOS prototype described in [2].

This brief is organized as follows. Section II introduces the proposed mismatch shaping architecture. Section III describes the details of the technique and analyzes it, and Section IV concludes this brief.

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II. DAC Mismatch Shaping Architecture

A. Background

A multitude of techniques that shape the DAC mismatches and push the energy to high frequencies has been reported [3]–[8]. Among these, the tree structure scheme described in [4] provides second-order shaping of the mismatches, but it is only suited for high-OSR modulators. At $OSR = 8$, the approach suffers from low averaging of the mismatches because the oversampling is not fast enough to cycle through all possible combinations of the DAC elements over a sufficiently short time. For example, according to simulations, this technique yields a DR of only 73 dB (in the absence of device noise) with $OSR = 8$ in a fourth-order modulator employing a 4-bit DAC whose capacitors have a mismatch of 0.2%.

Data-weighted averaging (DWA) [3], on the other hand, lends itself better to low-OSR systems. It must, however, deal with two issues. First, in-band tones arising from DAC mismatch patterns degrade the overall signal-to-(noise+distortion) ratio (SNDR), and tone reduction techniques such as those in [5]–[7] inevitably raise the noise floor. Second, more importantly, the complexity of DWA logic exponentially grows with the number of bits, thereby introducing a significant delay [9] and limiting the settling time allowed for the second integrator and the conversion time allowed for the quantizer.

These observations indicate a need for a DAC mismatch shaping technique that is suited to low-OSR systems and can be realized with compact high-speed logic.

B. Basic Idea

Consider the modulator shown in Fig. 1(a), which is derived from the standard second-order loop [10] by factoring out the first integration and inserting it in series with the input and with the DAC. It can be shown that the first DAC mismatch $X_{\rm mis}$ experiences first-order shaping as it appears at the output, i.e.,

$$Y_{\rm out} = z^{-2}X_{in} + (1 - z^{-1})X_{\rm mis}. \tag{1}$$

Thus, the DAC mismatch is suppressed in a manner similar to the quantization noise, obviating the need for explicit randomization and shaping of the mismatches. However, due to "open-loop" integration, the signals at nodes A and B are unbounded.

To avoid an unbounded signal at node B, we return the input integrator to its original position while maintaining the one before $\rm DAC_1$ and inserting a differentiator after $\rm DAC_1$ [Fig. 1(b)]. The transfer function in (1) still applies, but the output of the digital integrator (accumulator) A remains unbounded. That

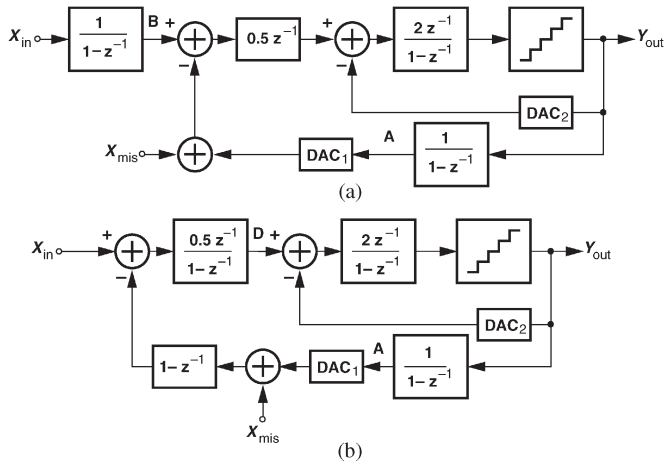

Fig. 1. (a) Factorization of $(1-z^{-1})^{-1}$ to shape $X_{\rm mis}$. (b) Modified structure to avoid overflow at input.

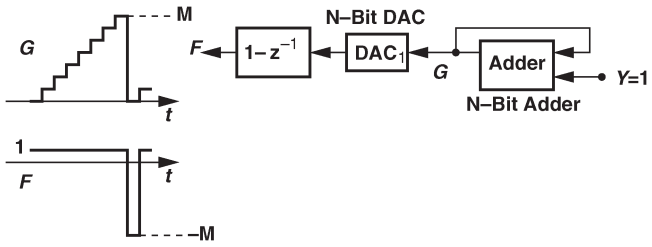

Fig. 2. Effect of accumulator overflow.

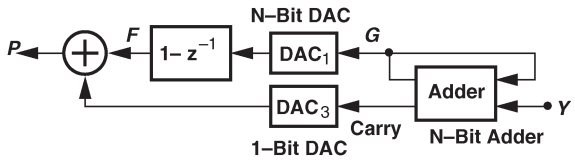

Fig. 3. Modified feedback path to remove overflow.

is, each time the accumulator reaches its maximum, DAC_1 produces a large step, which after differentiation and integration also appears at node D and in $Y_{\rm out}$.

The error resulting from the accumulator overflow can be viewed from another perspective. As shown in Fig. 2, for $Y=1$, the output of the accumulator reaches a value of M and subsequently falls to zero. As a result, the differentiator output F experiences a large negative "glitch" corresponding to $(1-z^{-1})$ times the overflow jump.

The foregoing analysis suggests that the overflow error can be removed if a pulse is added to the signal at node F so as to cancel the negative glitch. Indeed, as shown in Fig. 3, if the carry output of the accumulator is converted to analog form and summed with the differentiator output, then no overflow error occurs. In other words, the system from Y to P has a unity transfer function in the absence of DAC mismatches.

Fig. 4 illustrates a second-order loop incorporating the proposed technique. Note that DAC_1 mismatches are still shaped by $1-z^{-1}$ although DAC_3 is added. Owing to this factor, the DAC mismatch shaping can scale with OSR in a manner similar to quantization noise shaping. Moreover, the technique lends itself to high-speed logic because it requires no randomization.

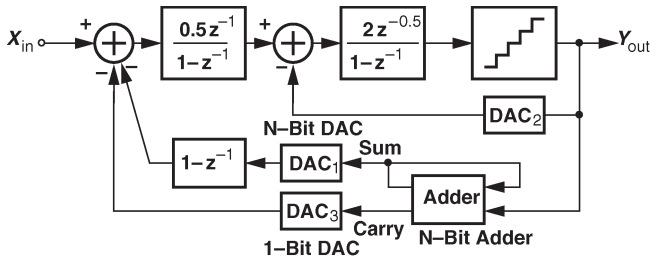

Fig. 4. Second-order $\Sigma\Delta$ modulator with DAC mismatch shaping.

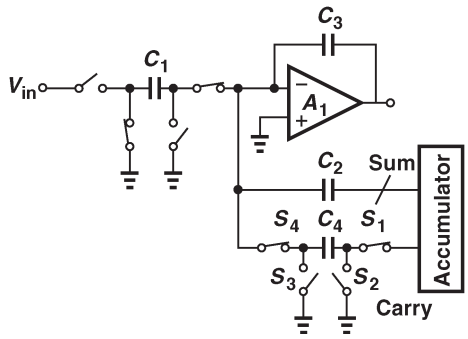

Fig. 5. Front end of first modulator.

C. Issues

The architecture in Fig. 4 entails a number of issues. First, the differentiator following DAC_1 appears to amplify high-frequency noise. This issue is resolved by merging the differentiator with the front-end integrator, thus arriving at a simple amplification function. As shown in Fig. 5, the front end now consists of an input integration network (C_1, C_3, and A_1), a DAC output amplification network (C_2, C_3, and A_1), and a carry integration network (C_4, C_3, and A_1). Capacitor C_2 consists of a segmented (2^N-1)-bit array (as subsequently described).

The second issue relates to mismatches between DAC_1 and DAC_3 in Fig. 4. Since the carry output only occurs occasionally, such mismatches are weighted by a small factor. Furthermore, the design is modified to obtain a signed carry, thereby forcing its average to zero. Fig. 6 depicts the path from the quantizer to the front end. Preceded by a thermometer/binary converter (TBC), the accumulator produces a 1.5-bit signed carry, which is applied to a single capacitor by means of S_1-S_4.[1] This modification further relaxes the matching requirements between DAC_1 and DAC_3 for a given DR requirement, as will be shown in Section III-C.[2]

III. Circuit Details and Analysis

A. Logic Implementation

The delay of the DAC logic shown in Fig. 6 directly adds to the delay of the quantizer in the feedback loop of a $\Sigma\Delta$ modulator. In discrete-time loops, the delay of this logic must be less than half a clock cycle, and in continuous-time loops, it may cause instability. The implementation of the architecture

[1]DAC_3 is unconditionally linear since it is implemented using a single capacitor and by only reversing the sign of the voltage across the capacitor.

[2]Since no element rotation is required, the TBC following the accumulator is optional and can be removed.

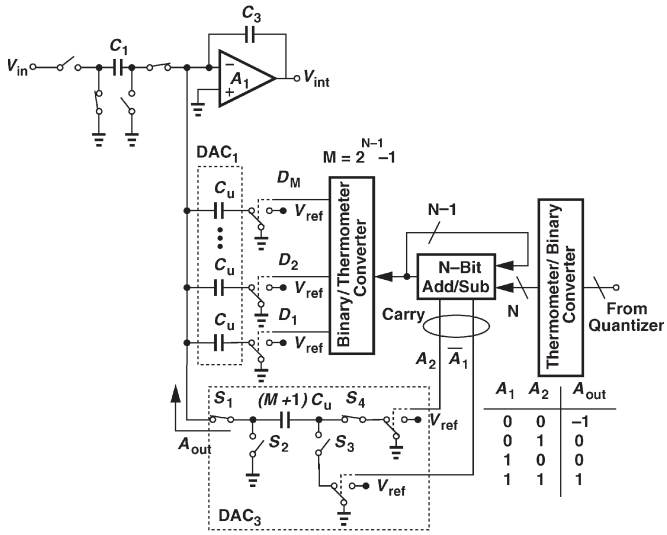

Fig. 6. Detailed diagram of feedback and DAC path.

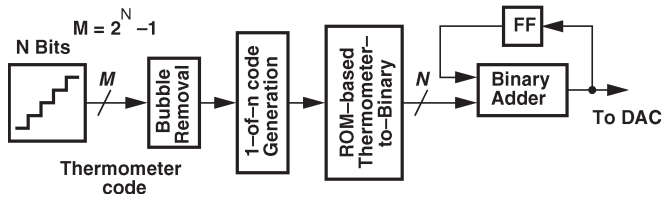

Fig. 7. First proposed implementation of the proposed architecture.

in Fig. 6 must therefore minimize the extra delays. Since the quantizer produces a thermometer code, one may attempt to realize the accumulator using thermometer-code adders. However, such a solution suffers from bubble errors and exponential growth of delay.

Another option is to perform the addition in the binary domain. With a standard binary adder [11], the total accumulator delay is then given by $(N-1) \times t_{\rm carry} + t_{\rm sum}$, where $t_{\rm carry}$ and $t_{\rm sum}$ are the carry and sum output delays of a full adder (FA) circuit, respectively. Fig. 7 shows the block diagram of the proposed implementation of the new DAC mismatch shaping technique. A bubble removal operation is followed by a 1-of-n converter and a ROM-based TBC. In this brief, bubble removal is merged with thermometer-to-binary conversion, yielding a total delay of $(2N-3) \times t_{\rm cell}$, where $t_{\rm carry} = t_{\rm sum} = t_{\rm cell}$.

As an example, Fig. 8 shows the implementation for a 3-bit quantizer combined with the accumulator to reduce the total delay. For an N-bit binary data (2^N thermometer inputs), the total delay is given by $(2N-2) \times t_{\rm cell}$.[3]

B. Advantages of Proposed Technique

As mentioned in Section II-A, the tree structure reported in [4] becomes less effective at low OSRs, and the DWA logic exponentially grows with the number of bits. In this section, we compare the proposed technique with DWA.

Fig. 9(a) shows a quantizer, a TBC, and a DWA logic consisting of an accumulator and a switching matrix. Fig. 9(b) shows the critical path from the input to the output of the switching

[3]The total delay is less than the sum of the TBC delay and the adder delay because the data are processed in parallel.

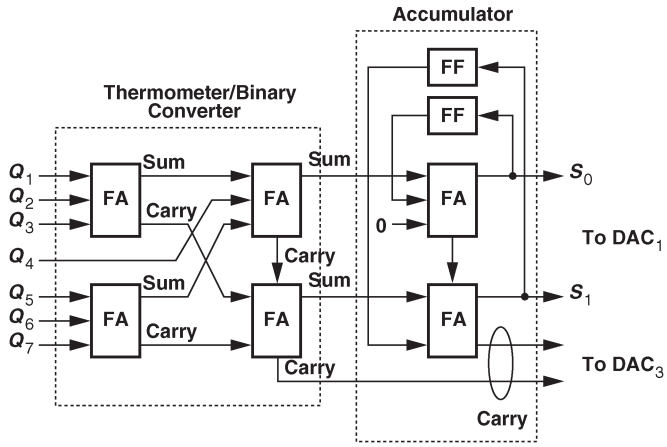

Fig. 8. Feedback data path logic using FAs.

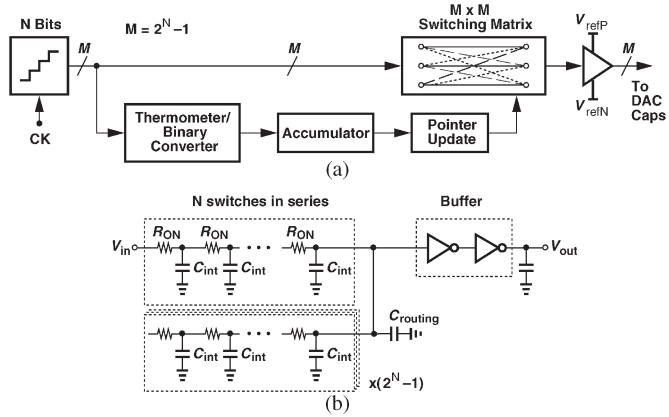

Fig. 9. (a) DWA logic. (b) Critical path for the switching matrix.

matrix, where each input is directed to the appropriate output through a binary tree. For an N-bit quantizer (2^N levels), the critical path consists of N switches in series, with each switch in the path driving two junction capacitances. The last switch in the chain, on the other hand, drives $2^N - 1$ junction capacitances. This leads to a total chain delay that exponentially grows with the number of bits in the quantizer. The layout exacerbates this effect because the total routing capacitance rises at a higher rate than the total junction capacitance.[4] Note that pipelining this logic degrades the stability of the loop.

Fig. 10 plots the total delay of the switching matrix (including the buffers) as a function of the DAC resolution. Obtained from the transistor-level simulations in 90-nm CMOS technology, this plot reveals that the delay rises from 250 ps for a 2-bit system to 2.9 ns for a 6-bit system.

Fig. 10 repeats the simulation for the proposed mismatch shaping technique and the logic shown in Fig. 8(b). It is observed that the delay remains smaller for all resolutions and, more importantly, is only one-fourth of the DWA logic delay for a resolution of 6 bits. In other words, while DWA logic prohibits operation of the $\Sigma\Delta$ modulator at a clock frequency of, say, 300 MHz (because it leaves no time for DAC and integrator settling), our proposed approach allows it with comfortable margin.

[4]For example, for a 1-bit increase in N, the number of branches in Fig. 9(b) is doubled, and M in Fig. 9(a) is also doubled, thus quadrupling the physical dimensions of the matrix.

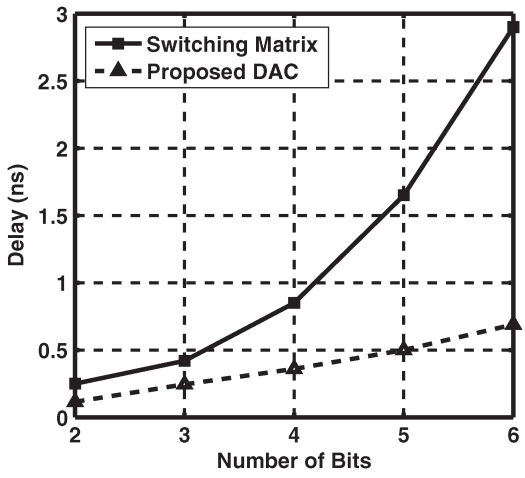

Fig. 10. Delay versus number of bits in the DAC for (solid line) the switching matrix and (dashed line) the proposed DAC logic.

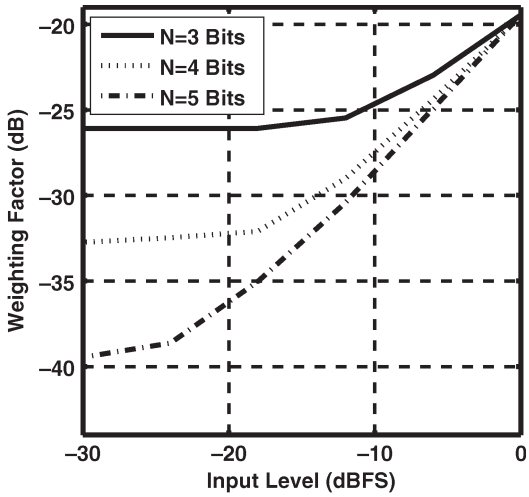

Fig. 11. Improvement factor of mismatch between DAC_1 and DAC_3.

C. Effect of Mismatches

As mentioned in Section II-C, the mismatches within DAC_1 in Fig. 6 are shaped by $1 - z^{-1}$, and the mismatches between DAC_1 and DAC_3 are suppressed by assigning a polarity to the carry. In this section, we formulate these effects analytically.

Referring to Fig. 6, we note that the unit capacitors in DAC_1 form an amplifier with the integrator. Thus, the change in $V_{\rm int}$ and hence the charge injected by DAC_1 into the virtual ground are proportional to the *change* in the thermometer code input of DAC_1. The total charge injected by DAC_1 and DAC_3 at discrete time index k can be written as

$$Q_{\rm DAC}(k) = \sum_{j=1}^{M} C_u V_{\rm ref} D_j(k) - \sum_{j=1}^{M} C_u V_{\rm ref} D_j(k-1) + (M+1) C_u V_{\rm ref} A_{\rm out}(k). \quad (2)$$

where $M = 2^{N-1} - 1$ (N is the quantizer resolution), and $A_{\rm out}(k)$ is the DAC_3 output at time k. Let us now assume mismatches among the unit capacitors comprising the two DACs. Then, the first two summations can be merged but with a mismatch variable e_{Dj}, i.e.,

$$Q_{\rm DAC}(k) = \sum_{j=1}^{M} C_u (1 + e_{Dj}) V_{\rm ref} \left[D_j(k) - D_j(k-1) \right] + (M+1) C_u (1 + e_A) V_{\rm ref} A_{\rm out}(k) \quad (3)$$

where e_A is the percentage deviation of the total capacitance in DAC_3 from the nominal value of $(M+1)C_u$. Equation (3) reveals two error components

$$Q_{\rm error}(k) = C_u V_{\rm ref} \sum_{j=1}^{M} e_{Dj} \left[D_j(k) - D_j(k-1) \right] + (M+1) C_u V_{\rm ref} e_A A_{\rm out}(k) \quad (4)$$

which translates to

$$Q_{\rm error}(z) = C_u V_{\rm ref} (1 - z^{-1}) \sum_{j=1}^{M} e_{Dj} D_j(z) + (M+1) C_u V_{\rm ref} e_A A_{\rm out}(z). \quad (5)$$

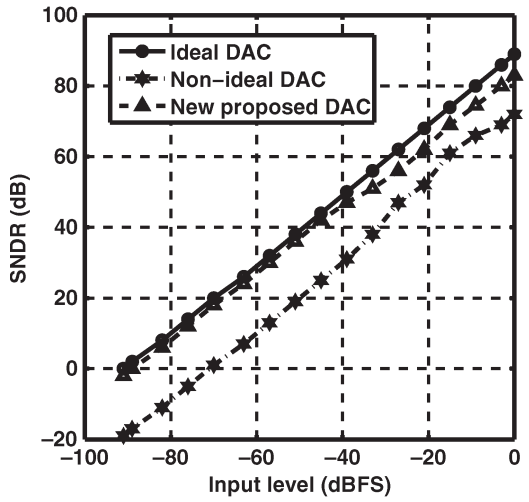

Fig. 12. SNDR for a 3-bit modulator with an ideal DAC, nonideal thermometer DAC, and the proposed new DAC.

The DAC mismatches are shaped by $1 - z^{-1}$. The mismatches between DAC_1 and DAC_3 are not only weighted by $A_{\rm out}$ but also scaled down by the OSR in a manner similar to kT/C and op amp noise. The weighting by $A_{\rm out}$ depends on the occurrence rate of the carry, which in turn depends on the input level. (A larger input level speeds up the accumulation, generating a carry more frequently.) Fig. 11 plots the weighting factor due to $A_{\rm out}$ as a function of the input for different quantizer resolutions. These results are obtained by the simulation of the overall fourth-order system. The key point here is that, at full scale, the signed carry reduces the second error term in (5) by 20 dB.[5] A $\Sigma\Delta$ modulator with an ideal DR of 91 dB (peak SNDR of 88 dB) with a 3-bit quantizer (3-bit DAC) is simulated in three cases: 1) an ideal DAC; 2) a DAC with 0.25% random mismatches; and 3) the same as 2) but with our proposed technique. Fig. 12 shows the SNDR plots versus the input level. The DR is 91 dB for the ideal case, falling to 74 dB for the second case, and rising to 86 dB in the presence of our technique.

[5]System-level simulations using Matlab indicate that the spurious tones resulting from capacitor mismatches of 0.5% or better are 90 dB below the full scale for a quantizer resolution of 3 bits or higher.

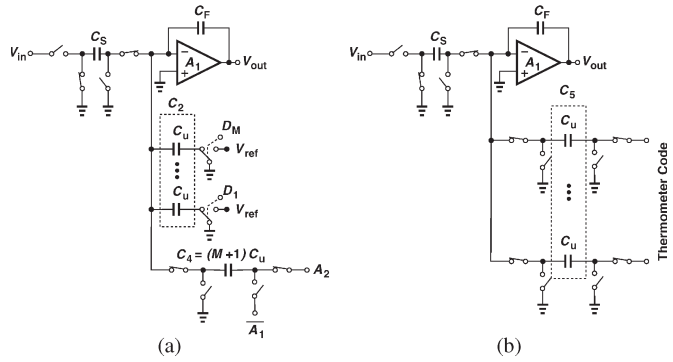

Fig. 13. (a) New and (b) standard modulator front ends.

D. Comparison With Standard Front End

In this section, we compare two important attributes of the front end developed above and shown in Fig. 13(a) with those of the standard architecture shown in Fig. 13(b). The connection of $C_4 = (M+1)C_u = 2^N C_u$ to the virtual ground node in Fig. 13(a) may appear to degrade the integrator loop gain considerably. However, it is important to note that the entire capacitance of DAC_1 and DAC_3, $C_2 + C_4 = (2^N - 1)C_u + 2^N C_u$ is chosen equal to the total capacitance of the simple DAC in Fig. 13(b), i.e., C_5 (typically equal to $0.5C_F$). In other words, the design begins with $(2^N - 1)C_u + 2^N C_u = 0.5C_F$ and determines C_u, ensuring the same loop gain as in the standard architecture.

Another point of comparison relates to the total kT/C noise in the two cases. In Fig. 13(a), the kT/C noise of $C_2 = (2^N - 1)C_u$ is amplified by a factor of $(C_2/C_F)^2$ as it appears in V_{out} and multiplied by $|1 - z^{-1}|^2$ when referred to the main input. Thus, the kT/C noise associated with C_2 experiences *first-order shaping*. The sampling capacitors, i.e., C_4 in Fig. 13(a) and C_5 in Fig. 13(b), on the other hand, contribute unshaped input-referred kT/C noise equal to $(kT/C_j)(C_j/C_F)^2/(C_S/C_F)^2 = kTC_j/C_S^2$ for $j = 4$ and 5. Since $C_4 \simeq C_5$, the proposed topology exhibits significantly *less noise*. Since $C_S \simeq C_5$, the total input-referred noise is equal to $1.5kT/C_S$ in Fig. 13(a) and $2kT/C_S$ in Fig. 13(b). We therefore conclude that all of the capacitors in Fig. 13(a) can be 25% smaller than those in Fig. 13(b), saving a proportional power in the integrator.[6]

[6]In Fig. 13(b), sharing capacitors between input and DAC and in the absence of low-output-impedance reference buffers result in high-order harmonics at the output spectrum [9]. These buffers are power hungry.

IV. Conclusion

This brief has introduced a DAC mismatch shaping technique that lends itself to both low OSRs and compact high-speed logic. Unlike prior approaches, the proposed method simply shapes the mismatches by the $\Sigma\Delta$ modulator loop—in a manner similar to the shaping of the quantization noise. The efficacy of the technique is also experimentally demonstrated in [2]. The proposed mismatch shaping technique can also be combined with other schemes to create higher-order shaping and achieve greater accuracies.

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