A 200-MHz 15-mW BiCMOS Sample-and-Hold Amplifier with 3 V Supply

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***Abstract*—A sample-and-hold amplifier designed for the front end of high-speed low-power analog-to-digital converters employs a BiCMOS sampling switch and a low-voltage amplifier to achieve a sampling rate of 200 MHz while allowing input/output voltage swings of 1.5 V with a 3-V supply. The circuit also incorporates a cancellation technique to relax the trade-off between the hold-mode feedthrough and the sampling speed. Fabricated in a 20-GHz 1-μm BiCMOS technology, an experimental prototype exhibits a harmonic distortion of -65 dB with a 10-MHz analog input and occupies an area of 220 $\times$150 μm^2. The measured feedthrough is -52 dB for a 50-MHz analog input and the droop rate is 40 μV/ns.**

I. Introduction

THE DESIGN of low-voltage analog and mixed-signal circuits often imposes severe speed and precision limitations upon signal processing systems. In multistep analog-to-digital (A/D) converters, for example, the front-end sample-and-hold amplifier (SHA) must achieve high speed and high linearity with low power dissipation while the limited voltage headroom constrains its dynamic range.

This paper describes the design of a BiCMOS sample-and-hold circuit intended for use at the front end of high-speed low-power A/D converters with 10-b resolution. The primary challenge has been to attain a voltage swing of 1.5 V in a 3.3-V system with negligible sacrifice in speed, linearity, or power dissipation.

Using a BiCMOS sampling switch and a low-voltage amplifier, the SHA achieves a sampling rate of 200 MHz with a harmonic distortion of -65 dB for a 10-MHz analog input. The circuit also employs a feedthrough cancellation technique to allow the use of small sampling capacitors, thereby relaxing the trade-off between the acquisition speed and the hold-mode feedthrough. The measured feedthrough for a 50-MHz analog input is -52 dB, and the droop rate is 40 μV/ns.

The next section of this paper provides a brief overview of conventional sampling techniques and their drawbacks for low-voltage operation. In Section III, the architecture and circuit details of the BiCMOS SHA are described, and in Section IV, experimental results are presented.

II. Conventional Sampling Circuits

A sample-and-hold circuit often used in CMOS A/D converters is depicted in Fig. 1. Here, in the acquisition mode S_1-S_4 are on, and S_5 and S_6 are off. Thus, the op amp is reset, and the voltage across C_1 and C_2 tracks the analog input. In the transition to the hold mode, S_3 and S_4, and subsequently, S_1 and S_2 turn off, and S_5 and S_6 turn on. While this switching sequence suppresses input-dependent charge injection, the circuit fundamentally suffers from a long hold settling time because the differential output always starts from zero at the beginning of the hold mode. Furthermore, the use of an op amp to establish virtual ground at nodes P and Q makes the operation from low supply voltages difficult. More specifically, (a) the op amp suffers from various trade-offs in dynamic range, linearity, and speed as its supply voltage is reduced, and (b) the op amp requires an input/output common-mode level approximately equal to half the supply voltage, thereby limiting the gate-source overdrive voltage of S_3–S_6 and degrading the settling behavior.

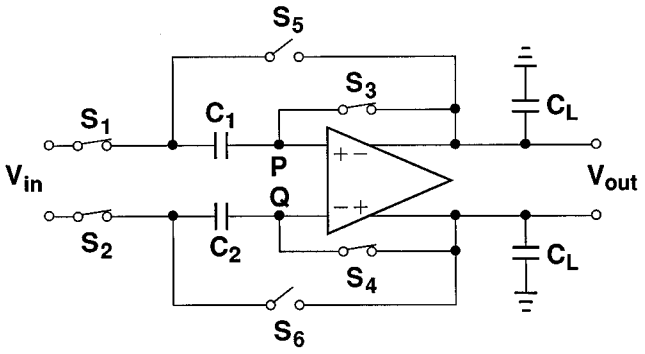

Fig. 1. CMOS SHA architecture.

For comparison purposes, the circuit of Fig. 1 was designed and simulated in a 0.6-μm CMOS technology with a folded-cascode op amp and 0.2-pF load capacitors. These simulations indicate that the maximum sampling rate of the circuit is no more than 25 MHz. This can be partly attributed to the large device widths required in the op amp so as to achieve adequate voltage swings. In fact, since the cut-off frequency f_T of a MOSFET is given by

$$2\pi f_T = \frac{g_m}{C_{gs} + C_{gd}} \tag{1}$$

$$= \frac{g_m}{2WL_{\text{eff}}C_{ox}/3 + 2WC_{ov}} \tag{2}$$

and, for square-law devices, $g_m = \mu C_{ox} W(V_{GS} - V_{TH})/L_{\text{eff}}$, we have

$$2\pi f_T = \frac{\mu C_{ox}(V_{GS} - V_{TH})}{L_{\text{eff}}(2L_{\text{eff}}C_{ox}/3 + 2C_{ov})}. \tag{3}$$

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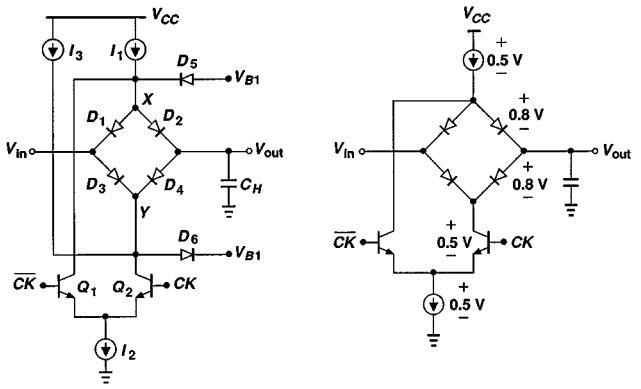


(a) (b)

Fig. 2. Sampling diode bridge.

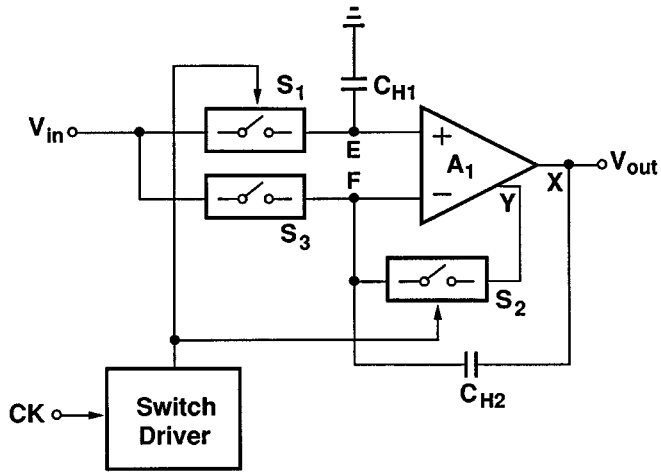
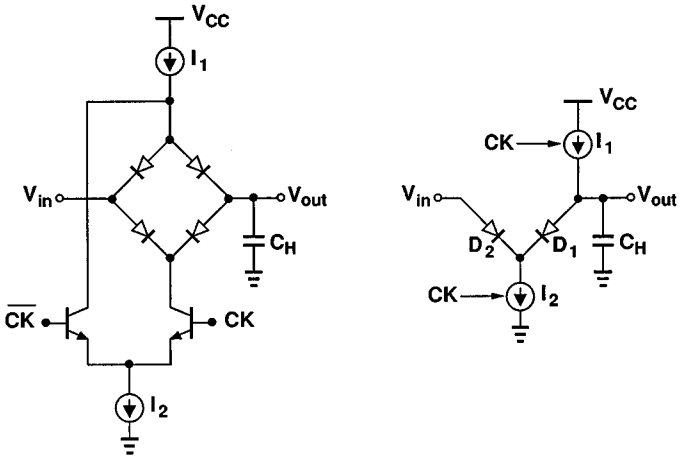


Fig. 3. BiCMOS SHA architecture.



(a) (b)

Fig. 4. Modification of conventional bridge to increase the headroom.

This equation suggests a sharp drop in speed if device width is increased to reduce $(V_{GS} - V_{TH})$ to a few hundred millivolts while maintaining the same bias current. For submicron devices, on the other hand, simulations imply a trend close to $f_T \propto (V_{GS} - V_{TH})^{0.5}$.

High-speed bipolar sample-and-hold circuits have traditionally employed diode bridges for the best trade-off between speed and resolution. Fig. 2(a) illustrates such an implementation. In addition to the bridge, the circuit incorporates clamp diodes D_5 and D_6 to limit the swings at nodes X and Y. To calculate the minimum supply voltage, the circuit can be simplified as shown in Fig. 2(b), where it is assumed that $V_D \approx 0.8$ V, $V_{CE,\min} \approx 0.5$ V, and the minimum voltage across I_1 and I_2 is 0.5 V. Thus, $V_{CC,\min} \approx 3.1$ V.

The above observations exemplify the difficulties in scaling the supply voltage of sampling circuits, indicating the need for low-voltage sampling techniques.

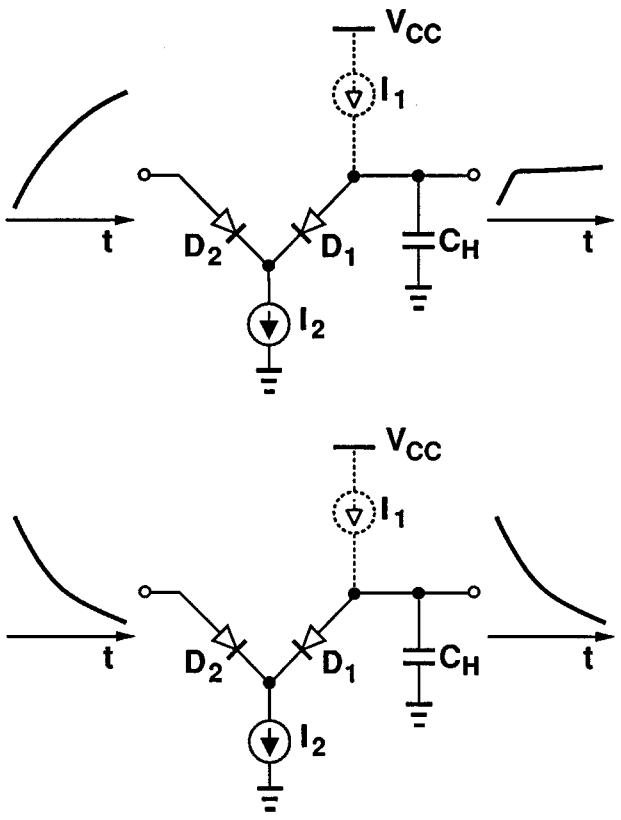


Fig. 5. Effect of slew rate if I_1 turns off before I_2.

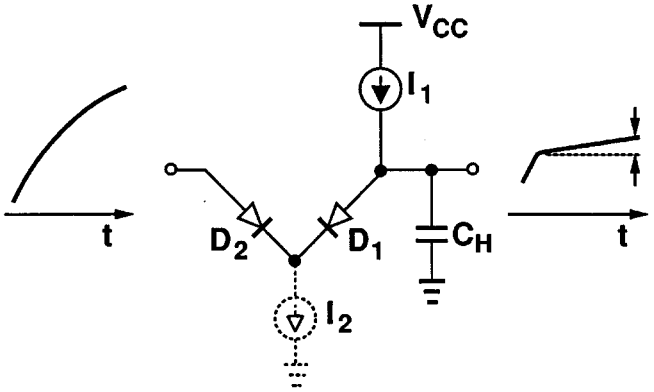


Fig. 6. Hold mode offset generated when I_2 turns off before I_1.

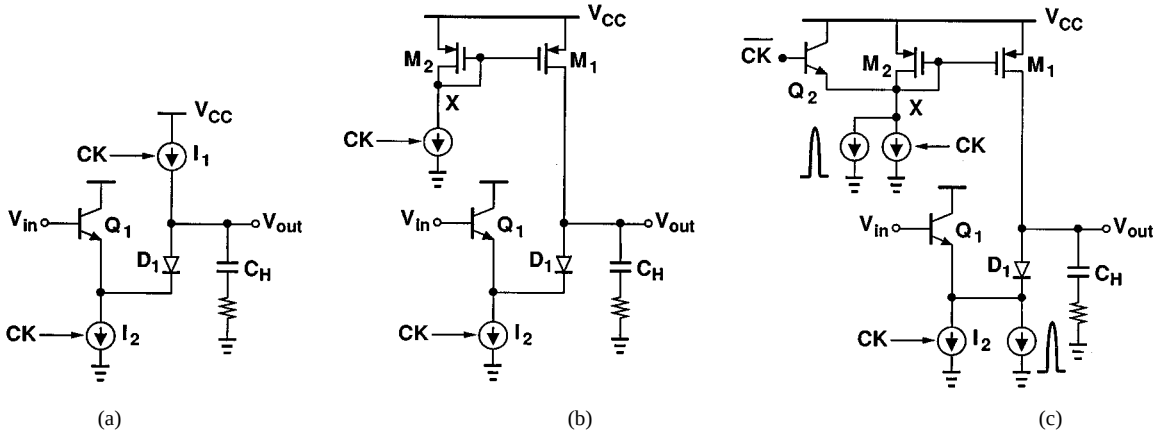


Fig. 7. Evolution of the sampling switch.

III. BiCMOS Sample-and-Hold Amplifier

A. Architecture

The SHA architecture is shown in Fig. 3. It consists of identical BiCMOS switches S_1-S_3, equal capacitors C_{H1} and C_{H2}, amplifier A_1, and a switch driver circuit that interfaces the input clock with S_1 and S_2. Switch S_3 is always off, and its role will be explained later. Outputs X and Y of the amplifier differ by $V_{BE} \approx 0.8$ V but are identical otherwise.

In the sampling mode, S_1 and S_2 are on, the voltage across C_{H1} tracks V_{in}, and A_1 is configured as a unity-gain amplifier. In the transition to the hold mode, S_1 and S_2 turn off, and C_{H2} maintains a unity-gain loop around A_1. In this topology, both the charge injection of S_1 and S_2 and the hold-mode droop appear as a common-mode voltage at the inputs of A_1, thereby allowing the use of smaller values for C_{H1} and C_{H2} than in a single-ended case.

It is important to note that with a 3-V supply, S_1–S_3 in Fig. 3 cannot be easily implemented using only MOS devices. This is because, as mentioned in Section II, the bias voltage at E and F is typically around half of the supply voltage, leaving a small gate-source overdrive for MOS switches connected to these nodes and hence slowing down the acquisition. This problem is especially acute if low-threshold MOSFET's are not available.

The sampling switches used in this paper incorporate bipolar devices in the signal path. A critical issue in such a design is the hold-mode feedthrough because the junction capacitance of bipolar transistors can be substantial even when these devices are off. This translates into a direct trade-off between the size of the sampling capacitor(s) and the magnitude of the feedthrough signal, thereby limiting the speed. This issue is addressed in Section III.E.

B. BiCMOS Sampling Switch

The implementation of S_1–S_3 in Fig. 3 has evolved from the conventional diode bridge of Fig. 2(b). As illustrated in Fig. 4(b), to increase the dynamic range, the upper diodes are removed, and the emitter-coupled pair is replaced with a single-ended current switch. These modifications increase the maximum allowable voltage swings by approximately 1.3 V,

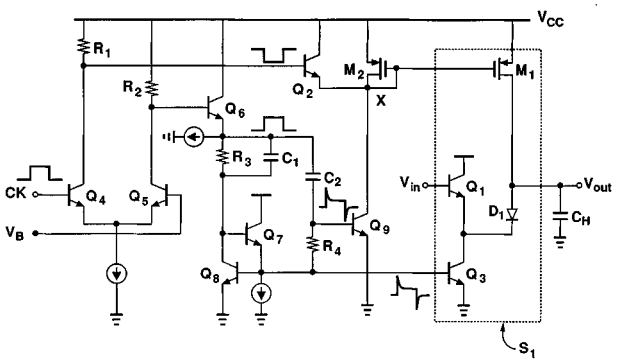


Fig. 8. Switch driver.

allowing a dynamic range of 10 b with a 3-V supply. However, unlike the conventional bridge, in this topology, both I_1 and I_2 must turn off at the end of the acquisition mode.

Since I_1 and I_2 in Fig. 4(b) are driven by inherently different signal paths, it is difficult to guarantee that they switch simultaneously. We therefore consider two cases. Suppose I_1 turns off *before* I_2 (Fig. 5). Then, for positive slew rates, most of I_2 flows from D_1, and the voltage across C_H remains relatively constant. For negative slew rates, on the other hand, most of I_2 serves to discharge C_H, and the output tracks the input. This effect can also be viewed as slew-dependent switch on-resistance, resulting in harmonic distortion while I_2 turns off.

In the second case, we assume I_1 turns off *after* I_2 (Fig. 6). Then, the two diodes are off, and I_1 continues to charge the capacitor, producing a constant offset in the held value. This offset is cancelled in the architecture of Fig. 3 because it appears as a common-mode disturbance. We have chosen this case and implemented proper timing in the switch driver to guarantee that I_2 always turns off before I_1.

An interesting point of contrast between the conventional bridge of Fig. 2(a) and the sampling switch of Fig. 4(b) relates to their pedestal error. In the former circuit, the coupling of the voltage change at nodes X and Y to the output through the junction capacitance of D_2 and D_4 introduces nonlinearity unless V_{B1} is made to track V_{out} [1], [2], a remedy that may increase the hold-mode settling time [3]. In the latter circuit,

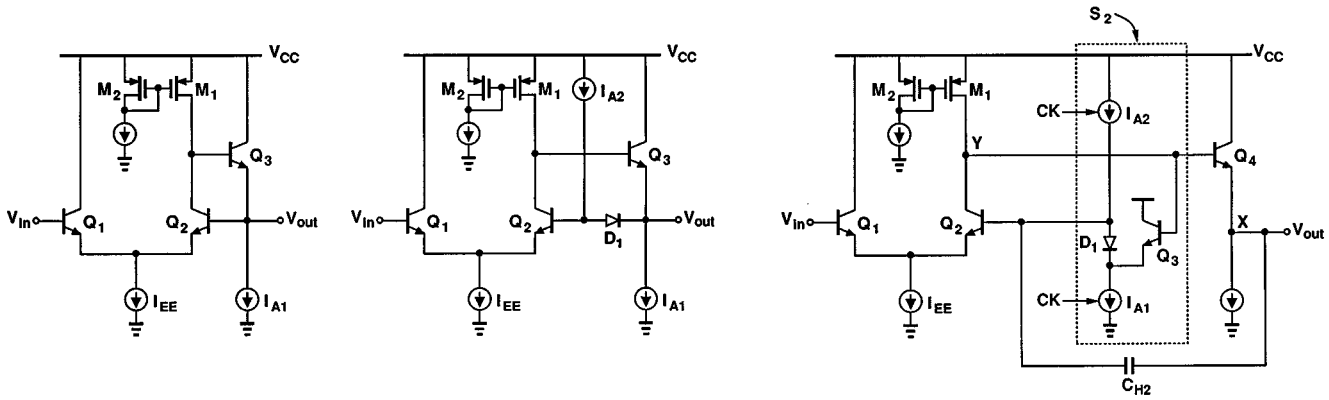


Fig. 9. Evolution of output buffer.

on the other hand, there is no such effect, and the charge injection due to I_1 and I_2—which is relatively independent of the analog input—is cancelled by the architecture of Fig. 3. The trade-off is that the shunt path provided by D_5 and D_6 in Fig. 2(a) is not present, making the hold-mode feedthrough larger than that of the conventional bridge.

In Fig. 4(b), diode D_2 can be replaced with an emitter follower to reduce the transient currents drawn from the input (Fig. 7(a)). Since the output inductance of the emitter follower degrades the settling time, a small resistor is placed in series with C_H to dampen the ringing. The switched current source I_1 can be realized as shown in Fig. 7(b). However, the small transconductance of M_2 and the large capacitance at node X yield a time constant greater than 1 ns. Note that the time constant itself increases as M_2 turns off, slowing down the switching considerably. This issue is resolved using two techniques as illustrated in Fig. 7(c). First, to minimize the aperture window, emitter follower Q_2 is added so that it rapidly pulls node X high when M_1 and M_2 must turn off. Second, to speed up the turn-on, an additional impulse of current is pulled from M_2 on the proper clock edge, thereby discharging node X quickly. The switched current source I_2 is also accompanied with such an impulse to match the initial surge in the drain current of M_1. Note that Q_2, M_2, and their associated current sources can be shared among several sampling switches. The clock signals and current impulses required by the BiCMOS switch are generated by the switch driver.

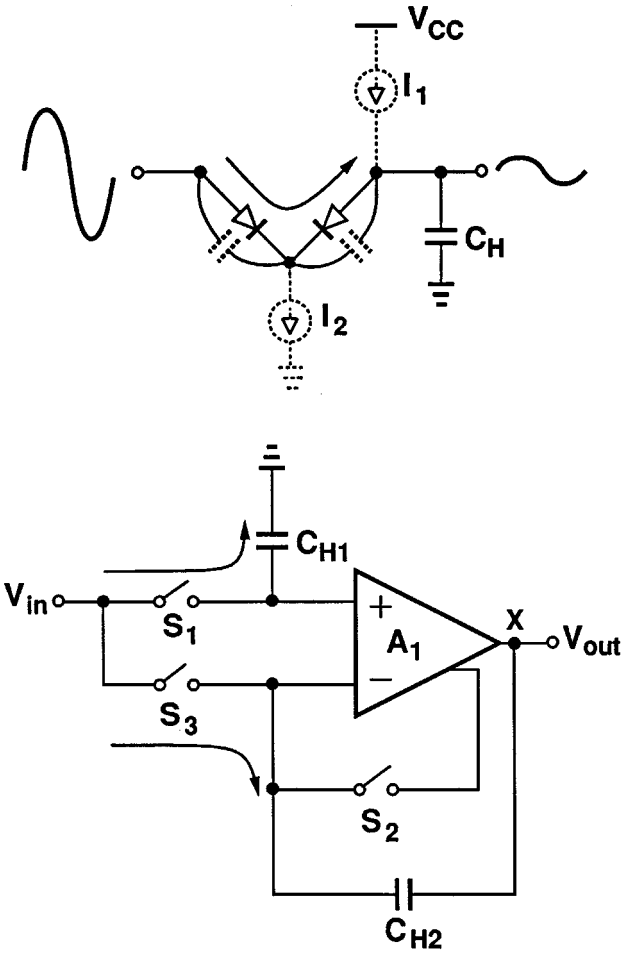


Fig. 10. Feedthrough cancellation.

C. Switch Driver

Fig. 8 shows the switch driver and its interface with the BiCMOS sampling switch S_1. The driver consists of: an input differential pair providing complementary clocks for Q_2 and Q_6; a slow/fast network R_3, R_4, C_1, C_2, Q_7, and Q_8; and Q_3 and Q_9 operating as switched current sources. Capacitors C_1 and C_2 couple the logic transitions at the emitter of Q_6 to the bases of Q_3 and Q_9, respectively, thus producing impulses 0.3 ns wide in I_{C3} and I_{C9}. The final current levels are set primarily by the collector current of Q_8 and sizing of Q_3 and Q_9.

In the circuit of Fig. 8, the tail current of Q_4–Q_5 is approximately equal to 0.25 mA and $R_1 = R_2 = 6\,\text{k}\Omega$. The collector current of Q_3 in the acquisition mode is about 1 mA, $C_H = 0.5$ pF, and M_1 has a $W/L = 100\,\mu\text{m}/1\,\mu\text{m}$ to supply 0.5 mA with a small gate-source overdrive voltage.

As mentioned previously, the switch driver must turn off Q_3 before M_1 to avoid harmonic distortion in the sampled signal. To understand how this timing is guaranteed, suppose

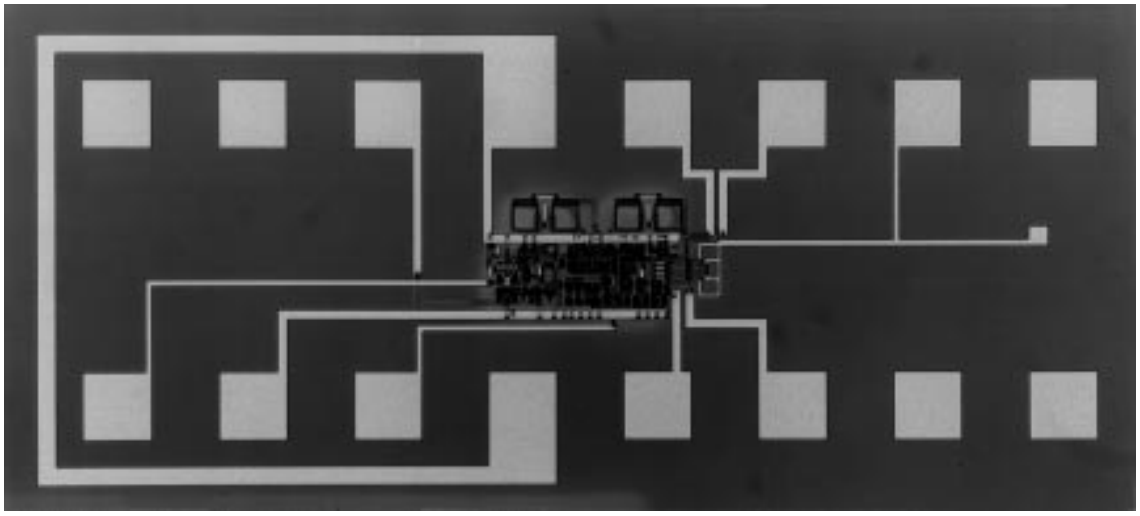
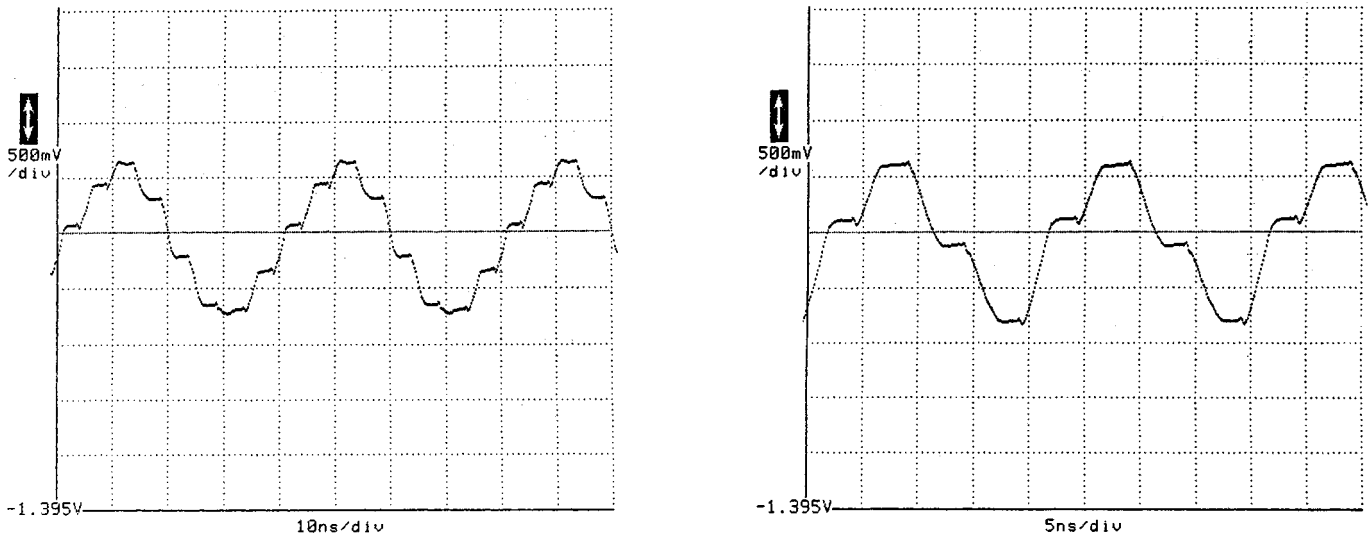


Fig. 11. Die photograph.



(a) (b)

Fig. 12. Measured output at 200-MHz sampling rate with analog input at (a) 25 MHz. (b) 50 MHz.

in Fig. 8, Q_4 turns off, and Q_5 turns on. Then, the voltage at node F (collector of Q_5) begins to fall from V_{CC}, directly reducing the base voltage of Q_3 through C_1 and Q_7, and the base voltage of Q_9 through C_2. Therefore, a change of approximately -10 kT/q in V_F is sufficient to turn off both Q_3 and Q_9. However, the long time constant at node X (before Q_2 turns on) delays the turn-off of M_1. We also note that since V_E (at the collector of Q_4) begins from $V_{CC}-$ 1.5 V and reaches $V_{CC}-1.5\,\mathrm{V}+$ 10 kT/q when V_F has dropped by 10 kT/q, Q_2 is still off when Q_3 and Q_9 turn off.

In the switch driver, the current through R_3 and hence the collector current of Q_8 are supply-dependent. This problem can be solved by means of a replica cancellation circuit.

D. Output Buffer

The amplifier A_1 in Fig. 3 must efficiently drive the input capacitance of the following A/D converter. While it is desirable to employ MOS devices at the input of A_1 so as to achieve a low droop rate, the low open-loop gain and high closed-loop output impedance of such an implementation severely limit the output settling speed (as was noted for the CMOS op amp of Fig. 1). Fig. 9 illustrates the evolution of the amplifier topology. Shown in Fig. 9(a) is a BiCMOS unity-gain stage with low output impedance but consuming a voltage headroom of $|V_{DS1}| + V_{BE3} + V_{BE2} + V_{IEE} \approx$ 2.5 V. To relax the headroom constraint, a level shifter can be placed in series with the base of Q_2, as depicted in Fig. 9(b).

In Fig. 9(b), the circuit comprising Q_3, D_1, I_{A1}, and I_{A2} happens to be the same as the sampling switch of Fig. 7(c) and can operate as such, thereby performing the role of S_2 in Fig. 3. In order to maintain feedback after this switch turns off, another emitter follower Q_4 and a capacitor C_{H2} are added as shown in Fig. 9(c).

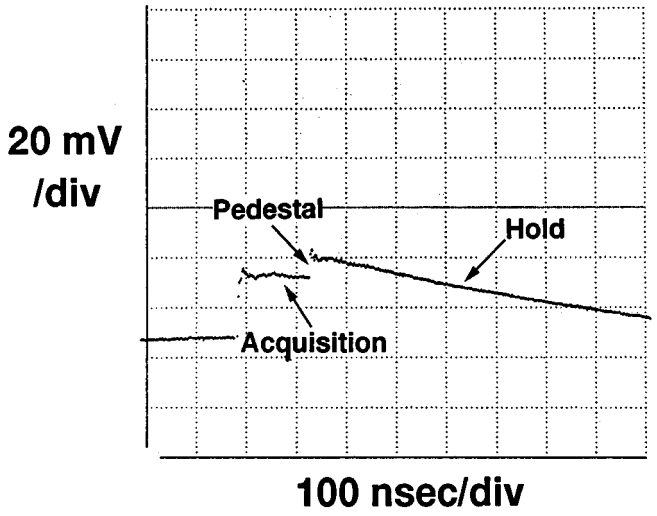


Fig. 13. Hold mode droop and pedestal.

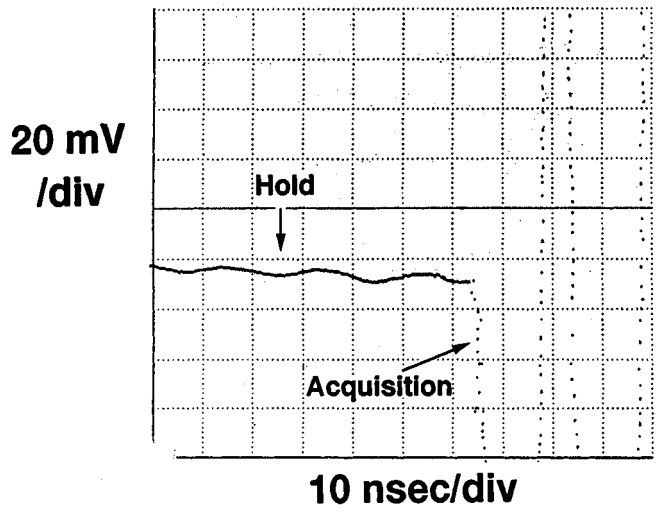


Fig. 14. Hold mode feedthrough with 50-MHz analog input.

Note that the small-signal resistance of D_1 slightly degrades the amplifier phase margin but Q_4 is sized such that its base-collector capacitance ($\approx$ 100 fF) compensates the circuit reliably.

In this circuit, the input differential pair has a tail current of 0.2 mA, and the output transistor is biased at 2 mA.

E. Feedthrough Cancellaation

As mentioned in Section III.A, the diode switches introduce significant feedthrough of the analog input during the hold mode, necessitating the use of large sampling capacitor(s). In the architecture of Fig. 3, this limitation is overcome by allowing S_1 and S_3 conduct equal feedthrough signals to both inputs of the amplifier (Fig. 10). This technique remains effective as long as the output impedance seen at node X is sufficiently small. It can be shown that if the open-loop gain and output impedance of the amplifier are A_0 and R_0,

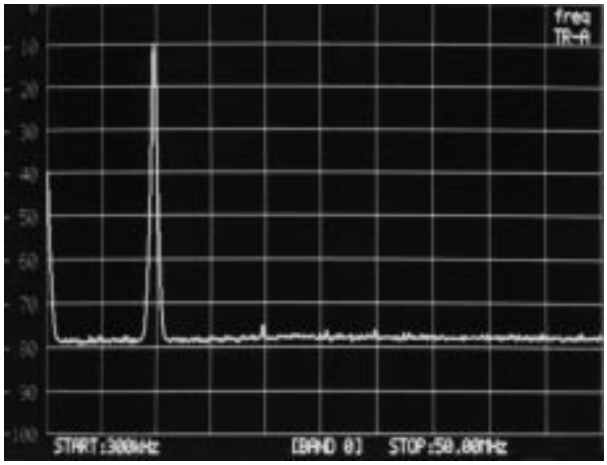


Fig. 15. Output spectrum with 200-MHz sampling rate and 10-MHz input (Horiz., 5 MHz/div.; Vert., 10 dB/div.).

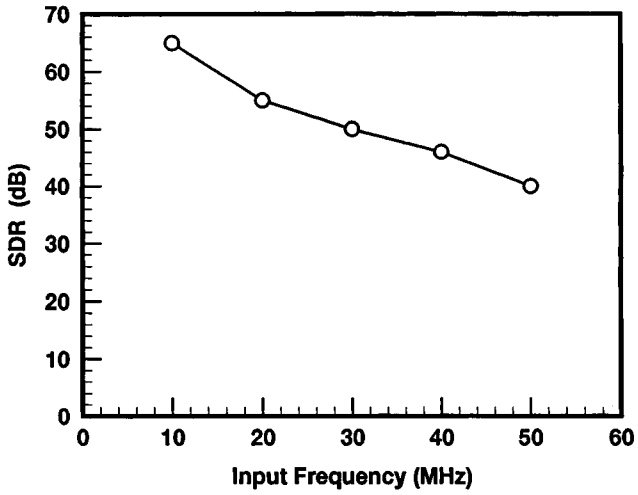


Fig. 16. Output harmonic distortion as a function of analog input frequency with a sampling rate of 200 MHz.

respectively, then the net feedthrough is given by

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) \approx \frac{C_p R_0 s}{C_p R_0 s + A_0} \tag{4}$$

where C_p is the total feedthrough capacitance of each switch (assumed to be much less than C_1 and C_2).

Simulations indicate that the net feedthrough is 60 dB below the analog input for frequencies as high as 100 MHz.

IV. Experimental Results

The sample-and-hold amplifier has been fabricated in a 20-GHz 1-μm BiCMOS technology [4]. Shown in Fig. 11 is a photograph of the prototype, whose active area measures approximately 220 μm $\times$ 150 μm. The circuit has been tested on wafer using Cascade probes and a Tektronix active probe. All tests have been performed with a 3-V supply. The SHA dissipates 15 mW: 7 mW in A_1, 6 mW in S_1 and S_2, and 2 mW in the switch driver.

Since the SHA is not capable of driving a 50-Ω load, accurate measurement of its acquisition and hold settling times

TABLE I
SHA CHARACTERISTICS

Sampling Rate	**200 MHz**
Harmonic Distortion	**−65 dB @ 10 MHz**
Feedthrough	**−52 dB @ 50 MHz**
Droop	**40 μV/nsec**
Voltage Swing	**1.5 V**
Pedestal	**8 mV**
Power Dissipation	**15 mW**
Supply	**3 V**
Technology	**20-GHz 1-μm BiCMOS**

has not been possible. Simulations suggest a 10-b acquisition time of 2.2 ns and a hold settling time of 1.2 ns.

Table I summarizes the performance of the BiCMOS SHA.

Fig. 12(a) and (b) show the measured output at 200-MHz sampling rate with input sinewaves of 25 and 50 MHz, respectively. Fig. 13 depicts the droop in the hold mode, indicating a droop rate of approximately 40 μV/ns. The pedestal error is approximately equal to 8 mV. The hold-mode feedthrough with a 50-MHz analog input is roughly −52 dB, as shown in Fig. 14. The accuracy of this measurement is limited by ground feedthrough in the setup.

The sampled waveform has also been examined for harmonic distortion. In this test, the SHA output is applied to a resistive divider feeding a spectrum analyzer. Fig. 15 shows the resulting spectrum with 200-MHz sampling rate and 10-MHz analog input, exhibiting a distortion less than −65 dB. Plotted in Fig. 16 is the distortion as a function of the analog input frequency while the SHA samples at 200 MHz. Note that this measurement includes the output slewing during the acquisition mode, a substantial source of nonlinearity. It is expected that if only the held values are considered, much lower distortion will be observed.

V. CONCLUSION

High-speed sample-and-hold amplifiers can employ low-voltage techniques to provide 10 b of dynamic range in a 3-V system with low power dissipation. The availability of both bipolar and MOS devices on the same substrate makes it possible to design low-voltage high-performance sampling switches and amplifiers. A sample-and-hold circuit using such topologies has been designed and fabricated in a 1-μm 20-GHz BiCMOS technology. Operating at 200 MHz, the SHA dissipates 15 mW from a 3-V supply and accommodates input/output swings of 1.5 V.

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Behzad Razavi, (S'87–M'90) for a photograph and biography, see p. 109 of the February 1995 issue of this JOURNAL.