Behzad Razavi

TSPC Logic

Since its introduction in the 1980s, true single-phase clock (TSPC) logic [1] has found widespread use in digital design. Originally proposed as a high-speed topology, the TSPC structure also consumes less power and occupies less area than other methods. In this article, we study the properties of this logic family.

Background

In the early 1980s, the design of high-speed digital CMOS circuits faced some interesting challenges. One general issue was related to clock distribution in complex chips; heavy capacitive loading and long interconnects caused both slow transitions and skew, making it especially difficult to distribute multiple, high-speed clock phases. On the other hand, it had already been recognized that dynamic logic afforded simpler, faster circuits that also occupied less area. For example, "clocked CMOS" (C^2MOS) logic, introduced in 1973 [2] and illustrated in Figure 1(a), replaced more complex latches with a four-transistor dynamic implementation. This approach, however, required two nonoverlapping clock phases so as to avoid transparency during (slow) clock transitions. That is, clock generation and distribution had to deal with not only skews but the loss of timing due to nonoverlap intervals, making single-phase clocking more attractive.

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Figure 1(b) depicts a single-phase approach. Merged with the dynamic latches, the logic is realized by NMOS or PMOS devices in alternate stages (NMOS and PMOS blocks, respectively). Here, when the clock (CK) is low, node X is precharged to V_{DD}, and when CK goes high, the N block is enabled and, according to the inputs, keeps the ONE or discharges it to ZERO. The principal issue here is that the second stage begins to evaluate while the first precharges X, a race condition that can lead to a partially charged level at Y and hence an indeterminate logical value. This issue can be resolved by delaying the second stage's clock or by placing an inverter at the output of each stage.

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Shown in Figure 2, the latter method is called "Domino" logic[3]. Note that this family performs operations using NMOS transistors, with p-type switches acting as only reset devices. Domino, however, is a *noninverting* circuit, prohibiting some logical functions [4].

The inverters in Domino logic consume power while realizing no particularly useful function. We then consider including dynamic logic within the inverters. Shown in Figure 3, the result is called "NORA" logic [5], and the cost is two clock phases.

Both Domino and NORA circuits suffer from charge sharing; for example, when CK goes high in Figure 2, C_X loses charge to C_P if M_1 is on and if V_X must remain nominally high.

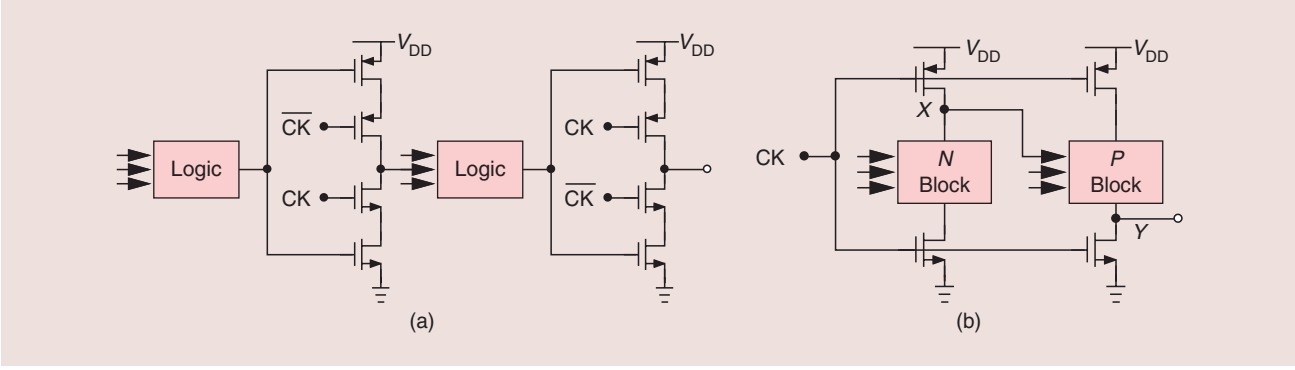

FIGURE 1: (a) C^2MOS logic and (b) an example of single-phase clocking.

The resulting degradation is less serious in Domino due to the restoration provided by the inverter. Nevertheless, the inverter does draw a static current in such a case. By contrast, C²MOS logic is free from charge sharing (why?).

The single-phase clocking of CMOS latches can be traced back to 1973, when Oguey and Vittoz reported the scheme shown in Figure 4 for a divide-by-two circuit [6]. Compared to C²MOS, this configuration employs fewer devices per branch. In 1974, Piguet filed a patent for the latch topology depicted in Figure 4(b) [7], where the clocked device in the first stage is tied to its output node.

In 1986, Christer Svensson of Linkoping University, Sweden, having read the NORA paper [5] and been intrigued by its properties, asked high Ph.D. student Ingemar Karlsson to investigate methods of improving its performance [8]. Karlsson came up with a different idea and ran some SPICE simulations that looked promising. Svensson then assigned the task to his other Ph.D. student, Jiren Yuan. Yuan modified Karlsson's topology and, in July 1986, reported his findings to Svensson. Figure 5 shows the TSPC topology drawn by Yuan in that memo [8].

TSPC gradually found its way into digital design. In 1992, Digital Equipment Corporation reported the use of TSPC in its Alpha microprocessor [9]. In 1993, Lu et al. exploited the idea in the design of a 700-MHz 24-b accumulator [10], and Rogenmoser et al. demonstrated its potential in a 1.16-GHz prescaler [11].

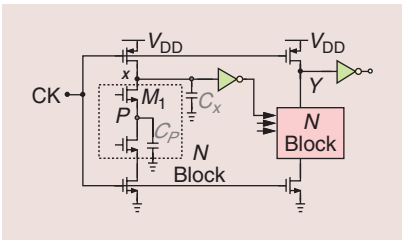

FIGURE 2: Domino logic.

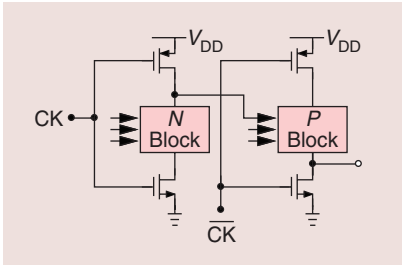

FIGURE 3: NORA logic.

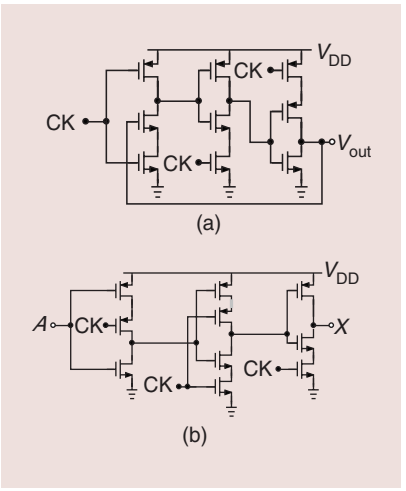

FIGURE 4: (a) A single-phase frequency divider reported by Oguey and Vittoz in 1973 and (b) a latch filed for patent by Piguet in 1974.

TSPC Principles

Let us return to the C²MOS topology of Figure 1(a) and, in the spirit of Piguet's circuit, remove one of the clocked transistors [Figure 6(a)]. When CK is high, the latch reduces to an inverter and operates properly. When CK is low, the circuit is in the store mode and retains the output state if A does not change or has only a low-to-high transition. If we precede this structure with a Domino stage that incorporates N-type logic [Figure 6(b)], we guarantee that, when CK goes low to precharge the first stage, the second stage's output remains intact. In summary, when CK is high, the first stage evaluates while the second senses, and when CK is low, the first stage is reset while the second stores.

As an application example, TSPC can be used in a divide-by-two circuit. Since the cascade shown in Figure 6(b) does not invert, we precede it with a third TSPC stage using a clocked PMOS transistor [Figure 6(c)] and tie the output to the input [1]. Note that this arrangement exhibits no charge sharing.

It is possible to further reduce the number of clocked transistors through the use of "split" outputs [1]. Beginning with the structure of Figure 6(a) and recognizing that the drain and source voltages of M_3 are roughly equal when CK is high, we follow the stage with an inverter but split the signal paths [Figure 7(a)] [1]. This latch passes A to X if CK is high and freezes X if CK is low and A has no high-to-low transitions. Since the high level at node B_2 is equal to $V_{DD} - V_{TH3}$, transistor M_5 receives less overdrive and suffers from some speed degradation.

To arrive at a master-slave flipflop, we precede the foregoing cascade with another clocked branch with split outputs, as shown in Figure 7(b). This realization incorporates only two clocked devices, serving as an attractive candidate for large register files. It is interesting to note that, even though the first stage is sensitive to input transitions when CK is high, the overall

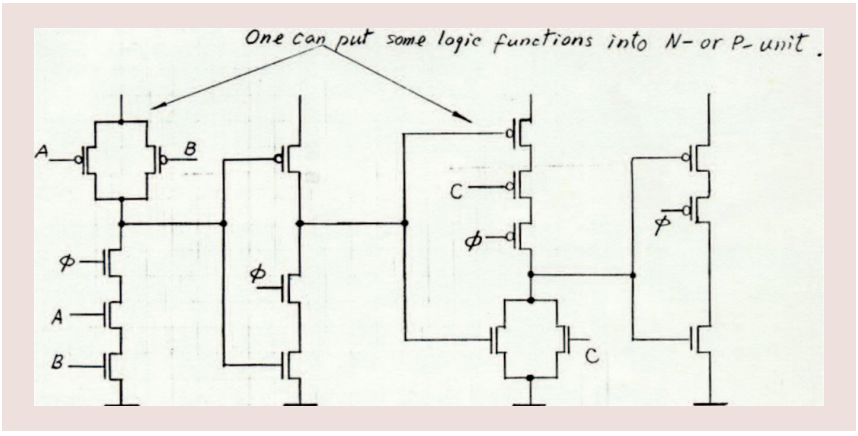

FIGURE 5: Yuan's original drawing of a TSPC circuit.

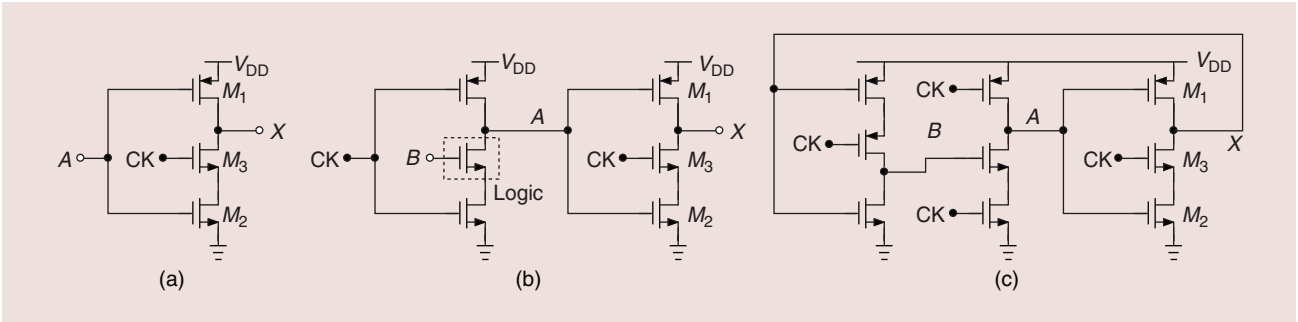

FIGURE 6: (a) A dynamic latch with a single clocked device, (b) cascaded TSPC stages, and (c) a three-stage master-slave flip-flop operating as a frequency divider.

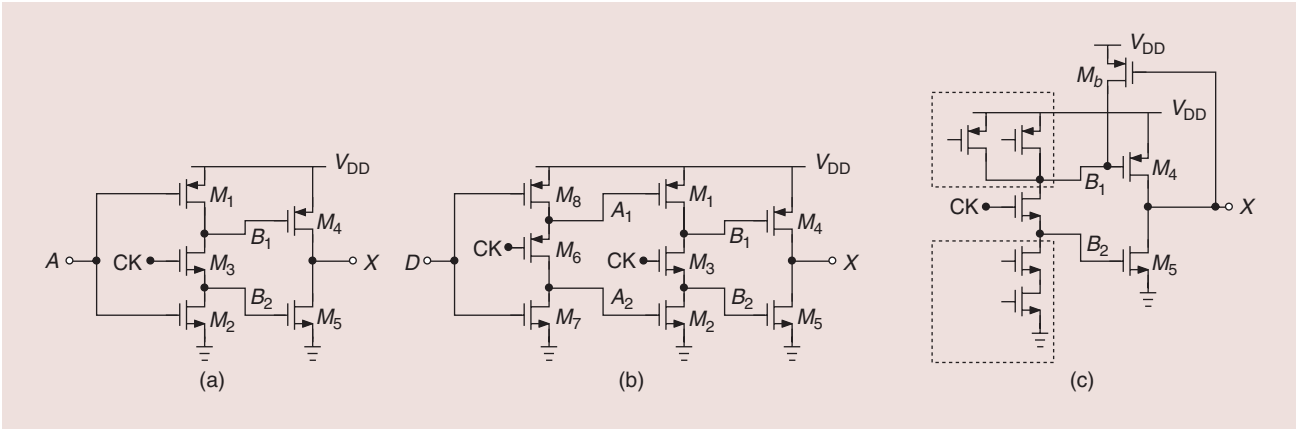

FIGURE 7: (a) A TSPC stage with split outputs, (b) a complete latch with split paths, and (c) a split-output topology incorporating random logic.

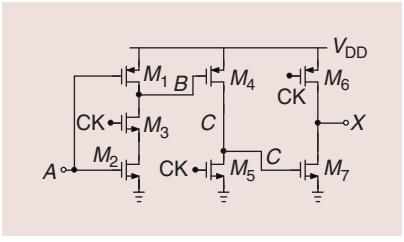

FIGURE 8: A ratioed TSPC flip-flop.

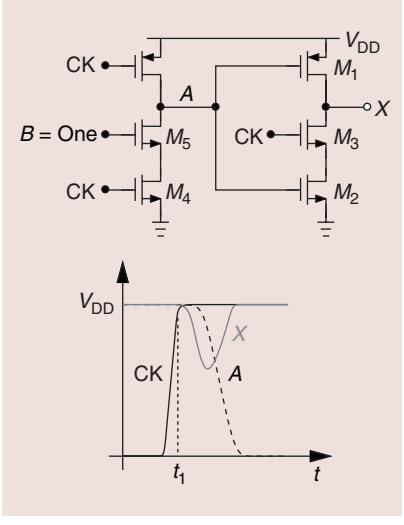

FIGURE 9: The problem of race in TSPC stages.

cascade is not. Specifically, suppose the second stage must store a ONE (so that X = ZERO). For this state to be overwritten when CK is high, A_2 must rise, which is not possible because M_6 is off. Similarly, if the second stage is storing a ZERO, only a fall in A_1 can overwrite it, which cannot occur because M_6 is off.

The TSPC latches described here can also employ random logic. For example, M_1 and M_2 in Figure 7(a) can be replaced with dual logic blocks [Figure 7(c)] [1]. In addition, a weak "bleeder," transistor M_b, can be added [9] so as to improve immunity to noise and leakage.

In addition to less hardware and power, TSPC logic also affords designs having lower phase noise. With fewer transistors and faster transitions in the signal path, TSPC techniques lead to less phase noise in circuits such as frequency dividers and phase/frequency detectors (PFDs). For example, [12] reports 6 dB of phase noise reduction if a PFD design incorporates TSPC logic rather than static CMOS gates.

As with basic static CMOS gates, the TSPC implementations studied previously are "unratioed," i.e., their NMOS and PMOS device widths need not satisfy certain ratios for the circuits to operate properly. Both classes also exhibit zero static power dissipation (except for that due to leakage). To improve the speed, we can allow some static current and construct the master-slave flip-flop shown in Figure 8 [13]. Here, a TSPC stage serves as the master and the last two stages as the slave. When CK is high, $B = \overline{A}, C$ = ZERO, and X stores a logical value. After CK goes low, $C = \overline{B}$ and $X = \overline{C} = B$. We observe that this operation requires that M_5 and M_7 be strong enough to impress a logical ZERO at their drain nodes when their corresponding PMOS device is on. The circuit draws a static current through M_5 when CK is high and through M_7 when it is low. In a typical design, we choose all of the transistor widths to be roughly the same, except for W_5, which should be two to three times greater so as to maximize the speed.

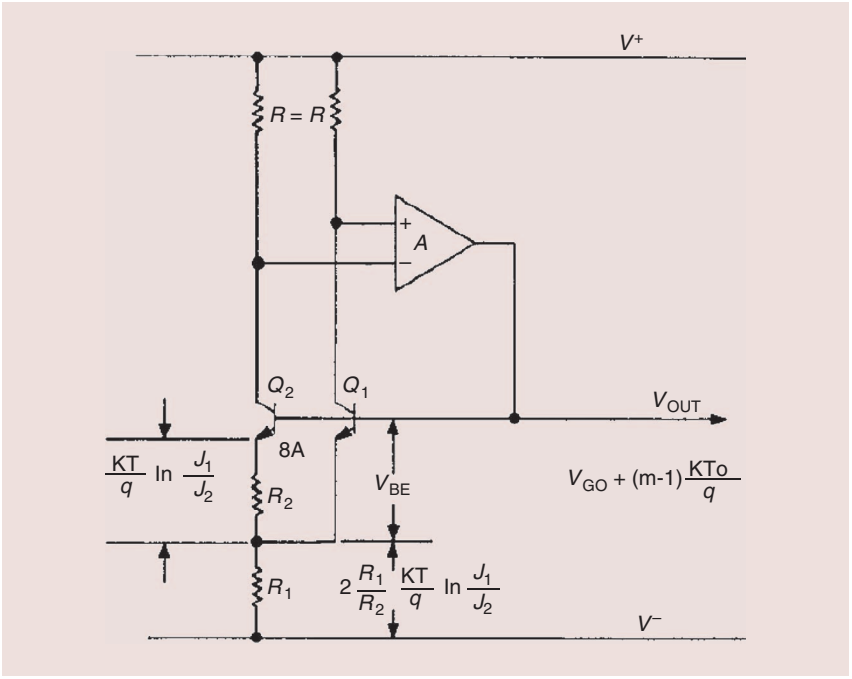

FIGURE 10: Brokaw's bandgap circuit.

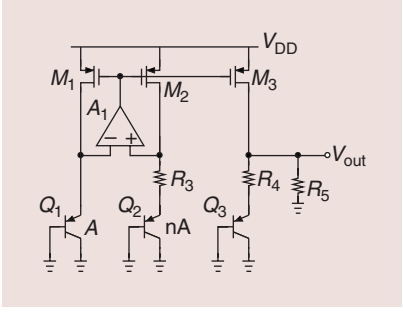

FIGURE 11: Low-voltage reference.

Design Considerations

As with other dynamic logic families, TSPC circuits fail at sufficiently low clock frequencies. Transistor leakages arising from subthreshold conduction and source and drain junctions corrupt the stored states if the clock period is excessively long. This issue typically becomes more serious at high temperatures, demanding careful simulations. As a rule of thumb, we consider these effects for clock rates below 100 MHz.

The use of a single clock phase can, in fact, create a race condition, thereby producing glitches at some nodes in TSPC circuits [11]. Consider, for example, the flip-flop shown in Figure 6(c), whose last two stages are shown in Figure 9 with the assumption that B is high and so is the state stored at X. Now suppose CK goes high, activating both M_4 and M_3. Since M_3 turns on while A is still high (around $t = t_1$), X begins to fall until A has dropped enough to turn on M_1. Consequently, X experiences a potentially large glitch that may be misinterpreted by subsequent stages. This issue can be ameliorated by making M_4 and M_5 stronger and M_2 and M_3 weaker.

Questions for the Reader

1) Can the third stage in the frequency divider of Figure 6(c) be a simple, unclocked inverter?
2) Can the frequency divider of Figure 6(c) generate an output with a 50% duty cycle?

Answers to Last Issue's Questions

1) Brokaw's bandgap, shown in Figure 10, contains both positive and negative feedback. Prove that the negative-feedback loop is stronger.

   The negative- and positive-feedback loops consist of amplifier A and transistors Q_1 and Q_2, respectively. Carrying equal currents, the two transistors have equal transconductances, but Q_2 is degenerated by R_2. As a result, the positive feedback is weaker.
2) Is the op amp offset also scaled down in the circuit of Figure 11?

   If the op amp has an input-referred offset of V_{OS}, then the output voltage assumes the form

$$V_{\text{out}} = \frac{R_5}{R_5 + R_4} \times \left[\frac{R_4}{R_3}(V_T \ln n - V_{os}) + V_{BE3} \right]. \quad (1)$$

   We note that the offset is also scaled down.

Correction

In Figure 1 of last issue's column [14], the base-emitter voltage of Q_3 should read V_{BE3}.

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