A 5.2-GHz CMOS Receiver with 62-dB Image Rejection

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***Abstract*—A 5.2-GHz CMOS receiver employs a double downconversion heterodyne architecture with a local oscillator frequency of 2.6 GHz and applies offset cancellation to the baseband amplifiers. Placing the image around the zero frequency, the receiver achieves an image rejection of 62 dB with no external components while minimizing the flicker noise upconversion in the first mixing operation. Realized in a 0.25-μm digital CMOS technology, the circuit exhibits a noise figure of 6.4 dB, an IP_3 of −15 dBm, and a voltage conversion gain of 43 dB, while draining 29 mW from a 2.5-V supply.**

***Index Terms*—Heterodyne architecture, image-reject architecture, low-noise amplifiers, mixers, offset cancellation, RF CMOS design, RF receivers.**

I. Introduction

As various wireless standards continue to populate the 80-MHz spectrum in the 2.4-GHz band, other unlicensed international bands that allow high-speed data communications become more attractive. In addition to excessive occupancy by users, the 2.4-GHz band suffers from enormous interference generated by microwave ovens, possibly creating frequent outages in wireless local area networks (WLANs) [1]. The 5-GHz band, on the other hand, provides several hundred megahertz of unlicensed spectrum and is free from microwave oven radiations.

The IEEE 802.11 committee has recently supplemented its 2.4-GHz standard with a 5-GHz version called IEEE 802.11a [2], [3]. Furthermore, the High Performance Radio Local Area Network (HIPERLAN) standard has been defined for operation in this band [4]. With data rates as high as 54 Mb/s [2], [3], these standards offer attractive solutions for data-intensive applications

This paper describes a 5.2-GHz CMOS receiver for WLAN systems. Designed in conjunction with the frequency synthesizer reported in [5] and based on a dual-conversion heterodyne architecture, the receiver incorporates a frequency planning that both simplifies the design of the synthesizer and achieves a high image rejection with no external filters. Fabricated in a digital 0.25-μm CMOS technology and operating from a 2.5-V supply, the receiver exhibits an overall noise figure of 6.4 dB, an image rejection ratio (IRR) of 62 dB, and a voltage gain of 42 dB while consuming 29 mW.

The next section of the paper reviews pertinent requirements of the IEEE and HIPERLAN standards and introduces the receiver architecture and design issues. Section III describes the design of the building blocks. Section IV summarizes the experimental results.

TABLE I
IEEE 802.11a and HIPERLAN Receiver Requirements

IEEE 802.11a (54 Mb/s)	
Modulation	**64QAM with OFDM**
Frequency Range	**5.18–5.32 GHz 5.745–5.805 GHz**
Channel Bandwidth	**20 MHz**
Sensitivity	**–65 dBm**
HIPERLAN	
Modulation	**GMSK**
Frequency Range	**5.15–5.3 GHz**
Channel Bandwidth	**23.5 MHz**
Sensitivity	**–70 dBm**

II. Standard Requirements and Receiver Architecture

The receiver architecture and frequency planning are heavily influenced by the IEEE 802.11a and HIPERLAN requirements as well as the synthesizer design constraints. Table I summarizes the receiver specifications recommended by the two standards.

The IEEE standard supports a multitude of data rates and modulation schemes, specifying 64 quadrature amplitude modulation (64QAM) and orthogonal frequency division multiplexing (OFDM) for the highest rate, 54 Mb/s, in a 20-MHz channel. To create the OFDM signal, the baseband data in the transmitter is decomposed into about 50 slower sequences, each of which is modulated on a 312.5-kHz subchannel. As a result, each subchannel carries a low data rate and is therefore less susceptible to multipath effects during propagation. The standard leaves the zeroth (center) subchannel empty to simplify dc offset removal and frequency offset corrections.

HIPERLAN employs Gaussian minimum shift keying (GMSK) modulation with a channel bandwidth of 23.5 MHz and a data rate of 23.5 Mb/s. A new version of HIPERLAN, HIPERLAN2, has also been introduced whose characteristics are close to those of IEEE 802.11a.

Fig. 1 shows the receiver architecture. The circuit performs two downconversions, each using a 2.6-GHz local oscillator (LO) frequency. As a result, the signal center frequency is translated from 5.2 GHz to an intermediate frequency (IF) of 2.6 GHz

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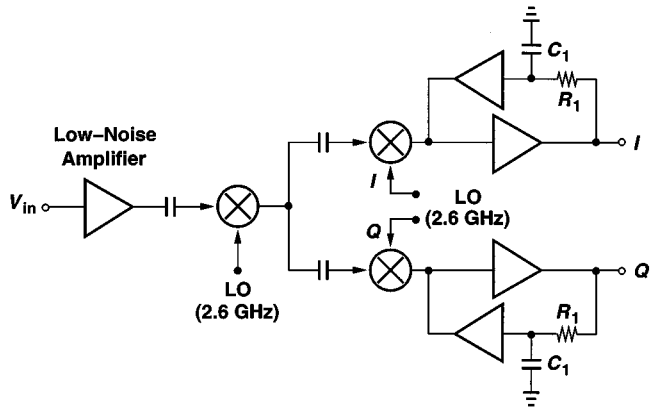

Fig. 1. Receiver architecture.

and subsequently to zero. Each baseband branch then amplifies the signal while suppressing the dc offset component. (The frequency synthesizer is not included in this prototype.)

The frequency planning chosen in this work offers several advantages over that of conventional heterodyne or image-reject architectures. First, the frequency synthesizer operates at half the input frequency, thereby imposing less stringent requirements on its oscillator and frequency divider and achieving potentially more accurately matched quadrature phases. Second, the image band is centered around the zero frequency, thus experiencing a very high suppression by the antenna and the RF front end and obviating the need for an explicit image-reject filter. In contrast to a direct-conversion receiver, the proposed architecture creates less LO leakage to the antenna in the 5-GHz band. (The leakage at 2.6 GHz is suppressed by the preselect filter and the antenna's selectivity.) Furthermore, unlike other image-reject receivers [6], [7], it does not require extremely accurate phase and gain matching.

The architecture of Fig. 1 must nonetheless deal with three issues. First, since the image lies around the zero frequency, the flicker noise in the low-noise amplifier (LNA) and the input stage of the first mixer is upconverted to the first IF, corrupting the signal (Fig. 2). It may appear that, with a total channel bandwidth of 20 MHz or larger in IEEE 802.11a and HIPERLAN, the contribution of flicker noise is negligible. However, since the MOS transistors used in the LNA and the mixer have relatively small dimensions, their flicker-noise corner frequency may be as high as several megahertz. Thus, the signal-to-noise ratio (SNR) may degrade considerably.

The second issue in the proposed architecture relates to the LO-IF feedthrough of the first mixer because this component falls in the center of the IF band and hence cannot be filtered out. If this feedthrough is large, it may substantially desensitize the second downconversion mixers.

The third issue is that the high IF prohibits channel-selection filtering at 2.6 GHz, requiring a high linearity in the IF mixers. These issues are resolved in the design of the building blocks.

III. Building Blocks

Each of the four stages in the receiver chain, namely, the LNA, the RF mixer, the IF mixers, and the baseband amplifiers, directly impact the overall noise figure, linearity, gain,

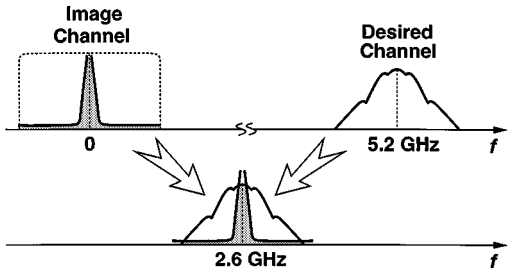

Fig. 2. Upconversion of flicker noise in the RF mixer.

and power dissipation of the receiver. The circuit therefore requires both forward (LNA-to-baseband) and backward (baseband-to-LNA) design iterations.

The 0.25-μm digital CMOS technology used in this work provides five metal layers but no high-quality resistors and capacitors. Capacitors made of metal-3/metal-4/metal-5 sandwiches exhibit a relatively small bottom-plate capacitance ($\approx$15%) but suffer from a low density ($\approx$75 aF/μm^2). These considerations influence many of the receiver design choices.

It is also important to quantify the noise-figure target for the standards considered here. IEEE 802.11a recommends a noise figure of 10 dB plus 5 dB of margin [3]. Since the preselect filter that is usually interposed between the antenna and the LNA suffers from 3 dB of loss and since the flicker noise of the baseband section degrades the SNR by as much as 1 dB, we target a noise figure of 6 dB plus 5 dB of margin.

HIPERLAN specifies a receiver sensitivity of -70 dBm for a packet error rate of 1%. With typical GMSK demodulators, such an error rate requires an SNR of about 12 dB, yielding a maximum allowable noise figure of 18.3 dB. In addition to the 4-dB degradation introduced by the preselect filter and the baseband flicker noise, HIPERLAN must also allow about 1 dB of corruption due to intersymbol interference (ISI) resulting from offset cancellation in the baseband (Section III-B). Thus, the target noise figure in this case is approximately equal to 13.3 dB.

A. RF Front End

While contributing noise and nonlinearity, the LNA and the RF mixer also determine the upconversion of flicker noise and the LO-IF feedthrough. To suppress the $1/f$ noise generated by the LNA, the amplified signal can be capacitively coupled to the input device of the mixer [Fig. 3(a)] but the $1/f$ noise of M_1 still falls in the image band. Thus, it is preferable to apply capacitive coupling between the mixer's input voltage-to-current (V/I) converter and the switching devices [Fig. 3(b)]. Here, the RF current produced by M_1 is absorbed primarily by M_2 and M_3, R_1 biases M_2 and M_3 while producing no flicker noise, and only a small fraction of the flicker noise of M_2 and M_3 is upconverted.

In Fig. 3(b), the V/I converter and the mixer draw twice as much supply current as the mixer of Fig. 3(a) does. Also, the dc compatibility of the LNA and the V/I converter is problematic. Both of these difficulties are resolved as shown in Fig. 4. The V/I converter, M_1, directly senses a level near V_{DD} and it is stacked on top of the mixer core, thus reusing the supply current. Capacitor C_2 provides a low impedance at the source of M_1 at 5 GHz. It is important to note that the stacking is possible here

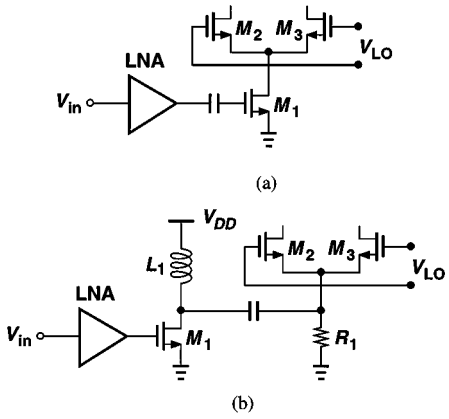

Fig. 3. Removal of flicker noise by capacitive coupling between (a) LNA and mixer, and (b) V/I converter and mixer core.

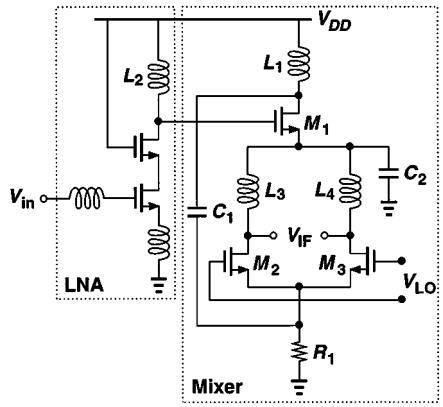

Fig. 4. Cascode LNA followed by stacked single-balanced mixer.

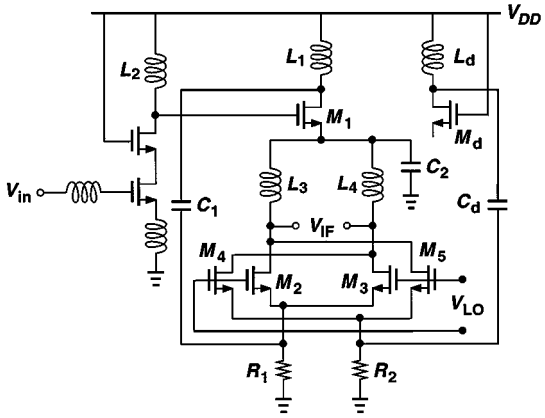

Fig. 5. Cascode LNA followed by stacked double-balanced mixer.

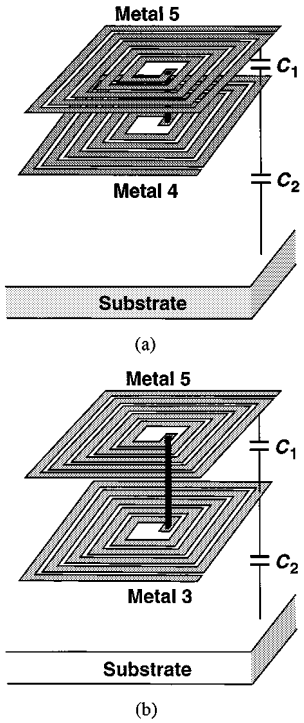

Fig. 6. Two-layer inductor made of (a) metal 5 and metal 4 layers, and (b) metal 5 and metal 3 layers.

because the IF is sufficiently high to allow the use of inductors (rather than resistors) as the loads of the RF mixer. The bias current of the stack somewhat depends on the common-mode level of $V_{\rm LO}$, but the impact on the overall receiver is negligible.

The single-balanced mixer topology of Fig. 4 produces excessive LO-IF feedthrough, desensitizing the IF mixers tremendously. It also makes the signal path more susceptible to the LO noise. The circuit is therefore modified to a double-balanced topology (Fig. 5), and the other input is connected to a dummy network (C_d,L_d, and M_d) to improve the symmetry. The second switching pair M_4-M_5 does inject additional noise to the output, but the high gain of the LNA ($\approx$18 dB) lowers the contribution to the receiver noise figure. If means of converting the single-ended antenna signal to differential (e.g., external transformers) are available, then the LNA can be realized in differential form as well [9]. In such a design, the LNA would also drive the dummy network, reducing the overall noise figure slightly.

The inductors used in the LNA and the RF mixer must exhibit a high equivalent parallel resistance, R_P, in the band of interest so as to provide a large voltage gain. Measurements on many inductors in this technology indicate that R_P increases relatively linearly with frequency across a wide range, suggesting that the quality factor *at resonance*, $Q = L\omega/R_P$, is relatively constant. This behavior is attributed to the skin effect and substrate loss. It is also observed that the Q at resonance is in the vicinity of 3 to 4 for various inductor values. Thus, to maximize R_P, it is desirable to use large values of inductance with minimum parasitic capacitance. Fig. 6(a) illustrates a typical two-layer inductor. It can be shown that the equivalent capacitance of this structure is equal to $(4C_1 + C_2)/12$ [8]. Thus, if C_1 is reduced, the self-resonance frequency $f_{\rm SR}$ rises substantially even if C_2 increases slightly. This observation leads to the structure depicted in Fig. 6(b), where the bottom spiral is moved away from the top one, reducing C_1 [8]. Applied to all of the inductors in the receiver, this modification increases the self-resonance frequency by 55%, allowing the use of 9-nH inductors in the 5-GHz signal path (L_1 and L_2) and 22-nH inductors at the 2.6-GHz IF (L_3 and L_4). Note that the modification does not change the total inductance or the substrate eddy currents significantly because the lateral dimensions are much greater than the vertical dimensions.

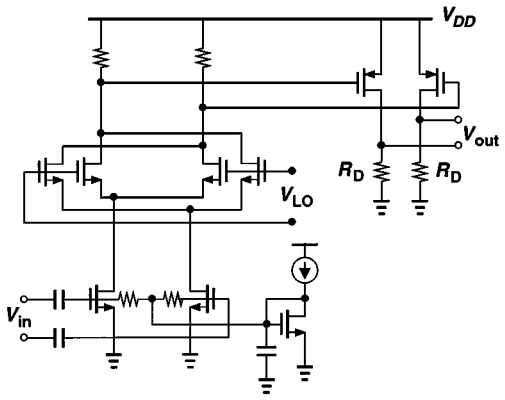

Fig. 7. IF mixer and baseband amplifier.

B. IF and Baseband Sections

Shown in Fig. 7, each of the quadrature IF mixers is realized as a double-balanced topology with grounded-source input transistors, achieving a third-intercept point (IP_3) of 1.26 V_{rms} (equivalent to $+15$ dBm in a 50-Ω system). The baseband signal is subsequently amplified by a differential pMOS stage designed for an IP_3 of 1.77 V_{rms} (equivalent to $+18$ dBm in a 50-Ω system). The high IP_3 required of the baseband amplifier limits its voltage gain to approximately 15 dB with a 2.5-V supply. (It also limits the IP_3 of the overall receiver.) This limitation can be quantified if we write for the pMOS common-source stage, $g_m = 2I_D/(V_{GS} - V_{TH})$ and $R_D = V_{RD}/I_D$, where V_{RD} denotes the dc voltage across R_D. Thus, $g_m R_D = 2V_{RD}/(V_{GS} - V_{TH})$, revealing the tradeoff between the voltage gain ($g_m R_D$), voltage head room (V_{RD}), and linearity ($V_{GS} - V_{TH}$).

The total voltage gain of the receiver exceeds 40 dB, requiring high linearity in subsequent baseband filters but allowing heavy source degeneration before the baseband noise becomes significant.

The second downconversion mixing operation shares some issues with direct-conversion receivers. In particular, the self-mixing of the LO in the IF mixers and the LO-IF feedthrough in the RF mixer produce tens of millivolts of dc offsets in the baseband, possibly saturating the baseband amplifier and other subsequent stages (or at least degrading their linearity markedly). For this reason, a method of suppressing the offset is necessary.

Since offset removal entails high-pass filtering the baseband signal, it is important to examine the consequences of such an operation for the modulation schemes of interest. In IEEE 802.11a, the center subchannel is unused, providing an empty spectrum of ± 156.25 kHz after translation to the baseband (Fig. 8). Thus, if the corner frequency of the high-pass filter (HPF), f_C, falls below this value, then the spectrum of the subchannels carrying information remains intact. A corner frequency of 156 kHz requires resistor and capacitor values on the order of a few hundred kilohms and a few picofarads, respectively—relatively practical values for integration.

An important concern in high-pass filtering is the effect of frequency offsets. Since IEEE 802.11a allows a few hundred kilohertz of offset (resulting from crystal frequency inaccuracies in transmitters and receivers), the HPF may in fact suppress a main subchannel rather than the empty one. This difficulty can be resolved by automatic frequency control (AFC), i.e., by deriving an error signal from the digital baseband processor proportional to the frequency offset and applying it to the crystal oscillator that generates the reference for the frequency synthesizer.

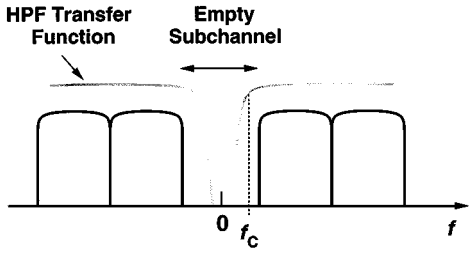

Fig. 8. DC offset removal in IEEE 802.11a.

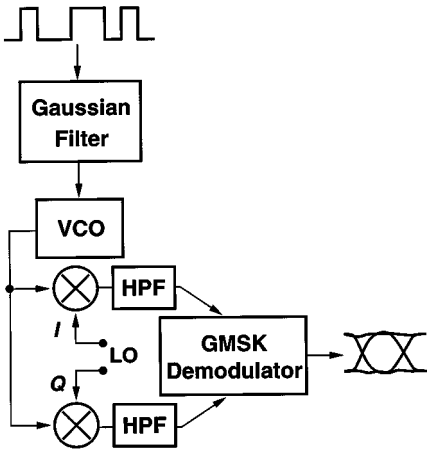

Fig. 9. Setup for studying the effect of high-pass filtering on GMSK signals.

The effect of high-pass filtering on GMSK signals (in HIPERLAN) is less straightforward. Removal of part of the spectrum leads to ISI, and the resulting degradation can be studied with the aid of the simulation setup shown in Fig. 9. Here, a random baseband bit stream is applied to a Gaussian filter and a voltage-controlled oscillator (VCO), thereby generating a GMSK signal. The output of the VCO is then decomposed into quadrature phases, translated to the baseband, high-pass filtered, and applied to a baseband GMSK demodulator. The quality of the output eye diagram can thus be studied as different corner frequencies are chosen for the HPFs.

Fig. 10 depicts the simulated eye diagrams for three values of f_C in terms of the bit rate, r_b. (For simplicity, the Gaussian filter is excluded in this simulation.) We note that for $f_C = 0.001 r_b$, the eye is almost identical to that for $f_C = 0$. If f_C rises to $0.01 r_b$, however, the eye experiences some closure. The HPF corner frequency must therefore fall between $0.001 r_b$ and $0.01 r_b$ so as to maintain signal integrity.

Fig. 11 illustrates two continuous-time offset cancellation techniques. In Fig. 11(a), the offset is removed completely, but the coupling capacitors cannot be implemented as MOSFETs unless they sustain a large voltage, a condition that limits the choice of the common-mode levels. In the digital CMOS technology used here, linear capacitors can be implemented as a sandwich structure consisting of all metal layers and the

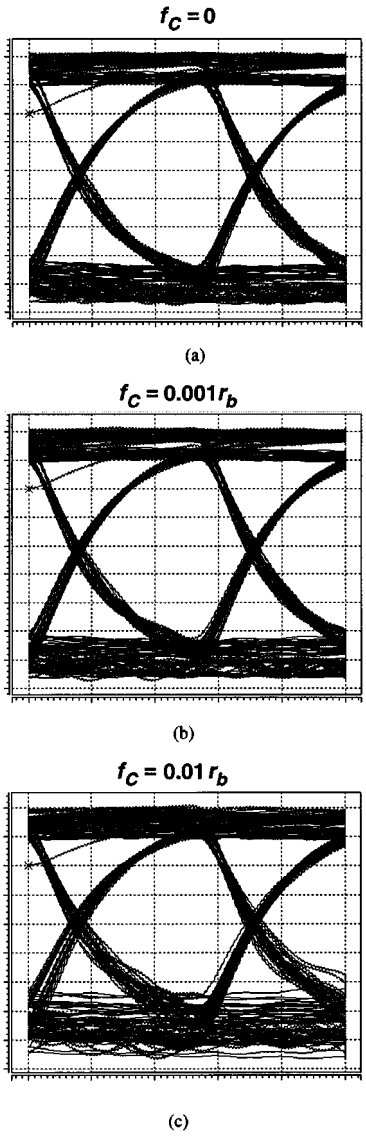

Fig. 10. Eye diagrams for three values of HPF corner frequency.

polysilicon layer. The density, however, is only 200 aF/μm^2, translating to a very large area for the four capacitors necessary in the differential I and Q paths. By comparison, MOSFETs provide a density 30 times higher. Also, the parasitic capacitance of the resistors directly attenuates the signal.

In Fig. 11(b), the offset is partially removed by negative feedback around the baseband amplifier. The critical advantage of this approach over that in Fig. 11(a) is that it employs only grounded capacitors and can therefore utilize MOSFETs. A 10-pF capacitor in this case consumes an area of 41 μm $\times$ 41 μm, whereas it would necessitate an area of 225 μm $\times$ 225 μm if realized as a sandwich structure. Another advantage is that the parasitic capacitance of the resistors does not lower the gain at the frequencies of interest.

With a bit rate of 23.5 Mb/s in HIPERLAN, the resistors in Fig. 11(a) must exceed 700 kΩ if each capacitor is limited to about 10 pF. The loop gain of the offset cancellation path in Fig. 11(b) further raises the minimum tolerable value to roughly 3 MΩ. Such a high value demands a very large area even if the resistors are made of n-well.

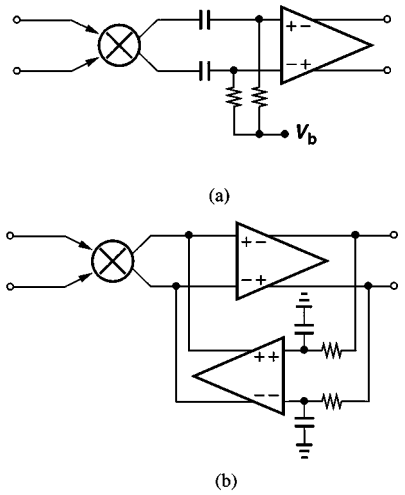

Fig. 11. Offset cancellation by (a) capacitive coupling, and (b) negative feedback.

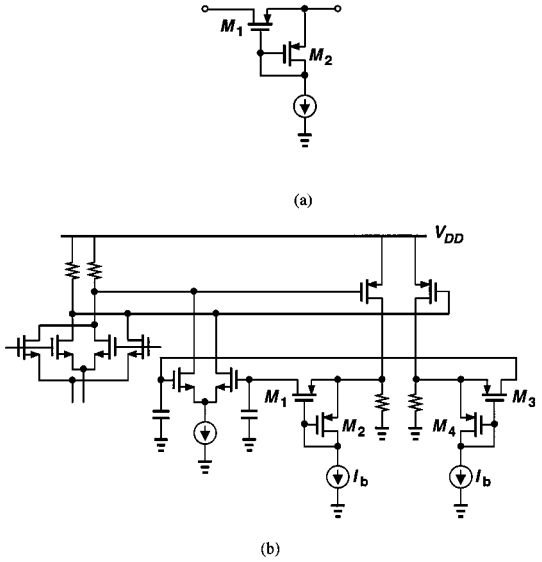

Fig. 12. (a) Floating resistor with controlled gate–source voltage. (b) Offset cancellation in the baseband section.

A long MOSFET with a well-defined gate–source overdrive voltage can act as a large floating resistor. Shown in Fig. 12(a) is a MOS device, M_1, operating in deep triode region with its gate–source voltage established by a diode-connected transistor, M_2. Here, $R_{\rm on1}$ tracks $1/g_{m2}$ if the overdrive voltage is large enough to overwhelm the threshold voltage mismatch between M_1 and M_2. The overall implementation of the dc feedback loop is illustrated in Fig. 12(b). With $(W/L)_{1,3} = 1\ \mu$m$/200\ \mu$m, $(W/L)_{2,4} = 1\ \mu$m$/10\ \mu$m, and $I_b \approx 1\ \mu$A, the corner frequency of the notch filter is on the order of a few kilohertz.

IV. Experimental Results

The receiver has been fabricated in a 0.25-μm CMOS technology and tested with a 2.5-V supply. Fig. 13 shows a photograph of the die, which measures 600 μm $\times$ 700 μm.

Table II summarizes the measured performance of the prototype. The image-rejection ratio is evaluated by applying a 12-MHz input (the highest frequency in the image channel of

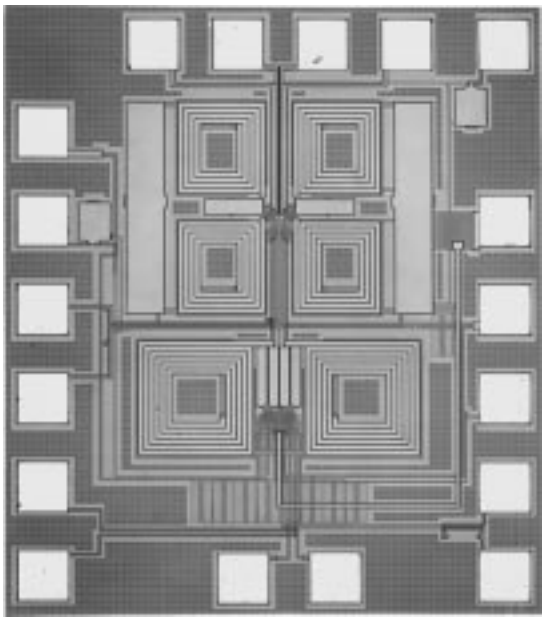

Fig. 13. Die photograph.

TABLE II
RECEIVER MEASURED PERFORMANCE

Center Frequency	**5.2 GHz**
Noise Figure	**6.4 dB**
Input IP_3	**–15 dBm**
1–dB Compression Point	**–26.5 dBm**
Image Rejection	**62 dB**
Voltage Gain	**43 dB**
LO Leakage to Antenna	
@ 5.2 GHz	**–64 dBm**
@ 2.6 GHz	**–57 dBm**
Output Offset Voltage	**25 mV**
Power Dissipation	
LNA	**8.75 mW**
RF Mixer	**5 mW**
IF Mixers	**10 mW**
Baseband Section	**5.25 mW**
Total	**29 mW**
Supply Voltage	**2.5 V**
Technology	**0.25–μm CMOS**

Fig. 2) and measuring the downconverted baseband component. The rejection is limited to 62 dB by signal leakage through the substrate and the test board, but, with another several tens of decibels of suppression provided by the antenna, the overall IRR is expected to reach 100 dB. While the 1-dB compression point may not be sufficient for some WLAN systems, it can be easily traded with the noise figure, which is several decibels lower than required.

The offset cancellation loop reduces the output offset by about one order of magnitude. It is expected that subsequent stages would incorporate a similar technique to limit the offset. The measured corner frequency of the notch is equal to 1.5 kHz.

Both the LO frequency and its second harmonic (generated at the sources of M_1–M_4 in Fig. 5) leak to the RF input. The cascode LNA suppresses the 5.2-GHz leakage to -64 dBm. The 2.6-GHz leakage arises primarily from the traces on the board, but it would be suppressed further by the selectivity of the antenna. Both leakage levels are well below typical WLAN limits.

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Dr. Razavi received the Beatrice Winner Award for Editorial Excellence at the 1994 International Solid-State Circuits Conference, the Best Paper Award at the 1994 European Solid-State Circuits Conference, the Best Panel Award at the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, and the Best Paper Award at the IEEE Custom Integrated Circuits Conference in 1998. He has also served as Guest Editor and Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS and *International Journal of High Speed Electronics*.