A Millimeter-Wave Circuit Technique

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***Abstract*—An inductive feedback technique increases the speed of resonant circuits by 62%, allowing operation near the f_T of transistors. The technique leads to a fundamental oscillator operating at 128 GHz with a power dissipation of 9 mW and a phase noise of −105 dBc/Hz at 10-MHz offset. A divide-by-two circuit based on the idea and incorporating a sampling mixer achieves a maximum speed of 125 GHz while consuming 10.5 mW. The prototypes have been fabricated in 90-nm CMOS technology.**

***Index Terms*—High-speed frequency dividers, inductive feedback, *LC* oscillators, Miller divider, millimeter-wave amplifiers, millimeter-wave oscillators, passive mixers.**

I. Introduction

THE growing interest in millimeter-wave transceivers for consumer, radar, and imaging applications has motivated work on various CMOS building blocks operating at 60 GHz and beyond [1]–[5]. The maximum speed of such circuits is typically limited by the quality factor, Q, of inductors or transmission lines: a higher Q would permit the use of a smaller inductance to resonate with transistor capacitances, thus achieving a higher speed. This limitation proves serious as skin effect and substrate loss in CMOS technology prohibit linear scaling of the Q with frequency, leading to values that tend to saturate for frequencies above 60 GHz. For example, [6] reports a Q of 12 for 180-pH inductors at 60 GHz, and [7] a Q of 17 for 400-pH inductors at 50 GHz.

This paper introduces an inductive feedback technique that substantially raises the maximum speed of resonant circuits, allowing operation near the self-resonance frequency of the inductors and the f_T of the transistors. The potential of the proposed technique is demonstrated in oscillators and frequency dividers that achieve the highest speeds reported in 90-nm CMOS technology. Section II describes the basic circuit and formulates its behavior. Sections III and IV apply the idea to the design of oscillators and frequency dividers, respectively. Section V presents the experimental results.

II. Basic Idea

Consider the passive fourth-order *LC* circuit shown in Fig. 1(a), where all of the components are ideal. The transfer function from the input current to the output voltage can be expressed as

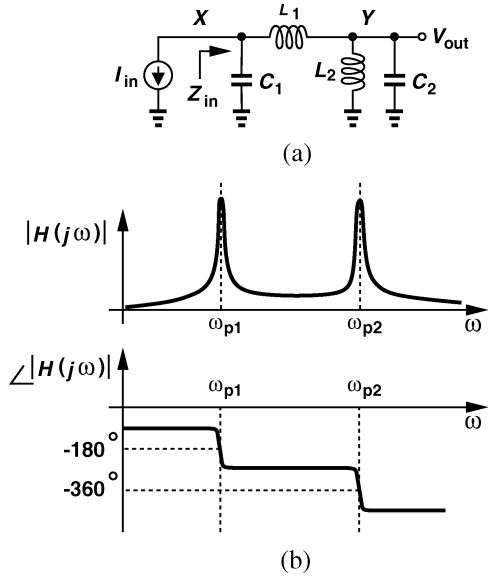

Fig. 1. (a) Fourth-order passive network. (b) Frequency response of the circuit.

$$H(s) = \frac{V_{\text{out}}}{I_{\text{in}}}(s) = \frac{-L_2 s}{L_1 L_2 C_1 C_2 s^4 + [(L_1+L_2)C_1 + L_2 C_2]\, s^2 + 1}. \quad (1)$$

The circuit contains four complex conjugate poles given by

$$\omega_{p1-p4}^2 = -\frac{1}{2(L_1 \| L_2)C_2} - \frac{1}{2L_1 C_1} \pm \sqrt{\frac{1}{4(L_1\|L_2)^2 C_2^2} + \frac{L_2 - L_1}{2L_1^2 L_2 C_1 C_2} + \frac{1}{4L_1^2 C_1^2}}. \quad (2)$$

To gain more insight, let us consider the special case $L_1 = L_2 = L$ and $C_1 = C_2 = C$. It follows that

$$\omega_{p1,p1'} = \pm j\sqrt{\frac{3-\sqrt{5}}{2LC}} \approx \pm j\frac{0.62}{\sqrt{LC}} \quad (3)$$

$$\omega_{p2,p2'} = \pm j\sqrt{\frac{3+\sqrt{5}}{2LC}} \approx \pm j\frac{1.62}{\sqrt{LC}}. \quad (4)$$

Note that the magnitude of ω_{p2} is 62% greater than the resonance frequency of second-order tanks, a critical advantage of the proposed technique.[1]

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[1]As pointed out by Associate Editor Derek Shaeffer and one of the reviewers, the factor $\sqrt{(3+\sqrt{5})/2} = (\sqrt{5}+1)/2$ is the Golden Ratio. The network may have certain recursive properties.

Fig. 1(b) sketches the magnitude and phase response of the circuit with nearly ideal components. The phase begins at -90° at low frequencies, crosses -180° at ω_{p1} and -360° at ω_{p2}, and asymptotically approaches -450°. As explained in Section III, the distinct phase shifts at ω_{p1} and ω_{p2} allow oscillation at only one of the two frequencies depending on the polarity of the feedback.

For subsequent derivations, the voltage gain from X to Y in Fig. 1(a) is necessary. To this end, we first obtain the input impedance:

$$Z_{\text{in}} = \frac{s(L_1L_2C_2s^2 + L_1 + L_2)}{L_1L_2C_1C_2s^4 + [(L_1 + L_2)C_1 + L_2C_2]\, s^2 + 1}. \quad (5)$$

In addition to the zero at the origin introduced by $L_1 + L_2$, the input impedance exhibits two imaginary zeros given by $\pm j/\sqrt{(L_1||L_2)C_2}$ because at each zero frequency, $Z_{\text{in}} = 0$, $V_X = 0$, and hence the circuit reduces to L_1, L_2, and C_2. The voltage transfer function from X to Y is therefore equal to

$$\frac{V_Y}{V_X}(s) = \frac{H(s)I_{\text{in}}}{-Z_{\text{in}}I_{\text{in}}} \quad (6)$$

$$= \frac{L_2}{L_1L_2C_2s^2 + L_1 + L_2}. \quad (7)$$

If $L_1 = L_2$ and $C_1 = C_2$, then

$$\frac{V_Y}{V_X} = -\frac{\sqrt{5}+1}{2} \text{ at } \omega_{p2}. \quad (8)$$

That is, V_Y and V_X bear a ratio of about 1.62 and are 180° out of phase at the second pole frequency.

The above analysis has assumed ideal components. In order to include the loss of the inductors and eventually arrive at the proposed circuit technique, we first construct a phasor diagram of the voltages and currents at an operation frequency equal to ω_{p2}. As depicted in Fig. 2(a), we assume an orientation for V_Y $(= V_{\text{out}})$ and note that the current flowing through C_2, denoted by I_4, must lead V_Y by 90°. Since C_2 and L_2 appear in parallel, their currents must remain 180° out of phase. Moreover, since $|\omega_{p2}|$ $(\approx 1.62/\sqrt{LC})$ is greater than the resonance frequency of L_2 and C_2, the inductive current is smaller: $|I_3| < |I_4|$. For I_2 to satisfy KCL at node Y, it must point upward. Also, since the input impedance and hence V_X approach infinity at ω_{p2}, we have $|I_1| \gg |I_{\text{in}}|$, i.e., $I_1 \approx I_2$. Lastly, V_X must lead I_1 by 90°.

We now include the loss of L_2 as a constant parallel resistance R_2 [Fig. 2(b)], a reasonable model for a narrow frequency range.[2] The current through R_2, denoted by I_5, is aligned with V_Y but has no phasor counterpart in the diagram of Fig. 2(a). Consequently, the I_4, I_3, and I_2 phasors must rotate clockwise to reach a zero vector sum along with I_5.

Let us now make a key observation. Another possibility for the above current phasors to satisfy KCL at node Y is that a new device is introduced that draws a current equal to $-I_5$ from this node. Such a current must therefore be proportional to $-V_Y$ and hence proportional to V_X. Illustrated in Fig. 3(a), the idea is to insert a transistor so as to ensure $g_mV_X + V_Y/R_2 = 0$. If this relationship holds, then R_2 plays no role in the frequency response, the circuit reduces to the idealized topology of Fig. 1(a), and $V_Y/V_X = -(\sqrt{5}+1)/2$. Thus, the required value of g_m is equal to $(\sqrt{5}+1)/(2R_2)$.

The loss of L_1 can be modeled by a resistance, R_1, tied between nodes X and Y. The analysis is less straightforward but an observation can lead to a relatively accurate value for the required g_m that compensates both losses. Consider the circuit

[2]The losses of capacitances can also be absorbed by R_2.

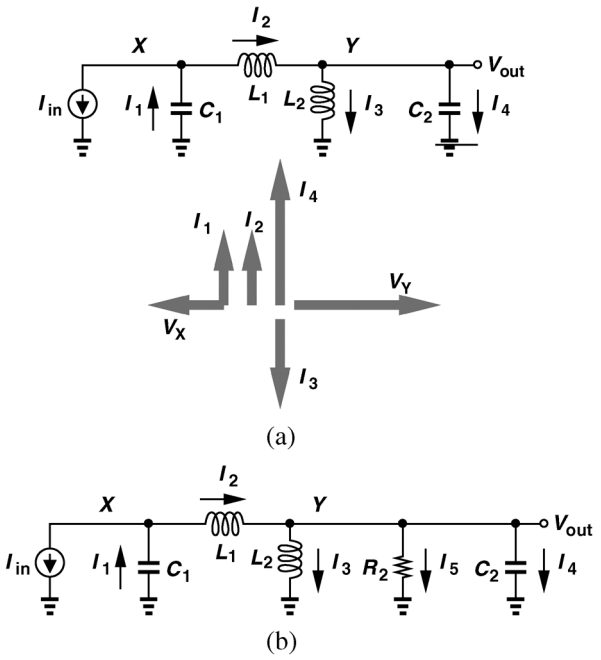


Fig. 2. (a) Phasor diagram of currents and voltages of the circuit. (b) Effect of loss of L_2.

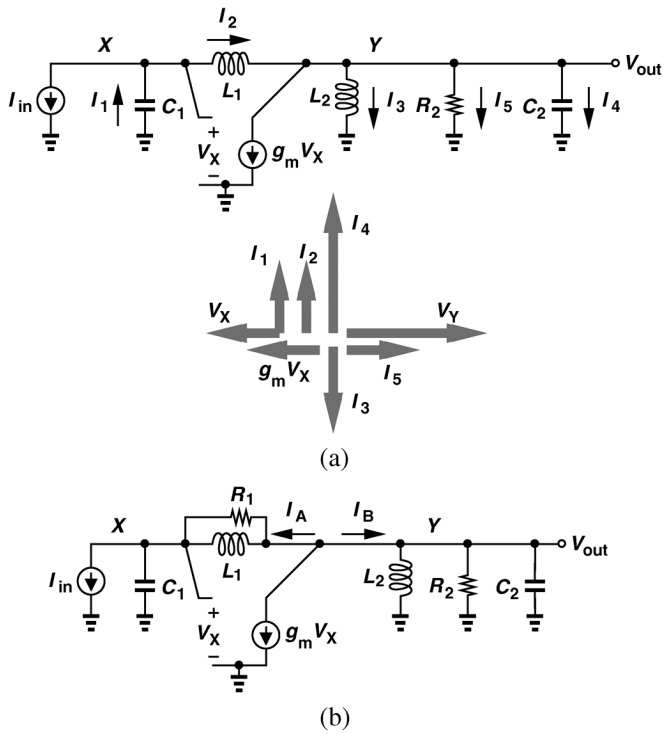


Fig. 3. (a) Cancellation of loss of L_2 by means of a transistor. (b) Circuit including the loss of L_1.

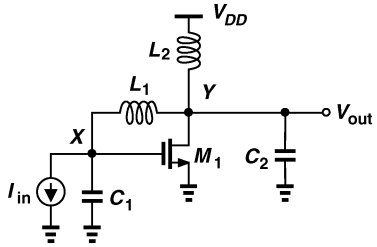


Fig. 4. Transimpedance amplifier based on proposed technique.

shown in Fig. 3(b) and suppose that proper choice of g_m allows V_X and V_Y to approach infinity at ω_{p2}. Since the current flowing through C_1 is much greater than $I_{\rm in}$, the effect of the input current can be neglected in calculating V_X (from V_Y) and applying KCL at the output node. Assuming $L_1 = L_2 = L$, $C_1 = C_2 = C$, and $R_1 = R_2 = R$ for the remainder of the paper, we write this KCL as

$$\frac{g_m(R+Ls)}{RL^2C^2s^2+R}V_Y + \frac{Cs(R+Ls)}{RL^2C^2s^2+R}V_Y + \frac{RLCs^2+Ls+R}{RLs}V_Y \approx 0. \quad (9)$$

Here, the first term represents g_mV_X and the last two terms, I_A and I_B, respectively. Factoring V_Y out and setting the remaining expression to zero, defining $R/(L\omega) = \mathrm{Q}$, and assuming $\omega = \omega_{p2}$, we obtain

$$g_m = \frac{j\mathrm{Q}\frac{3\sqrt{5}+5}{2}+1}{j\mathrm{Q}-1}\cdot\frac{1}{R}. \quad (10)$$

If $|j\mathrm{Q}| \gg 1$, then

$$g_m \approx \frac{3\sqrt{5}+5}{2}\cdot\frac{1}{R} \quad (11)$$

$$\approx \frac{5.85}{R}. \quad (12)$$

Simulations confirm the validity of this result.

The foregoing development leads to the transimpedance amplifier topology depicted in Fig. 4. The above choice of g_m places the circuit at the edge of oscillation without an input current source. It is therefore desirable to compute the open-loop Q of the circuit in terms of the Q of the constituent inductors. The open-loop Q of the circuit is defined as $(\omega_{p2}/2)d\phi/d\omega$, where ϕ denotes the phase of $H(j\omega)$, so as to signify how much the phase of the oscillator resists change due to injected noise [8]. As derived in Appendix I,

$$\frac{\omega_{p2}}{2}\frac{d\phi}{d\omega} \approx \mathrm{Q} + \frac{\mathrm{Q}}{2(1+\mathrm{Q}^2)} \quad (13)$$

where $\mathrm{Q} = R/(L\omega)$ represents the Q of each inductor. Thus, for relatively high Q's, the open-loop Q of the network is approximately equal to the Q of the inductors.

The gate-drain capacitance of M_1 and the coupling capacitance between the two terminals of L_1 introduce some capacitance between nodes X and Y. To the first order, this component can be decomposed using Miller's theorem, with the resulting capacitances absorbed by C_1 and C_2. A more accurate analysis requires simulations.

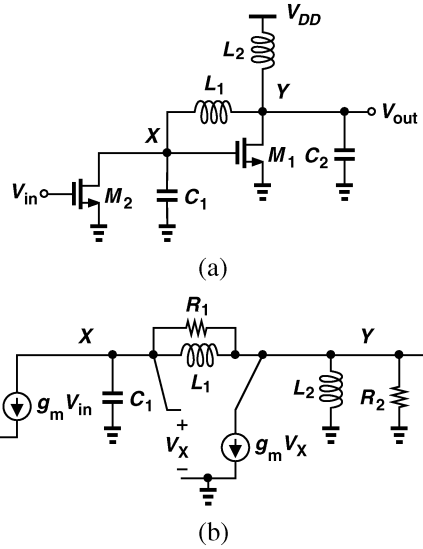


Fig. 5. (a) Voltage amplifier based on proposed technique. (b) Equivalent circuit.

If the input current source in Fig. 4 is replaced with a transistor to obtain a voltage amplifier, the circuit resembles a Cherry–Hooper topology [9] with resistors converted to inductors. However, the foregoing analysis of the frequency response and the role of M_1 reveals a number of new and unique properties of the proposed circuit that do not exist in the Cherry–Hooper amplifier. Specifically, 1) the resonance and sharp phase slope at ω_{p2} indicate potential for low-noise oscillator design; 2) the magnitude of ω_{p2} is considerably higher than speeds provided by second-order *LC* circuits; 3) the use of inductors rather than resistors allows operation from low supply voltages; 4) though not utilized in this work, mutual coupling between L_1 and L_2 in Fig. 4 can be exploited to modify and tailor the frequency response.

III. Oscillator Design

A. Proposed Oscillator

The choice of g_m according to (11) places the circuit of Fig. 4 at the edge of oscillation. Alternatively, the input current source in Fig. 4 can be realized by a second transistor [Fig. 5(a)] so as to achieve a unity loop gain with smaller MOSFETs. With the aid of the equivalent circuit shown in Fig. 5(b), we seek the necessary values of g_{m1} and g_{m2} to ensure $V_{\rm out}/V_{\rm in} = 1$. Note that C_2 includes the capacitive loading due to M_2 in an oscillator loop.

If $g_{m1} = g_{m2} = g_m$, then

$$\frac{V_{\rm out}}{V_{\rm in}}(s) = \frac{g_mLs\left(g_mLs - \frac{Ls}{R} - 1\right)}{L^2C^2s^4 + 3\frac{L^2C}{R}s^3 + \left(3LC + \frac{L^2}{R^2} + g_m\frac{L^2}{R}\right)s^2 + \left(2\frac{L}{R} + g_mL\right)s + 1}. \quad (14)$$

Equating the transfer function to unity, multiplying both sides by the denominator, grouping the real parts and the imaginary

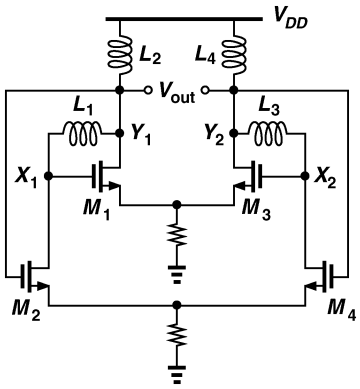


Fig. 6. Oscillator based on proposed technique.

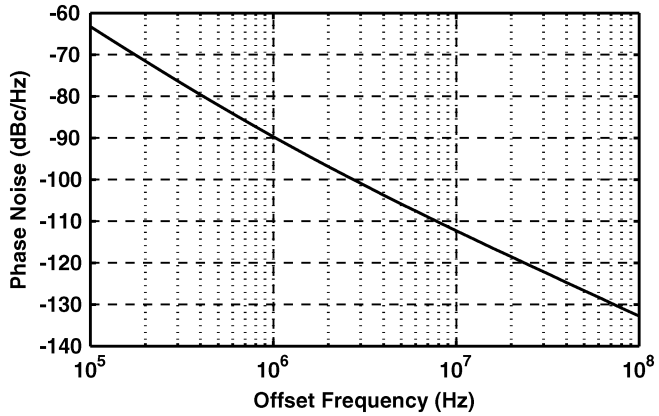


Fig. 7. Simulated phase noise of oscillator.

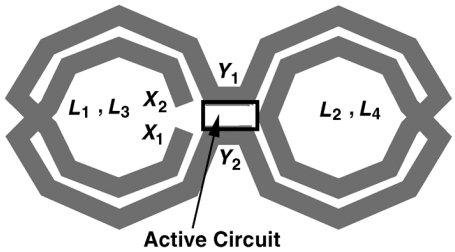


Fig. 8. Inductor geometries for oscillator.

parts, and setting the total imaginary part to zero, we obtain the oscillation frequency as

$$\omega_{\rm osc}^2 = \frac{2+2g_mR}{3LC}. \tag{15}$$

Next, we set the total real part to zero and use (15) to compute the required value of g_m. To simplify the final result, we assume $g_m^2R_2 - 2g_mR - 1 \ll 3R^2C/L(= 3R^2C^2\omega^2)$ because $3R^2C^2\omega^2$ reduces to $(3/2)(3+\sqrt{5})[R^2/(L^2\omega^2)] \approx 3.92\text{Q}^2$ in the vicinity of ω_{p2}. It follows that

$$g_m = \frac{5+3\sqrt{5}}{4} \cdot \frac{1}{R} \tag{16}$$

which is half of that dictated by (11). Each transistor in Fig. 5(a) need therefore be half as wide and consume half as much bias current as M_1 in Fig. 4.

The sharp phase slope at ω_{p2} suggests the possibility of oscillator design using the proposed topology. Fig. 6 shows a differential oscillator derived from this concept. Note that the polarity of feedback is chosen to permit oscillation at ω_{p2} and prohibit the mode at ω_{p1}. Simulations suggest that identical inductors and identical transistors yield the maximum frequency of oscillation.

Three versions of the circuit have been designed with $(W/L)_{1-4} = 8\ \mu\text{m}/0.1\ \mu\text{m}$, a bias current of 1.9 mA per transistor, and different inductor values ($L_2 + L_4 = 430$ pH, 270 pH, 200 pH) to provide prototypes in the range of 80 to 130 GHz. Fig. 7 plots the simulated phase noise at 130 GHz for an inductor Q of 10. The phase noise reaches -112 dBc/Hz at 10-MHz offset. The frequency can be varied by tying varactors to nodes X_1, X_2, Y_1, and Y_2, equivalently tuning C_1 and C_2 in Fig. 5(a) simultaneously. Simulation of the start-up condition in the 130-GHz oscillator indicates a minimum transistor g_m that is about 30% higher than that predicted by (16). This discrepancy arises from neglecting the gate-drain capacitance of the transistors and the coupling capacitance of the inductors in hand calculations.

The use of several inductors in the oscillator of Fig. 6 leads to difficulties in the layout. While L_2 and L_4 can be realized as a single symmetric structure, the *floating* elements L_1 and L_3 would require long interconnects (longer than the radius of one inductor) at either X_1 and X_2 or Y_1 and Y_2. Fortunately, this issue can be resolved by the layout style illustrated in Fig. 8, where L_1 and L_3 also form a symmetric inductor that is broken at its point of symmetry so as to produce nodes X_1 and X_2. The four critical nodes are thus placed in close proximity of one another.[3]

One may wonder if the mutual coupling between the L_1 and L_3 spirals in Fig. 8 alters the behavior of the oscillator. However, we note that, in the presence of differential signals, the mutual coupling simply raises the value of each inductance—in the same manner that it increases the net values of L_2 and L_4. In other words, differential operation results in equal net values for all four inductors.

B. Comparison With Cross-Coupled Oscillator

Comparison of the proposed oscillator with the conventional cross-coupled topology is not straightforward. Frequency of operation, inductor design, transistor dimensions, output swings, power dissipation, effect of loading by a buffer stage, and phase noise necessitate comparisons along several axes. We perform two comparisons here that portray a relatively fair picture of the two circuits.

The first comparison reveals the speed advantage of the proposed oscillator. We assume the inductor design and the buffer stage are given and determine the *minimum* transistor width in each oscillator necessary for start-up and hence the maximum oscillation frequency that it can achieve. (The bias currents are chosen so as to saturate the transconductance of the transistors, i.e., create a large overdrive voltage.) Fig. 9(a) plots the maximum oscillation frequency as a function of inductor Q. Note

[3]Coupling among these nodes through the substrate is negligible due to differential operation.

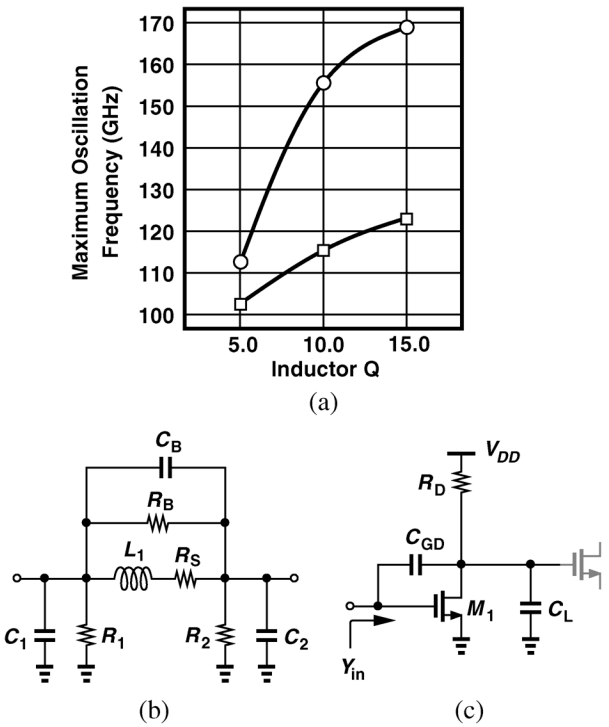


Fig. 9. (a) Maximum achievable frequency for the proposed oscillator (circles) and cross-coupled oscillator (squares). (b) Inductor model used in simulations. (c) Effect of loading of buffer stage.

that the frequencies obtained here correspond to circuits that are at the edge of oscillation with small output swings. In practice, the transistors must be wider to allow nearly complete steering of the tail currents, thus yielding lower oscillation frequencies. A relatively broadband inductor model (with series and parallel resistances) is used to maintain the same Q at each frequency pair. The inductance value is 100 pH and the parasitics are modeled as shown in Fig. 9(b).

It is important to understand the effect of loading of buffers at these frequencies and how the two oscillators react to this effect. Consider the half-circuit equivalent of a differential buffer, Fig. 9(c), which itself drives other stages, thus incurring a load capacitance of C_L. The real part of the input admittance can be expressed as

$$\mathrm{Re}\{Y_{\mathrm{in}}\} = \frac{[(1+g_mR_D)C_{GD}+g_mR_DC_L]\,R_DC_{GD}\omega^2}{1+R_D^2(C_{GD}+C_L)^2\omega^2}. \tag{17}$$

For example, if $g_mR_D = 2$, $R_D = 100\ \Omega$, $C_{GD} = 1.5$ fF, $C_L = 10$ fF, and $\omega = 2\pi \times (130\ \mathrm{GHz})$, then $\mathrm{Re}\{Y_{\mathrm{in}}\} = (768\ \Omega)^{-1}$. This low level of resistance is quite comparable with the parallel equivalent resistance of inductors [R_1 and R_2 in Fig. 5(b)], thereby reducing the Q considerably.[4] By virtue of negative feedback, the proposed oscillator proves more tolerant of capacitive and resistive loading than the cross-coupled topology does.

It is also interesting to note that a cross-coupled oscillator employing gate-drain capacitance neutralization to approach f_{max} of the transistors would still fall short of the values afforded by the proposed topology. For example, the 8-μm transistors used in this design have a C_{GD} of about 1 fF, requiring a neutralization inductance as large as 630 pH even at 200 GHz. Such an inductance suffers from an f_{SR} below 100 GHz. (The work in [6] reports a self-resonance frequency of 110 GHz for a 422-pH inductor.)

[4]If R_D is replaced with an inductor that resonates with C_L, then we can set $C_L = 0$ in (17), obtaining $\mathrm{Re}\{Y_{\mathrm{in}}\} = (1/g_m)\|R_p$, where R_p denotes the parallel equivalent resistance of the inductor.

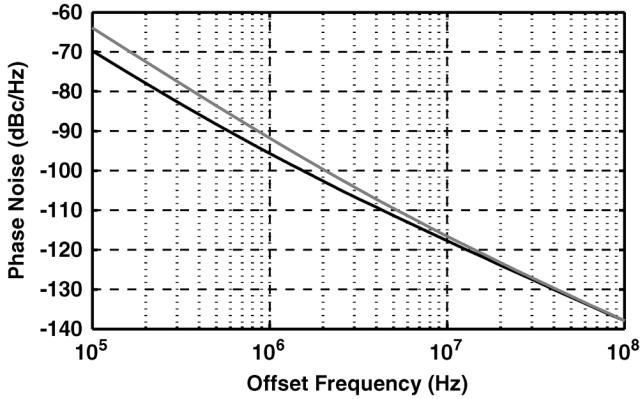


Fig. 10. Simulated phase noise of the proposed oscillator (black line) and cross-coupled oscillator (gray line).

The second comparison deals with the phase noise of the two oscillators for a given power dissipation and a given inductor design. In this case, the circuits incorporate identical transistor dimensions, but enough capacitance is added to the proposed oscillator nodes [i.e., C_1 and C_2 in Fig. 5(a) are artificially raised] so that the two topologies operate at the same frequency. Fig. 10 plots the simulated phase noise of both oscillators, suggesting a 4-dB advantage at 1-MHz offset and a 1-dB advantage at 10-MHz offset for the new topology. In these simulations, each circuit consumes 4 mW and operates at 82 GHz. The 4-dB advantage accrues because the flicker noise of transistors M_1 and M_3 in Fig. 6 produces negligible phase noise at 1-MHz offset. This can be explained by noting that, due to the path through L_1, a low-frequency voltage perturbation in series with the gate of M_1 can hardly change the phase difference between V_{X1} and V_{Y1}. Simulations confirm that such a perturbation generates a much smaller sideband in the proposed oscillator than in the cross-coupled topology.

IV. Divider Design

The bandwidth enhancement afforded by the proposed technique makes the amplifier topology of Fig. 5(a) attractive for high-speed frequency division as well. Shown in Fig. 11(a) is a Miller regenerative divider incorporating a mixer (M_1 and M_2) and an amplifier (M_3–M_6) employing the above concept. Cross-coupled transistors M_7–M_8 raise the gain, thus widening the frequency range of the divider. The inductor layouts follow the style illustrated in Fig. 8.

The limited voltage headroom points to the use of passive mixers in the Miller divider. However, the conventional double-balanced passive topology suffers from a drawback that proves serious in this environment. As illustrated in Fig. 11(b), the four transistors in such a mixer turn on simultaneously as LO and $\overline{\mathrm{LO}}$ cross, thus presenting a low instantaneous impedance between A and B. With sinusoidal LO waveforms, this "short circuit" persists for about 20% of the period, loading the amplifier and

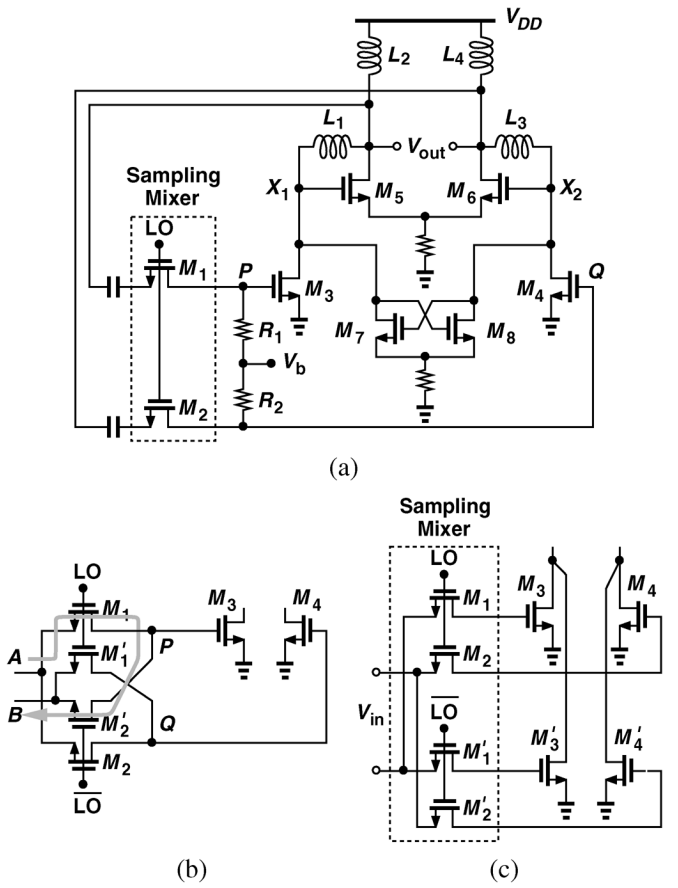


Fig. 11. (a) Frequency divider based on proposed technique. (b) Conventional double-balanced mixer. (c) Sampling mixer with differential LO phases.

limiting the lock range of the divider significantly. Moreover, the periodic switching of the total capacitance at node P between A and B creates another resistive component that further loads the amplifier. For example, a 20-fF capacitance switching at a rate of 130 GHz is equivalent to a resistance of 385 Ω.

The proposed differential-in, differential-out "sampling" mixer shown in Fig. 11(a) avoids this issue. With R_1 and R_2 establishing a time constant at nodes P and Q that is much greater than the LO period, this topology operates as a sample-and-hold circuit, thereby providing a voltage conversion gain close to that of the double-balanced topology of Fig. 11(b) $(4/\pi)$.

Another advantage of the sampling mixer is that it senses and produces differential signals while requiring a single-ended LO. This attribute proves critical in testing standalone high-speed dividers because it is extremely difficult to generate and route differential LO phases externally. If the divider is driven by an on-chip differential LO, then the sampling mixer can be realized as shown in Fig. 11(c), where an input short circuit is still avoided and the outputs are summed in the current domain.

The common-mode level at the sources and drains of the sampling devices in Fig. 11(a) is given by $V_{GS3,4}$, dictating a sufficiently high DC level for the LO so that M_1 and M_2 turn on with a large overdrive voltage. This is accomplished by setting the DC level of their gate voltages to V_{DD} through a resistor and capacitively coupling the LO.

Three prototypes of the divider of Fig. 11(a) have been designed with $(W/L)_{3-6} = 15\ \mu\text{m}/0.1\ \mu\text{m}$, a supply current of 7 mA, and different inductor values ($L_2+L_4 = 710$ pH, 610 pH, 520 pH) to achieve operation in the range of 80 to 130 GHz.

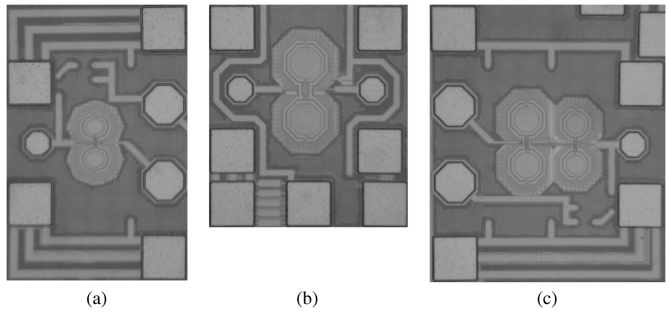


Fig. 12. Die photographs of (a) oscillator, (b) divider, and (c) two oscillators with their outputs mixed.

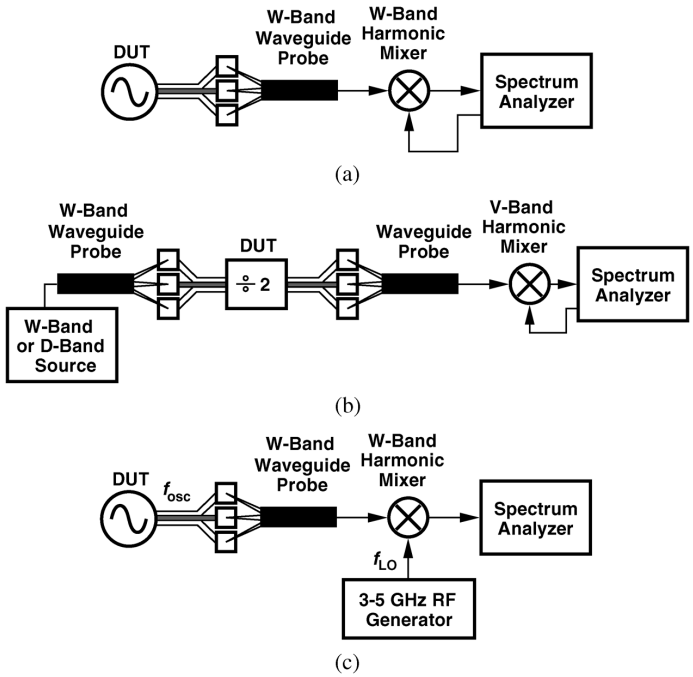
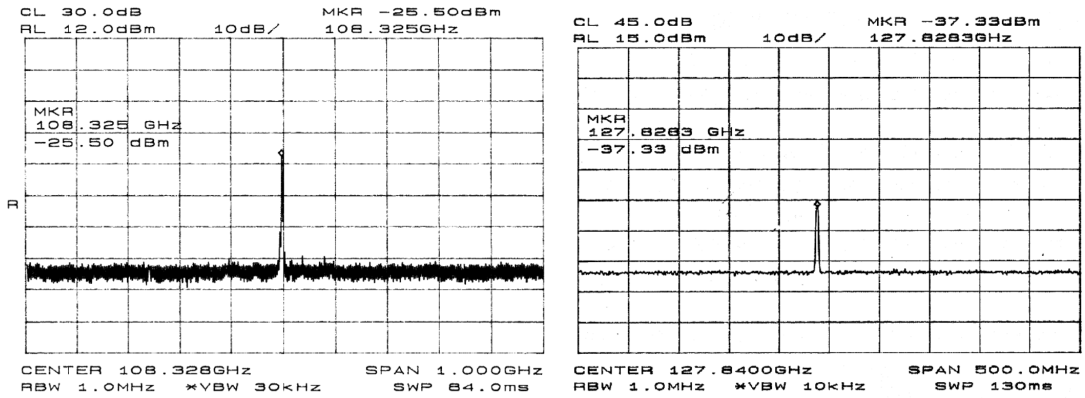


Fig. 13. Test setups for (a) oscillators, (b) dividers, and (c) unambiguous measurement of oscillator frequencies.

V. Experimental Results

The oscillators and frequency dividers have been fabricated in 90-nm CMOS technology and tested on a high-speed probe station. Fig. 12 shows the die photographs. The oscillator occupies an active area of 100 μm $\times$ 230 μm and the divider, 140 μm $\times$ 300 μm. Fig. 12(c) depicts the die photograph of two of the oscillators with their outputs mixed on-chip. The purpose of this arrangement is explained below.

Shown in Fig. 13(a) is the test setup for the oscillators. The output is sensed by a W-band (70–110 GHz) waveguide probe, applied to a W-band harmonic mixer, and monitored on a spectrum analyzer. For the frequency divider, as illustrated in Fig. 13(b), the input is provided by W-band and D-band generators manufactured by Micro-Now. The output is sensed by a V-band waveguide probe and, for input frequencies greater than 100 GHz, applied to a V-band harmonic mixer.



(a) (b)

Fig. 14. Measured output spectra of (a) 108-GHz and (b) 128-GHz oscillators.

A spectrum analyzer providing the LO drive to a harmonic mixer displays numerous pairs of spectral lines, making it difficult to determine the actual frequency of oscillators. This is particularly troublesome at low signal levels, for which the "signal identification" feature of the spectrum analyzer fails. To ensure correct measurement of the oscillation frequency, the setup shown in Fig. 13(c) complements that in Fig. 13(a). Here, the LO port of the harmonic mixer is driven by an external RF generator, with $f_{\rm LO}$ chosen such that $f_{\rm osc} - nf_{\rm LO}$ is a relatively small IF, e.g., 100 MHz. To determine n, $f_{\rm LO}$ is changed by Δf and the change in IF $(= n\Delta f)$ is measured.

The oscillator prototypes exhibit output frequencies of 83 GHz, 108 GHz, and 128 GHz while consuming 9 mW from a 1.2-V supply (excluding the on-chip buffer). The simulated f_T of the NMOS transistors is about 135 GHz and the self-resonance frequency of the inductors is around 145 GHz. The measured frequencies differ by 5% from the simulated values, which were obtained by first simulating the inductors, interconnects, and the metallization on the transistors as a multiport network in Ansoft HFSS and importing the S-parameters to Cadence. Fig. 14 shows the outputs of the last two. With the high loss of the harmonic mixers (e.g., >45 dB at 128 GHz), these output spectra provide no meaningful measure of the phase noise.[5] For this reason, the 108- and 128-GHz prototypes have also been laid out in close proximity [Fig. 12(c)] and their outputs have been mixed on-chip (Fig. 15) so as to produce a 20-GHz beat, which can be measured directly. Plotted in Fig. 16, this output reveals a phase noise of approximately −102 dBc/Hz at 10-MHz offset. The phase noise of each oscillator is about 3 dB lower. The discrepancy between this result and that in Fig. 7 is attributed to inaccuracies in inductor and transistor models as well as the noise picked up by the probes.

The three divider prototypes operate across the following frequency ranges: 88–104 GHz, 96–111 GHz, and 117–125 GHz. Fig. 17 shows the output spectra of the last two at the upper end of their lock range. The LO power in these measurements is roughly +3 dBm, with a great deal of uncertainty introduced by the unknown loss of the W-band input waveguide probe beyond its specified bandwidth as well as the quality of on-chip

[5]The unknown loss of the mixers also yields uncalibrated output power levels displayed by the spectrum analyzer.

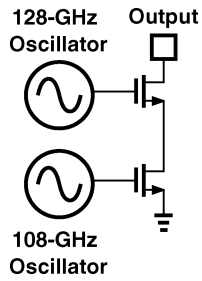


Fig. 15. On-chip mixing of two oscillator outputs.

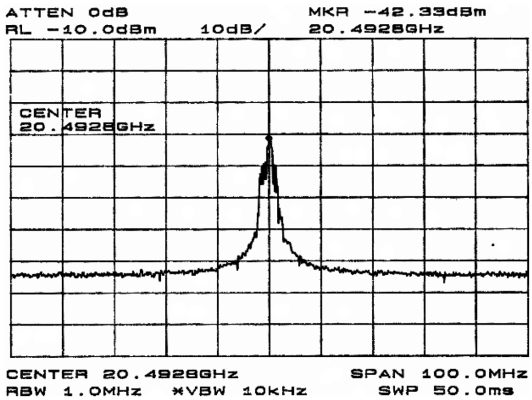


Fig. 16. Measured spectrum of mixed oscillator outputs.

50-Ω termination at these frequencies. Similarly, it is difficult to measure the minimum input level required for correct operation at each frequency because the loss of variable attenuators and waveguides cannot be easily calibrated.[6]

The measured performance of the proposed circuits is compared with that of recent art in Table I. Only fundamental oscillators in 90-nm technology are shown for consistency. We should remark that 1) while oscillators based on higher harmonics can be realized through the use of multiplication [14] or edge-combining [15], only fundamental oscillators can demonstrate the availability of *gain* at a given frequency, and 2) single-ended oscillators, e.g., those in [10] and [5], would consume about twice as much power if they were to become differential.

[6]This is primarily because no absolute reference is available at these frequencies: the generator output varies considerably with frequency and time, and the loss of mixers and variable attenuators is unknown.

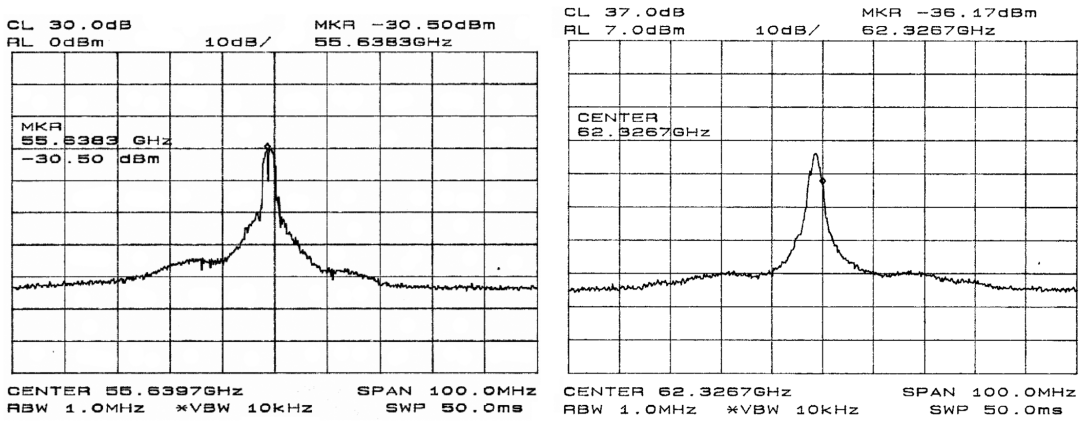


Fig. 17. Measured outputs of (a) 111 GHz and (b) 125 GHz dividers.

TABLE I
COMPARISON WITH PRIOR ART

Fundamental Oscillators	[10]	[11]	[5]	This Work
Frequency (GHz)	100	76	104	128
Power Diss. (mW)	30	13.6	6.5	9.0
Phase Noise (dBc/Hz at 10−MHz Offset)	−85	−111	NA	−105
Technology	90−nm CMOS	90−nm CMOS	90−nm CMOS	90−nm CMOS
Divide−by−Two Circuits	**[4]**	**[12]**	**[13]**	**This Work**
Frequency Range (GHz)	64−70	82−94	35−110	88−104 96−111 117−125
Power Diss. (mW)	6.5	8.4	225	10.5
Technology	0.13−um CMOS	65−nm CMOS	200−GHz SiGe	90−nm CMOS

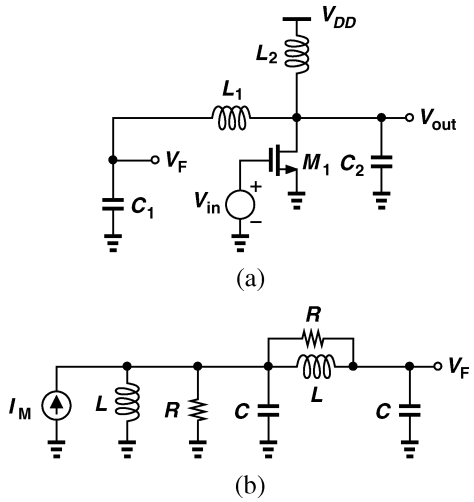


Fig. 18. (a) Open-loop circuit for loop transmission calculation. (b) Equivalent circuit.

VI. CONCLUSION

This paper has presented an inductive feedback technique that considerably raises the speed of high-frequency circuits, leading to fastest oscillators and dividers reported in 90-nm CMOS technology. Comparison of oscillators employing this technique with the conventional cross-coupled oscillator suggests advantages in the maximum frequency of operation and phase noise. A divide-by-two stage based on the proposed technique also incorporates a sampling mixer that accommodate differential inputs and outputs with a single-ended LO.

APPENDIX I

To determine the open-loop Q, we break the loop at the gate of M_1 as shown in Fig. 18(a). The objective is to determine the loop transmission and hence its phase slope. With the aid of the equivalent circuit depicted in Fig. 18(b), where $I_M = -g_m V_{\rm in}$, we write

$$\frac{V_F}{I_M}(s) = \frac{Ls\left(1+\frac{Ls}{R}\right)}{L^2C^2s^4 + 3\frac{L^2C}{R}s^3 + \left(3LC+\frac{L^2}{R^2}\right)s^2 + 2\frac{L}{R}s + 1}. \tag{18}$$

If the transfer function is expressed as $(A+jB)/(C+jD)$, then

$$\frac{d\phi}{d\omega} = \frac{A\frac{dB}{d\omega} - B\frac{dA}{d\omega}}{A^2+B^2} - \frac{C\frac{dD}{d\omega} - D\frac{dC}{d\omega}}{C^2+D^2}. \tag{19}$$

For the transfer function in (18), $A = -L^2\omega^2/R$, $B = L\omega$, $C = L^2C^2\omega^4 - (3LC + L^2/R^2)\omega^2 + 1$, and $D = -3L^2C\omega^3/R + 2L\omega/R$. Substituting these values in (19), carrying out the lengthy algebra, assuming $LC\omega^2 = (3+\sqrt{5})/2$ and $\mathrm{Q}^2 = (R/L\omega)^2 \gg 1$, and multiplying the result by $\omega/2$, we obtain the expression in (13).

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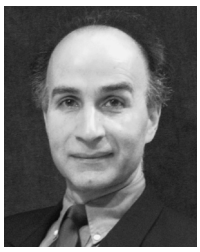

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