Behzad Razavi

The Flash ADC

Flash analog-to-digital converters (ADCs) find wide application both as stand-alone components and as building blocks of more complex systems. This architecture dates back to at least the early 1960s. For example, in a patent filed in 1963, Stephenson [1] describes the "parallel" ADC as a known technique. In this article, we study the properties and design issues of this topology.

Basic Architecture

To convert an analog signal to digital form, we can compare its value against a number of equally spaced reference voltages that span the expected range of input amplitudes. Shown in Figure 1, an N-bit flash ADC employs 2^N comparators along with a resistor ladder consisting of 2^N equal segments. The sampling function, which is necessary for conversion from continuous time to discrete time, can be realized within the comparators or as an explicit operation preceding this circuit. In response to $V_j < V_{in} < V_{j+1}$, comparators number one through j produce a logical one at their outputs and the remaining, a logical zero. This "thermometer code" is then converted to a binary or gray output.

The simplicity and elegance of this architecture make it suitable for various conversion rates so long as the speed–power tradeoff remains linear. A favorable tradeoff is obtained if the ADC incorporates a comparator topology with zero static power—a StrongArm latch [2]–[4], for example. As explained below, the ladder's static current is ultimately chosen according to the conversion speed.

Design Issues

The principal drawback of the flash ADC is the exponential growth of its "cost" as a function of resolution. The cost includes power consumption, input capacitance, comparator kickback noise, chip area, and difficulties in routing the signals. We elaborate on some of these issues here.

Suppose we wish to double the resolution of a 5-b flash stage. The analog least-significant bit (LSB) value is halved and so must be the comparator voltage. Using the MOS threshold mismatch equation $\Delta V_{TH} = A_{VTH}/\sqrt{WL}$, where A_{VTH} is a constant and WL denotes the channel area, we observe that WL must quadruple. Since the number of comparators is also doubled, the input capacitance rises by a factor of eight. This trend underscores the need for comparator offset cancellation for resolutions of 4 b and above.

The kickback noise of the comparators also becomes problematic as the resolution increases. This noise arises on each clock edge, as the comparators' input transistors couple internal transitions to the input terminals. Consider, as an example, the StrongArm latch input path shown in Figure 2. We identify two kickback mechanisms: 1) when nodes X and Y fall, they draw a transient current from the inputs through C_{GD1} and

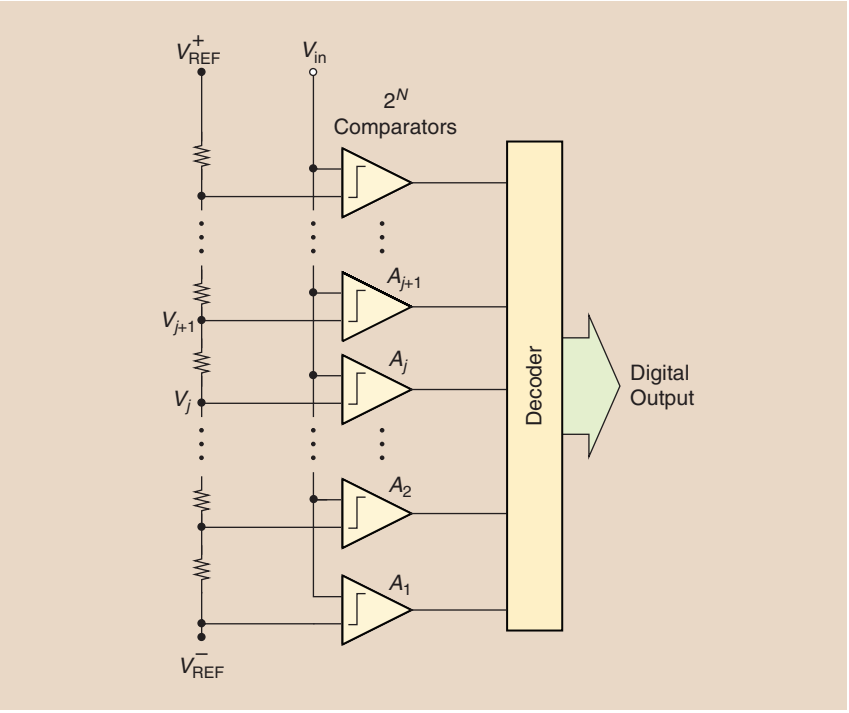

FIGURE 1: The flash architecture.

Digital Object Identifier 10.1109/MSSC.2017.2712998
Date of publication: 25 August 2017

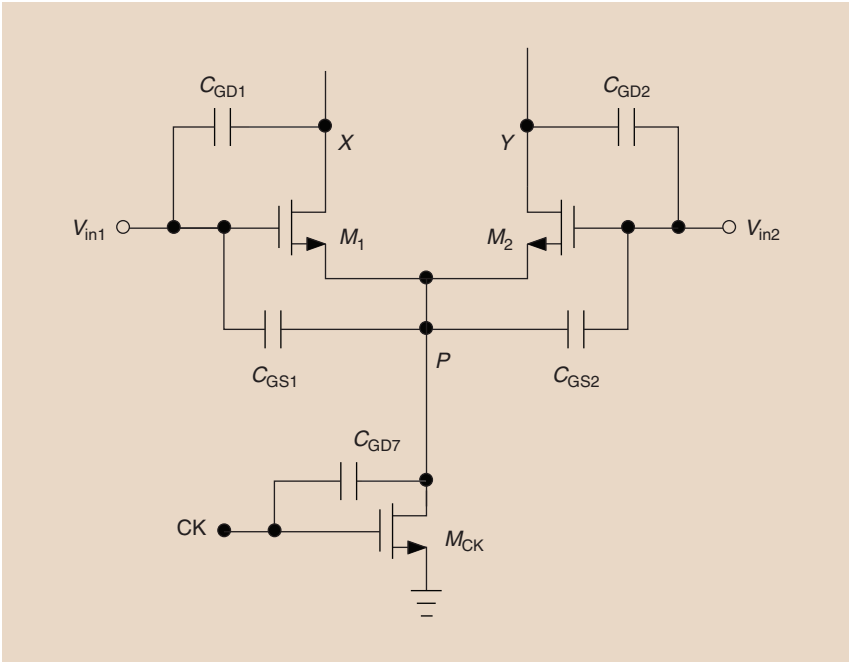

FIGURE 2: The input stage of a StrongArm latch.

C_{GD2}, a significant effect as M_1 and M_2 enter the triode region and these capacitances increase, and 2) when CK goes high, M_{CK} turns on, drawing a transient current from C_{GS1} and C_{GS2} before V_P falls enough to turn M_1 and M_2 on. Note that both effects intensify as M_1 and M_2 are chosen wider so as to reduce the comparator offset. The trouble with kickback noise is that it corrupts the conversion of the present sample and/or lasts long enough to affect the next sample.

The kickback noise currents drawn from V_{in1} and V_{in2} in Figure 2 contain a significant differential component, leading to a differential error voltage if this component flows through a finite impedance. This is inevitable as the kickback sees either the ladder or the ADC input buffer. Consider the single-ended model shown in Figure 3, where $I_1, \ldots, I_n$ model the comparators' kickback noise and are assumed approximately equal. Using superposition, it can be shown that the voltage disturbance at node j on the ladder is given by

$$V_j = \frac{(n-j)j}{2} I_u R_u, \tag{1}$$

where I_u is the value of $I_1, \ldots, I_n$, and R_u the ladder unit resistance. The greatest error occurs at $j = n/2$ and is equal to $(n^2/8) I_u R_u$. To maintain this disturbance below 1 LSB, R_u must be sufficiently small, dictating a lower bound for the ladder's power consumption. It is interesting to note that this power is, in fact, proportional to the sampling rate because, at higher speeds, the kickback noise has less time to subside, and vice versa.

One can precede a comparator design such as the StrongArm latch with a continuous-time differential pair to reduce both the input-referred offset and the kickback noise, but at the cost of considerable power penalty. The kickback noise currents in Figure 3 ultimately flow from V_{REF}^- and V_{REF}^+, demanding that these voltages have a low impedance. This issue translates to a high power dissipation in the reference buffers. One can place a capacitor between these two nodes, but the value of such a capacitor must be very large; otherwise, it slows down the settling of the ladder voltages.

Another difficulty in flash ADC design relates to the appearance of "bubbles" in the thermometer code. Suppose the offset of comparator number j, V_{osj}, in Figure 1 exceeds 1 LSB. Then, for

$$V_{j+1} < V_{in} < V_j + V_{osj}, \tag{2}$$

this comparator and comparator number $j+1$ produce a zero and a one, respectively, leading to a thermometer code of the form …11010…. Called a bubble, the out-of-place zero generated by comparator number j can create large errors as it travels through the decoder. We generally employ some means of bubble correction; for example, we can detect this situation and swap the outputs of comparators j and $j+1$ [5]. Alternatively, the decoder can simply count the total number of ones in the thermometer code and deliver the result as the final output.

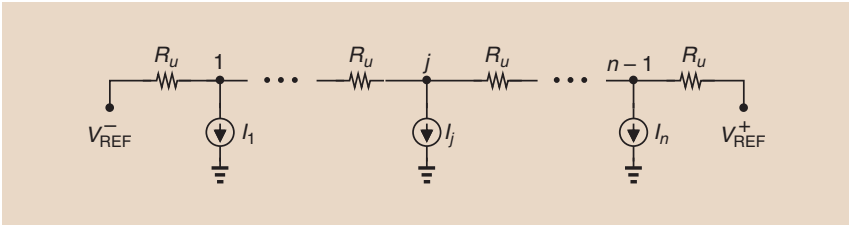

FIGURE 3: A model of kickback noise injected into the ladder.

Fully Differential Design

In most applications, the ADC must digitize a differential analog input, necessitating that the comparators compare this signal to a differential reference. Figure 4(a) illustrates one approach, where a StrongArm latch incorporates two differential pairs that produce currents proportional to $V_{in1} - V_{r1}$ and $V_{in2} - V_{r2}$, with V_{r1} and V_{r2} representing differential reference voltages. These currents are summed at the drains of $M_1 - M_4$ to yield $I_1 - I_2 \propto (V_{in1} + V_{r2}) - (V_{in2} + V_{r1}) = (V_{in1} - V_{in2}) - (V_{r1} - V_{r2})$.

The topology of Figure 4(a) entails three issues. First, the common-mode (CM) level of V_{r1} and V_{r2} must

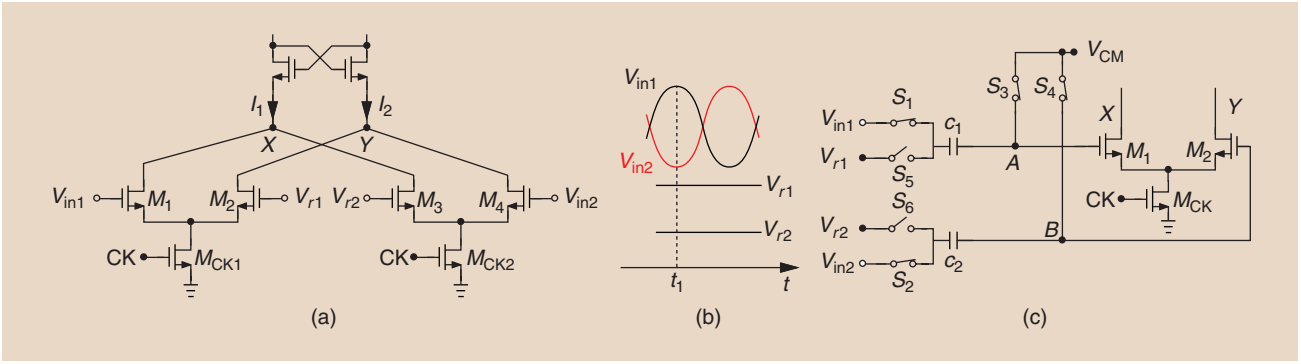

FIGURE 4: (a) A comparator input stage based on two differential pairs, (b) the effect of different CM levels, and (b) an alternative input stage.

accurately track that of V_{in1} and V_{in2}. To see this point, we note in Figure 4(b) that, even if $V_{in1} - V_{in2} \approx V_{r1} - V_{r2}$ at $t = t_1$, each differential pair experiences a heavy imbalance and suffers from a low transconductance. As a result, the mismatches at nodes X and Y and beyond contribute a higher input-referred offset. Second, the circuit introduces four devices, M_1–M_4 at the input and must therefore deal with the offsets of two differential pairs. Specifically, we have $I_1 - I_2 \propto (V_{in1} - V_{in2}) - [(V_{r1} - V_{os1}) - (V_{r2} - V_{os2})]$, where V_{os1} and V_{os2} denote the offset voltages of $M_{1,2}$ and $M_{3,4}$, respectively. Third, the input CM range of the circuit has a lower bound given by V_{GS1-4} and the voltage headroom necessary for M_{CK1} and M_{CK2}. This issue limits the flash ADC's full-scale range, especially at low supply voltages.

Shown in Figure 4(c) is an alternative fully differential input stage that ameliorates the foregoing difficulties. Here, a single differential pair senses an input difference produced by the input switching network and given by $(V_{in1} - V_{in2}) - (V_{r1} - V_{r2})$. In other words, this circuit performs the subtraction in the voltage domain [while in Figure 4(a), it is done in the current domain]. The comparator operates in three phases. First, CK is low, S_1–S_4 are on, and the input network samples the analog signal on C_1 and C_2. Next, these switches turn off and S_5 and S_6 turn on, producing at A and B a voltage difference nearly equal to $(V_{in1} - V_{in2}) - (V_{r1} - V_{r2})$. With a slight delay, CK then goes high to activate the comparator core circuit. This delay is necessary to guarantee that $V_A - V_B$ departs significantly from zero before M_1 and M_2 begin to amplify.

In contrast to the structure of Figure 4(a), the input stage shown in Figure 4(c) deals with the offset of only one differential pair and does not require accurate tracking between the input and reference CM levels. Furthermore, capacitive coupling in this arrangement allows rail-to-railinputswings. Yet another advantage is that the analog sampling provided by C_1 and C_2 in Figure 4(c) obviates the need for a lumped front-end sampler for the ADC. On the other hand, the clocking and X and Y discharge actions in Figure 4(a) tend to *integrate* the input and hence "smear" the sampling point, generally necessitating that the ADC employ an explicit sample-and-hold circuit.

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The use of the sampling network in Figure 4(c) does raise the input capacitance presented to the analog input. To ensure negligible attenuation of $(V_{in1} - V_{in2}) - (V_{r1} - V_{r2})$, C_1 and C_2 must be chosen much greater than the capacitances seen at A and B. For example, suppose $C_1 = C_2 = 5C_{in}$, where C_{in} includes the gate capacitance of the differential pair and the drain capacitance of S_3 (or S_4). This means that the input capacitance in the sampling mode is more than five times that in Figure 4(a). When S_5 and S_6 turn on, V_{AB} reaches $[(V_{in1}-V_{in2}) - (V_{r1}-V_{r2})][C_1/(C_1+C_{in})] = (5/6)[(V_{in1}-V_{in2})-(V_{r1}-V_{r2})]$, exhibiting a loss of about 17%.

It is possible to reduce the capacitance presented to the analog input by changing the switching sequence in Figure 4(c). We first turn on S_3–S_6 to sample the differential reference on the capacitors and then turn off these switches and turn on S_1 and S_2. The differential voltage thus generated between A and B is the same as before, but the capacitance seen by V_{in1} and V_{in2} is now given by the series combination of the input capacitors and C_{in}. This approach, however, faces two drawbacks: 1) C_1 and C_2 load the resistor ladder, causing a long settling time for V_{r1} and V_{r2}, and 2) the circuit no longer samples the analog input, requiring a front-end sampler for the ADC. A similar timing is described in [6].

Flash ADC Variants

A number of architecture and circuit techniques have been invented to ease the tradeoffs in flash stages. We study two here.

Recall that the input capacitance of the converter grows rapidly with

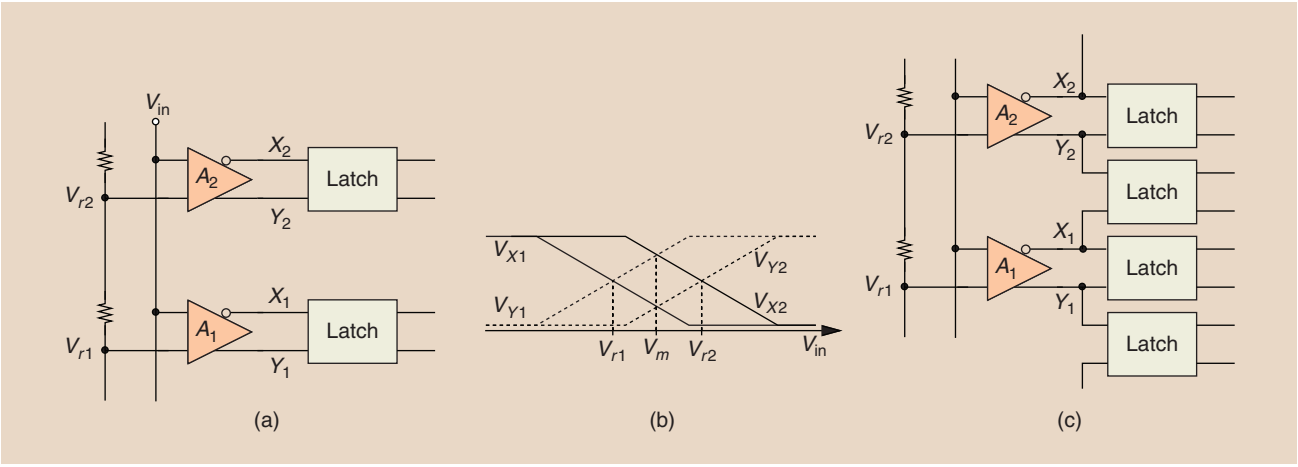

FIGURE 5: (a) A flash stage showing comparators' input differential pairs, (b) characteristics provided by the differential pairs, and (c) a flash stage using interpolation.

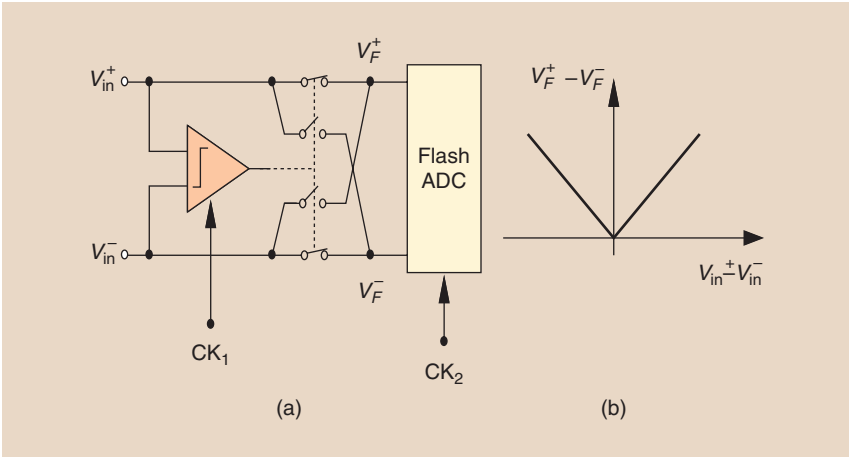

FIGURE 6: (a) A flash stage preceded by a polarity detector and (b) the resulting characteristic.

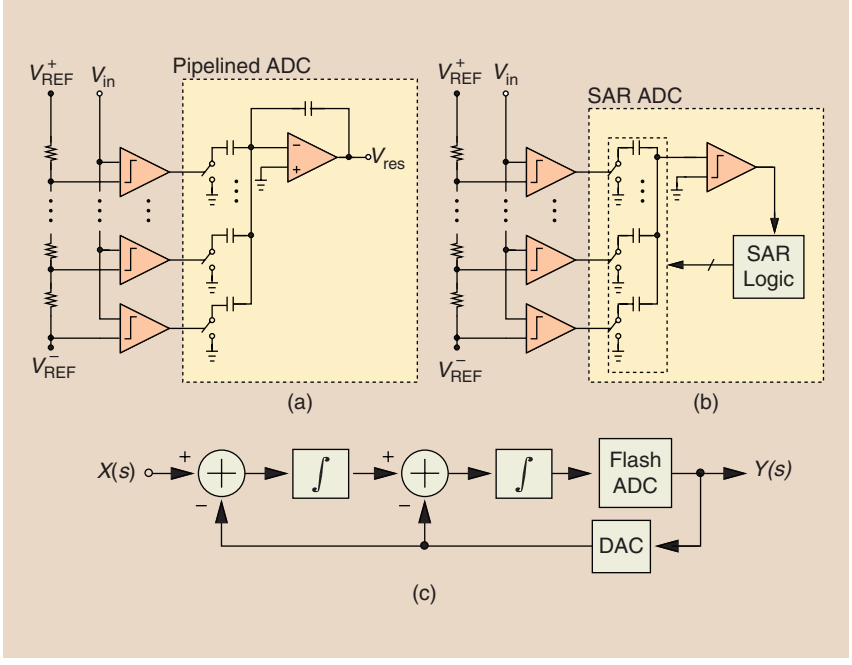

FIGURE 7: The use of flash stages in (a) pipelined converters, (b) SAR ADCs, and (c) $\Delta\Sigma$ modulators.

the resolution. It is possible to alleviate this issue through the use of interpolation. In this context, we view each comparator as a differential pair followed by a latch. Let us first examine the differential pair outputs in Figure 5(a) as V_{in} varies from below V_{r1} to above V_{r2}. Noting that $V_{X1} = V_{Y1}$ for $V_{in} = V_{r1}$ and $V_{X2} = V_{Y2}$ for $V_{in} = V_{r2}$, we can construct the characteristics shown in Figure 5(b). Now, we recognize that $V_{X1} = V_{Y2}$ at $V_{in} = V_m = (V_{r1} + V_{r2})/2$. That is, a latch sensing these two voltages (or V_{Y1} and V_{X2}) can detect when V_{in} crosses midway between V_{r1} and V_{r2}. As depicted in Figure 5(c), the "interpolating" flash [7] architecture doubles the resolution without doubling the number of differential pairs.

The performance improvement afforded by interpolation appears almost free, but it does require that the comparators include a differential pair and suffer from its power dissipation. In particular, a simple StrongArm latch would not suffice for the comparator design in this environment.

Another approach to reducing the complexity and power is illustrated in Figure 6(a) [8]. Here, a front-end comparator detects, under the command of CK_1, the *polarity* of $V_{in}^+ - V_{in}^-$ and accordingly routes the inputs through two of the switches such that the flash stage always senses a positive differential value. Plotted in Figure 6(b), the resulting characteristic

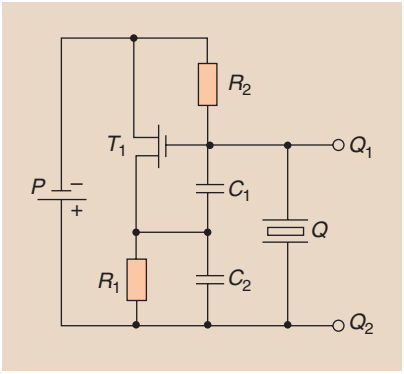

FIGURE 8: The MOS crystal oscillators patented by Luscher.

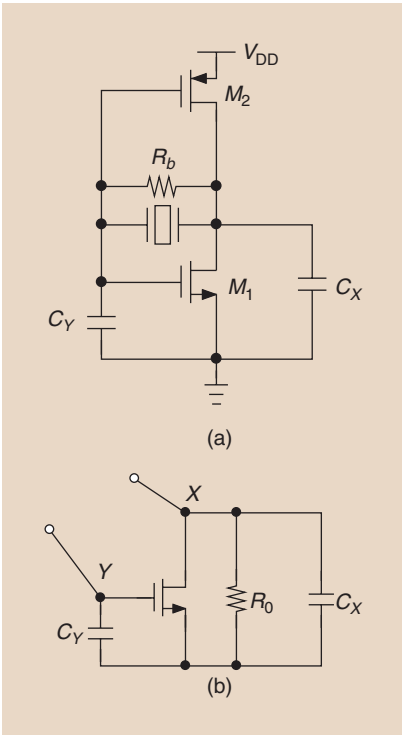

FIGURE 9: (a) A three-point oscillator using an inverter and (b) its simplified model.

is an example of "folding" and produces the most significant bit. Once $V_F^+ - V_F^-$ settles, CK_2 strobes the flash ADC so as to generate the remaining bits. We observe that the overall input capacitance, power, and complexity are approximately halved as the number of comparators drops from 2^N to $2^{N/2}+1$. These benefits accrue at the cost of more than twofold reduction in speed: not only must the front-end comparator respond to an input difference of, say, 0.5 LSB and activate the proper switches, but also $V_F^+ - V_F^-$ must also settle while the switches drive the input capacitance of the flash stage. Note that the offset of the front-end comparator must remain lower than 1 LSB.

Applications

Flash ADCs exhibit a favorable tradeoff between speed and power dissipation at low resolutions, e.g., in the range of 4–6 b. As such, they prove useful in extremely high-speed applications, e.g., in optical communication receivers that deal with high-order modulation schemes such as 64 quadrature amplitude modulation. Moreover, flash stages can augment other ADC architectures. As shown in Figure 7(a), a flash stage preceding a pipelined converter considerably reduces the magnitude of the residue generated by the first op amp, V_{res}, thereby relaxing its gain, linearity, and output swing requirements. Similarly, as depicted in Figure 7(b), a flash front end can 1) save some clock periods in the convergence of a successive approximation (SAR) ADC and 2) reduce the digital-to-analog converter settling time in the remaining SAR cycles. Another application is in ΔΣ modulators [Figure 7(c)], where a multibit (flash) quantizer lowers both the overall quantization noise and the integrator output swing.

As standalone circuits, flash ADCs perform full conversion in one clock cycle with the aid of massive comparator redundancy, the extreme opposite of how a SAR structure operates. For resolutions up to about 6 or 7 b, the flash topology provides a power-efficient, high-speed solution.

Questions for the Reader

1) In Figure 4(a), why can we not apply V_{in1} and V_{in2} to M_1 and M_2 and V_{r1} and V_{r2} to M_3 and M_4?
2) How does the characteristic shown in Figure 6(b) change if the front-end comparator has an offset equal to 1.5 LSB?

Answers to Last Issue's Questions

1) Estimate the oscillation frequency of Figure 8 if R_1 and R_2 are large.

   The impedance presented to the crystal consists of the series combination of C_1 and C_2 and a negative resistance. This net capacitance must be added to the parallel crystal capacitance in the parallel resonance frequency equation.
2) How does the finite output impedance of M_1 and M_2 in Figure 9 affect the oscillator's performance?

   Since M_1 and M_2 are in parallel, we can return to the three-point oscillator model shown in Figure 9(b) and ask how the finite resistance R_0 affects the startup condition. If R_0 is large, we can transform the parallel combination of R_0 and C_X to a series combination having an equivalent resistance approximately equal to $1/(R_0 C_X^2 \omega^2)$. Thus, this positive resistance weakens the effect of the negative resistance provided by the transistors.

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