The Role of PLLs in Future Wireline Transmitters

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***Abstract*—As data rates in wireline transmitters approach 80–100 Gb/s, phase-locked loops emerge as a serious bottleneck, requiring co-design of the clock and data paths. This paper describes speed, skew, and jitter issues at these rates and formulates the corruption due to effects such as the reference phase noise and the loop filter leakage. The phase noise performance of cascaded loops is also analyzed and a new transmitter architecture is proposed that substantially relaxes the speed and skew requirements.**

***Index Terms*—Cascaded phase-locked loops (PLLs), dividers, frequency doublers, gate leakage, millimeter-wave circuits, multiplexers, oscillators, phase noise, random and deterministic jitter.**

I. Introduction

THE demand for higher data rates in wireless and wireline systems continues to push circuit and architecture design. At present, the link speeds are approaching 20 Gb/s in copper media and 40 Gb/s in fiber media; it is therefore plausible that the next generation will reach 80–100 Gb/s—at least in optical links.

This paper describes phase-locking issues in high-speed wireline transmitters and proposes circuit and architecture techniques to alleviate these issues. The paper expands upon and more rigorously deals with some of the concepts mentioned in [1] and also presents a number of new ideas. Section II summarizes general issues and Section III deals with random and deterministic jitter. Section IV analyzes cascaded loops and Section V describes a new architecture and its circuit details.

II. General Considerations

Fig. 1(a) shows a generic wireline transmit path consisting of a multiplexer (MUX) and a retiming flip-flop (FF). The phase-locked loop (PLL) produces a half-rate clock, f_{MUX}, to drive the MUX and a full-rate clock, f_{CK}, to drive the FF. The retiming is necessary so as to remove the jitter introduced by the mismatches within the MUX paths and by the duty cycle distortion of f_{MUX}. Note that the duty cycle distortion of f_{CK} is benign.

At high speeds, the architecture of Fig. 1(a) entails several issues. First, the $\div 2$ delay, ΔT, translates to a skew between the MUX output and the FF clock, degrading the retiming phase margin [Fig. 1(b)]. It is possible to cancel this skew by inserting a delay replica in series with f_{CK}, but the required full-rate bandwidth makes the design of the delay stage difficult. We deal with this issue in the architecture proposed in Section V.

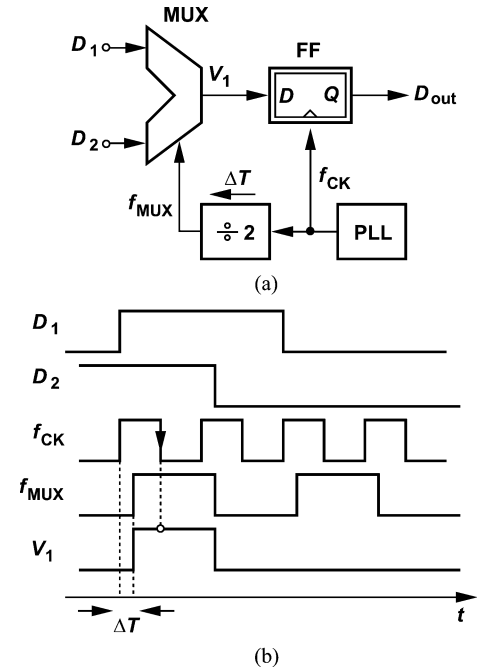

Fig. 1. (a) Generic transmitter. (b) Problem of divider delay.

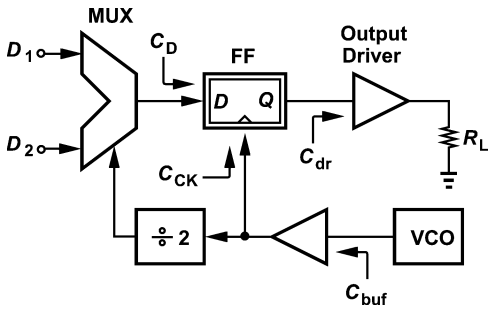

Fig. 2. Propagation of driver capacitance to VCO.

Second, the PLL and data path designs are inextricably linked. As illustrated in Fig. 2, the TX design begins with the output driver and proceeds backwards, sizing the FF so that it can drive the output stage, and the voltage-controlled oscillator (VCO) so that it can drive the FF and the $\div 2$ circuit. Since bandwidth, power consumption, and signal routing constraints limit the number of buffers that can be placed in the data and clock paths, we say the output driver's input capacitance "propagates" to the VCO.

Third, the VCO, the driver, and the retiming FF present difficult circuit design challenges as speeds reach 80–100 Gb/s. Fortunately, developments in millimeter-wave CMOS VCOs and

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dividers [2]–[5] can be leveraged here. We address the problem of FF design in Section V.

III. Jitter

A. Random Jitter Issues

If the retiming FF and the output driver in Fig. 1(a) provide sufficient bandwidth, the PLL becomes the dominant source of jitter in the transmitted data. At speeds approaching 80–100 GHz, the random jitter rises considerably because (1) the Q of inductors begins to saturate; for example, [6] reports a Q of 12 at 60 GHz; (2) the Q of varactors is likely to be even lower; (3) the very large frequency multiplication factor realized by the PLL greatly amplifies the reference phase noise, $S_{\rm REF}$. In this section, we investigate the choice of the PLL loop bandwidth so as to minimize the overall integrated phase noise. Consider a second-order type-II PLL having the following transfer function:

$$\frac{\phi_{\rm out}}{\phi_{\rm in}}(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{1}$$

The -3-dB bandwidth of the loop is obtained by equating the magnitude of (1) to $1/\sqrt{2}$ and is given by

$$\omega_{-3\ \rm dB}^2 = \left[2\zeta^2 + 1 + \sqrt{(2\zeta^2+1)^2+1}\right]\omega_n^2. \tag{2}$$

For $\zeta \approx 1$

$$f_{-3\ \rm dB} \approx 2.5 f_n \tag{3}$$

where $f_n = \omega_n/(2\pi)$. Called the "loop bandwidth," this value is usually chosen to be about one-tenth of the reference frequency. Approximating the PLL with a first-order low-pass filter (LPF) having this bandwidth, we express the total integrated phase noise at the output due to the reference phase noise as follows:

$$\overline{\phi_{n,tot}^2} \approx 2 \times \frac{\pi}{2}(2.5 f_n N^2 S_{\rm REF}) \tag{4}$$

$$\approx 2.5\pi f_n N^2 S_{\rm REF} \tag{5}$$

where the factor of 2 in (4) accounts for the phase noise on both sides of the carrier, $\pi/2$ denotes the noise bandwidth factor of a first-order LPF, and N is the PLL frequency multiplication factor. The square root of $\overline{\phi_{n,tot}^2}$ divided by 2π yields the fractional output jitter [in unit intervals (UI)]. To compute the output jitter in seconds, we write

$$\text{Jitter}_{\rm rms} = \frac{\sqrt{\overline{\phi_{n,tot}^2}}}{2\pi} \cdot \frac{1}{N f_{\rm REF}} \tag{6}$$

$$= \sqrt{\frac{1}{4\pi} \cdot \frac{2.5 f_n}{f_{\rm REF}} \cdot \frac{S_{\rm REF}}{f_{\rm REF}}}. \tag{7}$$

If the loop bandwidth, $2.5 f_n$, is equal to a certain fraction of the reference frequency, $\alpha f_{\rm REF}$, then

$$\text{Jitter}_{\rm rms} = \sqrt{\frac{1}{4\pi}\frac{\alpha S_{\rm REF}}{f_{\rm REF}}}. \tag{8}$$

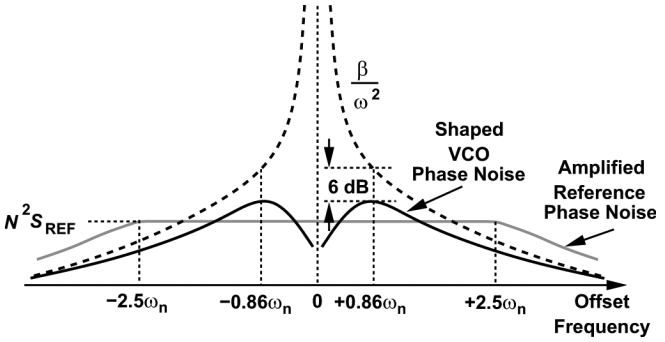

Fig. 3. Shaped reference and VCO phase noise in a PLL.

Remarkably, the jitter (in seconds) due to the reference phase noise remains independent of the PLL multiplication factor or the output frequency.[1] For example, high-quality (high-cost) crystal oscillators around 100 MHz exhibit a phase noise of about -150 dBc/Hz at offsets higher than 100 kHz, yielding an rms jitter of 0.28 ps if $\alpha = 0.1$. The peak-to-peak jitter is roughly 8 times this value—about 0.22 UI at 100 GHz.

Let us now consider the effect of VCO phase noise. The transfer function from the VCO output to the PLL output is given by

$$\frac{\phi_{\rm out}}{\phi_{VCO}}(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{9}$$

If flicker noise contributes negligibly, the VCO phase noise is given by β/ω^2, where β is a proportionality factor. The PLL output phase noise is therefore equal to the magnitude squared of (9) multiplied by β/ω^2

$$S_{\rm out} = \frac{\omega^4}{(\omega^2-\omega_n^2)^2 + 4\zeta^2\omega_n^2\omega^2} \cdot \frac{\beta}{\omega^2}. \tag{10}$$

This profile begins from zero at $\omega = 0$, reaches a peak at

$$\omega_{\rm peak} = \sqrt{-\zeta^2 + \sqrt{\zeta^4+2}}\,\omega_n \tag{11}$$

and approaches β/ω^2 as ω^4 becomes sufficiently large in the denominator of (10). If $\zeta = 1$, the peak of the profile occurs at $\omega \approx 0.86\omega_n$ and is equal to

$$S_{\rm out,peak} = \frac{\sqrt{3}-1}{3}\frac{\beta}{\omega_n^2} \tag{12}$$

$$\approx \frac{1}{4.1}\frac{\beta}{\omega_n^2}. \tag{13}$$

The profile is thus 6 dB below the free-running phase noise at $\omega \approx 0.86\omega_n$ and approaches β/ω^2 as ω exceeds approximately $4\omega_n$. Fig. 3 summarizes these results.

The optimization of the loop bandwidth requires that we integrate (10) from 0 to ∞, add (5) to the result, and differentiate with respect to f_n. Since (10) does not easily lend itself to this analysis, we seek a simpler expression that reaches a maximum of $\beta/(4\omega_n^2)$ at $\omega = 0.86\omega_n$ and a value of β/ω^2 at

[1]This point should not be confusing: if N varies, either $f_{\rm REF}$ or the output frequency must vary. In the latter case, the phase noise rises but the jitter (in seconds) remains constant.

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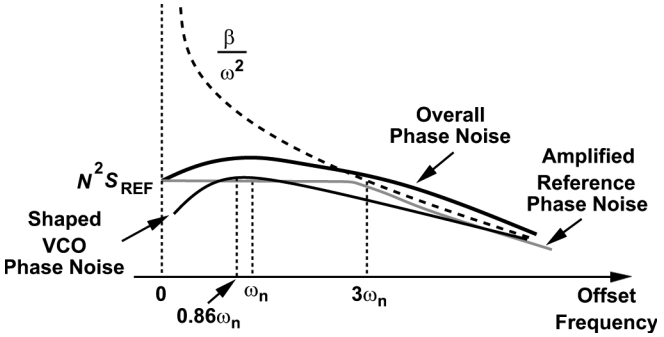

Fig. 4. Optimum choice of loop bandwidth.

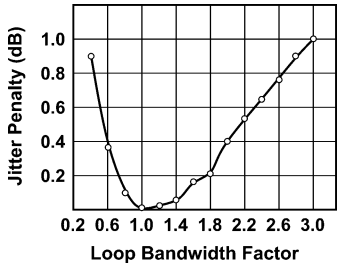

Fig. 5. Rise in jitter as loop bandwidth deviates from intersection frequency of amplified reference phase noise and VCO phase noise.

$\omega \approx 4\omega_n$ [similar to the behavior of (10)]. Such an expression is as follows:

$$S_{\text{out}} = \frac{f}{f^2 - 1.1f_n f + 0.9f_n^2} \times \frac{\beta}{16\pi^2 f_n} \tag{14}$$

where ω and ω_n have been replaced with $2\pi f$ and $2\pi f_n$, respectively. The integral of this function from $f = 0$ to $f = 10f_n$ (the region enclosing about 95% of the phase noise power) is equal to

$$\int_0^{10f_n} S_{\text{out}} df = \frac{0.204\beta}{\pi^2 f_n}. \tag{15}$$

The total integrated output phase noise due to the reference and the VCO can thus be written as

$$\overline{\phi_{n,tot}^2} = 2.5\pi f_n N^2 S_{\text{REF}} + \frac{0.204\beta}{\pi^2 f_n} \tag{16}$$

which reaches a minimum of

$$\overline{\phi_{n,tot,min}^2} = 0.8\sqrt{N^2 \beta S_{\text{REF}}} \tag{17}$$

if f_n is chosen equal to

$$f_n = \frac{0.32}{2\pi}\sqrt{\frac{\beta}{N^2 S_{\text{REF}}}}. \tag{18}$$

(Of course, if $N^2 S_{\text{REF}}$ is small, f_n has an upper bound imposed by the loop stability.) Fig. 4 plots the overall output phase noise in this optimized case. Note that the value of f_n suggested by (18) is approximately 1/3 the frequency at which β/ω^2 and $N^2 S_{\text{REF}}$ intersect. As a rule of thumb, we say that the "loop bandwidth" ($= 2.5f_n$) is chosen equal to the intersection frequency of the VCO phase noise and the amplified reference phase noise.

In order to assess the accuracy of the foregoing derivations, a linear phase model of a PLL has been simulated and the total integrated phase noise at the output due to the reference and the VCO computed. The loop bandwidth is then varied in a range around the intersection frequency of $N^2 S_{\text{REF}}$ and β/ω^2. To vary the loop bandwidth while maintaining a constant ζ, the charge pump (CP) current, I_P, and the main loop filter capacitor, C_1, are varied in opposite directions, i.e., in the form of γI_P and C_1/γ. Fig. 5 plots the rise in the total output jitter as γ varies from 0.4 to 3. For $\gamma = 1$, the loop bandwidth is equal to the intersection frequency. We observe that this choice indeed leads to minimum total jitter at the output.

B. Deterministic Jitter

Periodic modulation of the oscillator control voltage due to the charge pump (CP) nonidealities leads to reference sidebands and hence deterministic jitter. Various techniques have been developed to suppress these sidebands in the context of RF synthesizers, e.g., [7], and can be applied to wireline PLLs as well. However, an issue that has recently manifested itself, namely, the loop filter leakage current, demands investigation. This effect arises if the capacitors in the loop filter are realized as thin-oxide MOSFETs so as to save area.

Fig. 6 plots the simulated leakage for a $10\ \mu\text{m}/0.5\ \mu\text{m}$ device with a gate dielectric thickness of 20 Å in 45-nm technology. (The source and drain are grounded). Note that the strong dependence of the leakage current upon V_{GS} makes its cancellation difficult. Let us first consider the PLL in Fig. 7(a), where the loop filter is of first order. The MOS capacitor leakage current, I_G, discharges C_1 while the charge pump is off. In the steady stage, the PLL develops a static phase offset, ΔT, during which the CP replenishes the charge drained by I_G [Fig. 7(b)]. When the charge pump turns on, the Up current, I_P, flows through R_1, generating an instantaneous change of $I_P R_1$—a very large value. Capacitor C_1 then charges for ΔT seconds. The ripple remains unacceptably large in this case. We recognize that the "self-droop" rate, I_G/C_1, is independent of the MOS lateral dimensions and hence a constant of the technology (for a given V_{GS}). For example, $I_G/C_1 \approx 4.5\ \text{mV/ns}$ at $V_{GS} = 0.8$ V in 45-nm technology.

In practice, a second capacitor is added to the loop filter so as to absorb the unwanted CP injections [Fig. 8(a)]. Since C_2 is typically 5–10 times smaller than C_1, we neglect the leakage current of C_2 and repeat the above analysis. Constructing the equivalent circuit shown in Fig. 8(b), we observe that the average current produced by the CP is equal to I_G, thus creating an average voltage of $I_G R_1$ across R_1. The key point here is that, if the CP turns on briefly and if the ripple on the control voltage is small, then R_1 carries a current approximately equal to I_G most of the time. When the charge pump turns on, it rapidly charges C_2. After the charge pump turns off, C_2 is discharged through R_1 by a current approximately equal to I_G. If

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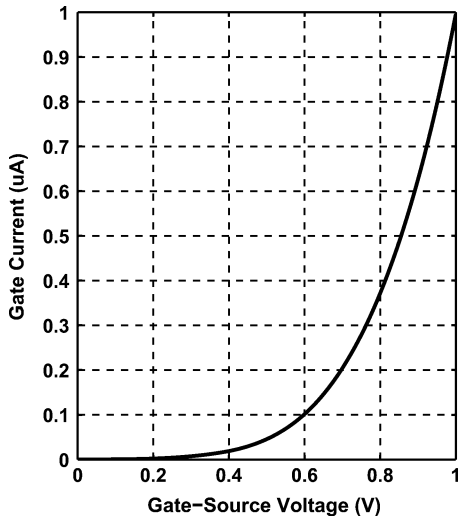

Fig. 6. Gate leakage in 45-nm technology.

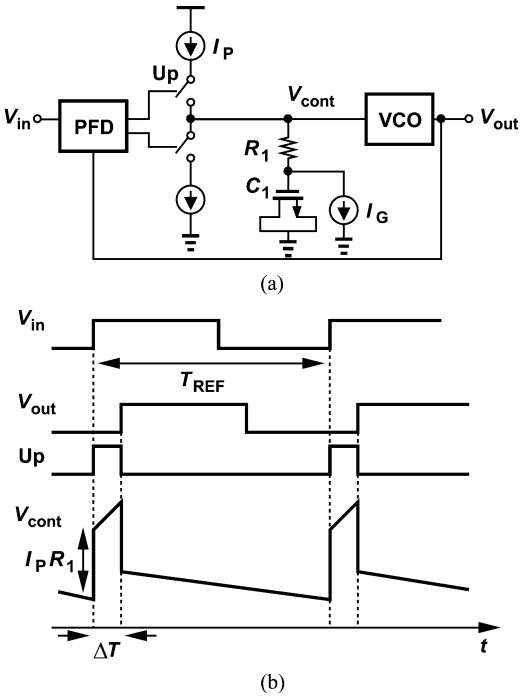

Fig. 7. (a) Gate leakage in a PLL. (b) Resulting phase offset and ripple.

the phase offset is small, the peak-to-peak ripple amplitude is equal to $(I_G/C_2)T_{\rm REF}$.

In order to calculate the output jitter resulting from the above phenomenon, we consider the detailed control voltage and output phase shown in Fig. 9. The average value of $V_{\rm cont}$ is such that the ripple areas above and below it cancel. With a small phase offset, the peak-to-peak variation of the phase is given by

$$\phi_{max} \approx K_{\rm VCO} \int_0^{T_{\rm REF}/2} \frac{I_G}{C_2} tdt \tag{19}$$

$$\approx \frac{1}{2} K_{\rm VCO} \frac{I_G}{C_2} \left(\frac{T_{\rm REF}}{2} \right)^2. \tag{20}$$

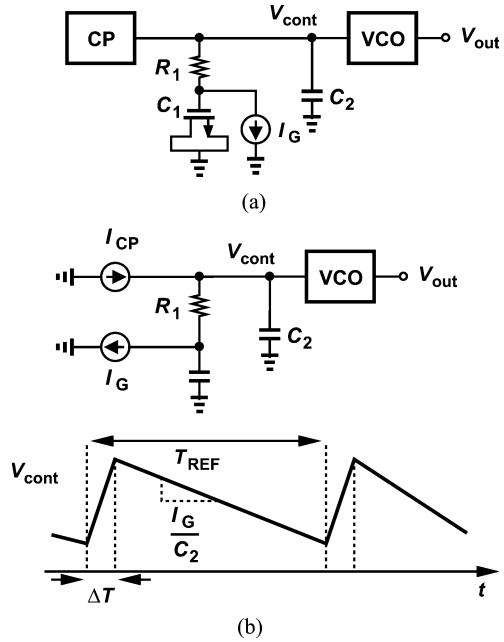

Fig. 8. (a) PLL using a second-order filter. (b) Equivalent circuit. (c) Resulting waveforms.

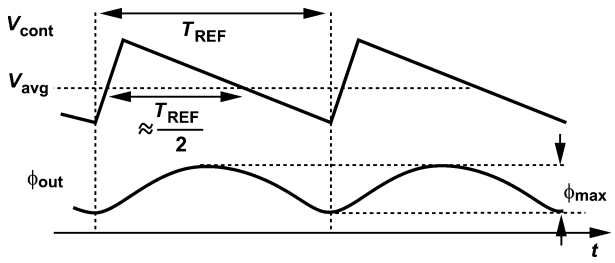

Fig. 9. Phase modulation due to leakage.

For example, if $K_{\rm VCO} = 2$ GHz/V, $I_G/C_2 = 5 \times 4.5$ mV/ns $(C_2 = C_1/5)$, and $T_{\rm REF} = 10$ ns, then $\phi_{\rm max} = 1.125$ UI. This very large value indicates that leakage cancellation is necessary. A cancellation technique is described in [8].

IV. Cascaded PLLs

With the large multiplication factors necessary to derive frequencies in the range of 80–100 GHz from crystal oscillators, one can consider a *cascade* of PLLs [9], [10] and determine whether proper choice of their bandwidth yields less jitter than a single PLL does. As shown below, cascading proves useful only under certain conditions.

Fig. 10 depicts a cascade of two PLLs. We assume the following are given: $f_{\rm REF}$, N_1N_2, the free-running phase noise of $\rm VCO_2(S_2)$, and the reference phase noise $(S_{\rm REF})$. We seek the optimum choice of N_1, N_2, and the loop bandwidths of the two PLLs, $\rm BW_1$ and $\rm BW_2$.

The benefit of cascading becomes apparent if three scenarios for $\rm VCO_1$ and $\rm VCO_2$ are considered: 1) The phase noise profile directly scales with frequency, $S_2 = N_2^2 S_1$. This occurs if the oscillator Q remains relatively *constant* from f_1 to f_2; 2) The phase noise does not scale, $S_2 = S_1$, i.e., the oscillator Q scales

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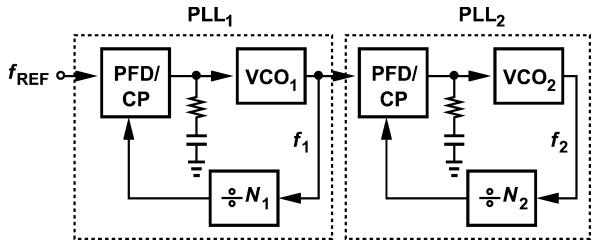

Fig. 10. Cascaded PLLs.

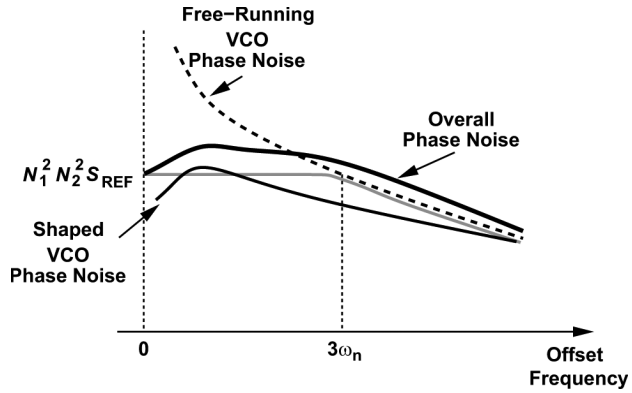

Fig. 11. Overall output phase noise of a single PLL with a given VCO phase noise.

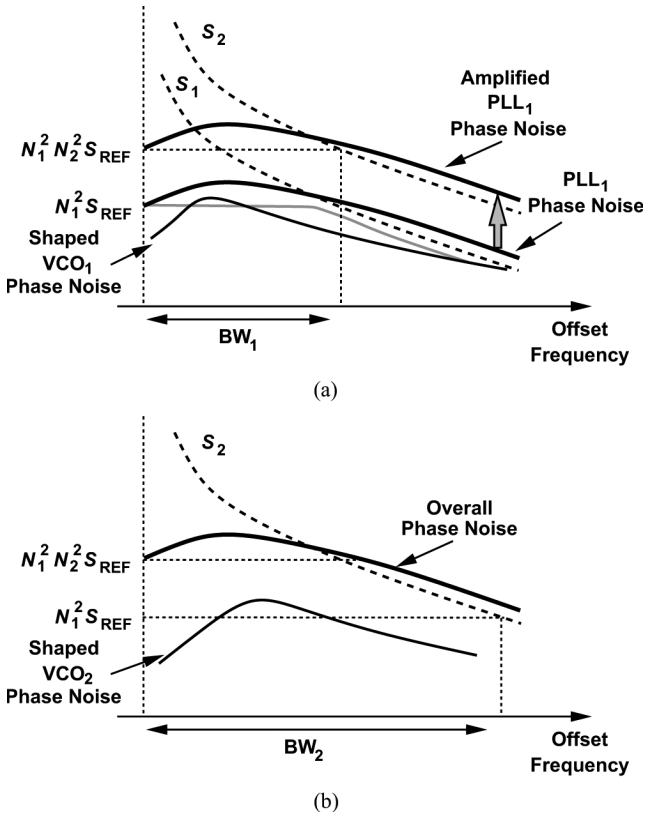

Fig. 12. (a) Phase noise of first PLL. (b) Overall output phase noise.

linearly with frequency; 3) The phase noise of VCO_2 is *higher* than $N_2^2 S_1$. We also follow the bandwidth choice prescribed by (18). As a point of reference, Fig. 11 shows the output phase noise of a *single* PLL operating at $N_1 N_2 f_{\mathrm{REF}}$.

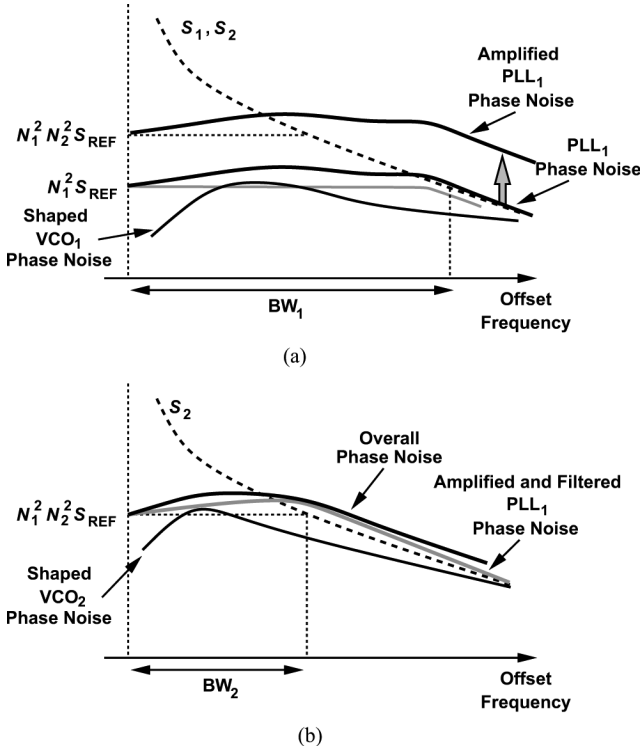

Fig. 13. (a) Phase noise of first PLL. (b) overall output phase noise.

Fig. 12(a) illustrates the first scenario. Proper choice of BW_1 yields the depicted phase noise profile at the output of PLL_1. This profile is amplified by a factor of N_2^2 but negligibly filtered by PLL_2. To this we add the shaped noise of VCO_2, arriving at the overall output spectrum shown in Fig. 12(b).[2] In the single-PLL case of Fig. 11, the output phase noise consists of a profile given by $N_1^2 N_2^2 S_{\mathrm{REF}}$ but limited to a bandwidth of BW plus the shaped noise of the VCO. In the scenario of Fig. 12, $\mathrm{BW}_2 \gg BW_1$ and the overall output phase noise consists of three components: (1) a profile given by $N_1^2 S_{\mathrm{REF}}$ and filtered by BW_1, (2) the shaped noise of VCO_1 amplified by a factor of N_2^2, and (3) the shaped noise of VCO_2, which is negligible. Since S_2 is assumed equal to $N_2^2 S_1$, we recognize that the sum of the first two components is equal to the phase noise of the single-PLL topology, concluding that cascading offers no phase noise advantage (and consumes higher power) in this scenario.

Shown in Fig. 13 is the second scenario. Here, BW_1 is chosen according to the intersection of S_1 and $N_1^2 S_{\mathrm{REF}}$, and BW_2 according to the intersection of S_2 and the amplified phase noise of PLL_1. We thus conclude that cascading offers no phase noise advantage in this scenario, either.

The third scenario is depicted in Fig. 14, where *both* BW_1 and BW_2 are chosen according to the intersection of $N_1^2 S_{\mathrm{REF}}$ with S_1 and S_2. The output phase noise of PLL_1 is amplified by a factor of N_2^2 while experiencing little filtering by PLL_2. The relatively large bandwidth of PLL_2 greatly reduces the phase noise of VCO_2, thereby yielding the overall output phase noise profile shown in Fig. 14(b). In comparison with the single PLL

[2]Note that BW_2 is chosen approximately equal to the intersection frequency of $N_1^2 S_{\mathrm{REF}}$ and S_2 so as to minimize the contribution of VCO_2.

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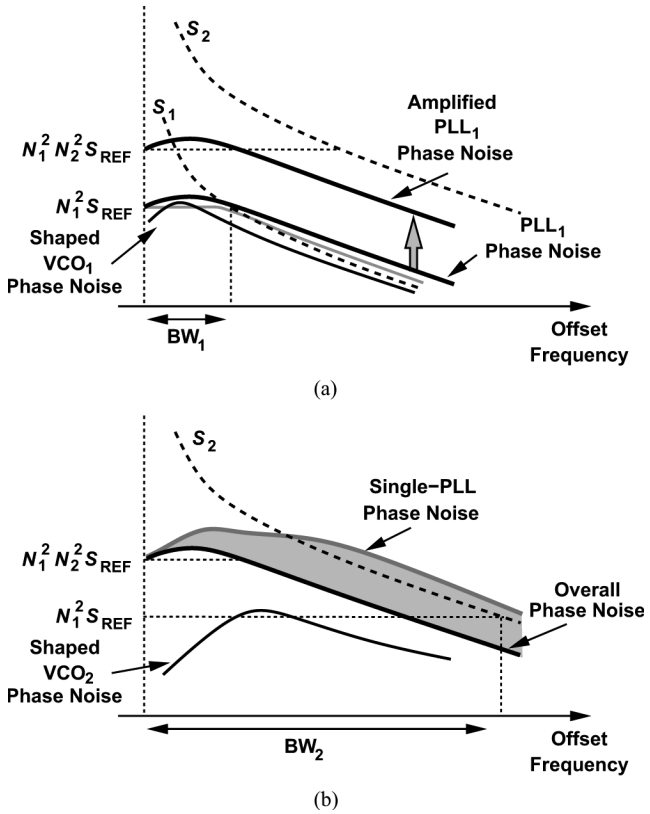

Fig. 14. (a) Phase noise of first PLL. (b) Overall output phase noise.

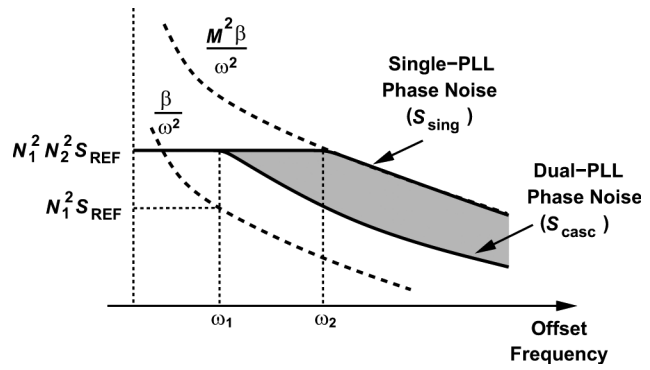

Fig. 15. Simplified phase noise profiles of single-PLL and cascade topologies.

case of Fig. 11, cascading saves an amount of phase noise given by the shaded area in Fig. 14(b) [9].

It is helpful to quantify the phase noise advantage accrued in the third scenario. To this end, we employ a more crude approximation of the phase noise profiles as shown in Fig. 15. Assuming $S_1 = \beta/\omega^2$ and $S_2 = M^2\beta/\omega^2$, where $M > N_2$, we compute the areas under the two profiles. Note that the shaped phase noise of VCO_2 is neglected so as to estimate the "best-case" improvement. The area under S_{casc} is given by

$$\overline{\phi^2_{\mathrm{casc}}} = 4N_1^2N_2^2S_{\mathrm{REF}}\omega_1 \tag{21}$$

where ω_1 is obtained from $\beta/\omega_1^2 = N_1^2N_2^2S_{\mathrm{REF}}$. It follows that

$$\overline{\phi^2_{sing}} - \overline{\phi^2_{\mathrm{casc}}} = 4\sqrt{\beta S_{\mathrm{REF}}}N_1N_2(M - N_2). \tag{22}$$

We can normalize this result to $\overline{\phi^2_{sing}}$

$$\frac{\overline{\phi^2_{sing}} - \overline{\phi^2_{\mathrm{casc}}}}{\overline{\phi^2_{sing}}} = 1 - \frac{N_2}{M}. \tag{23}$$

V. Proposed Transmitter Architecture

Borrowing ideas from RF design, we propose a transmitter architecture that relaxes two critical issues identified in the previous sections. Shown in Fig. 16, the architecture incorporates a "half-rate" PLL to drive the MUX along with a frequency doubler to clock the FF. The dummy MUX equalizes the loading seen by the VCO outputs.

The advantages of this approach over the conventional topology are as follows. 1) The twofold reduction in the PLL speed greatly eases the design of the VCO and the feedback frequency divider. For example, the first $\div 2$ stage may operate robustly at 50 GHz with no inductors [5], thus simplifying the layout and signal routing; 2) The architecture eliminates the troublesome divider delay depicted in Fig. 1(a). Instead, the doubler and MUX delays must match, a simpler task because they have the same polarity.

The performance of the proposed architecture hinges upon the doubler's design. This circuit must provide sufficient swings to the FF, preferably with no additional buffer or gain stages.

The proposed architecture (except for the PLL) has been designed at the transistor level and simulated in 65-nm CMOS technology for 80-Gb/s operation. Fig. 17 shows the MUX circuit. Class-AB clocking [11] and inductive peaking are utilized to improve the speed. The inductor model contains a parasitic capacitance and both series and parallel resistances to satisfy a relatively wide band, with the Q deliberately limited to about 5 at 80 GHz.

Depicted in Fig. 18, the doubler circuit is derived from the low-voltage symmetric XOR in [12]. Note that, to generate a differential output, I and $\overline{I}$ are mixed and so are Q and $\overline{Q}$. While typical doublers mix I and Q (and $\overline{I}$ and $\overline{Q}$), the XOR implementation of Fig. 18 produces larger output swings with the former permutation of the inputs. The doubler raises the PLL phase noise and sidebands by 6 dB.

An important concern here is that duty-cycle distortion in the oscillator output displaces every other falling (or rising) edge at the doubler output. More generally, asymmetries in the LO waveforms and in the doubler produce a 40-GHz component in the full-rate clock and hence systematic jitter in the FF output. To alleviate this issue, the doubler inductive loads must sufficiently attenuate the 40-GHz component. Simulations indicate that, with an inductor Q of 10 at 80 GHz, this component remains 40 dB below the 80-GHz waveform even with an amplitude imbalance of 10% between I and $\overline{I}$ or with an amplitude and phase imbalance of 10% and 10°, respectively, between I and Q. The resulting jitter is therefore negligible.

The retiming FF in Fig. 16 presents the greatest challenge in the design as it must generate a "clean" eye while presenting a small load capacitance to the MUX and the doubler. We introduce a new circuit technique here that markedly improves the speed of FFs. Illustrated in the latch shown in Fig. 19(a), the idea is to add a feedforward path that impresses the input data

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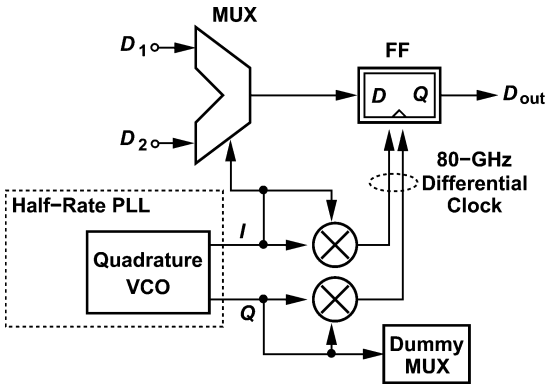

Fig. 16. Proposed transmitter architecture.

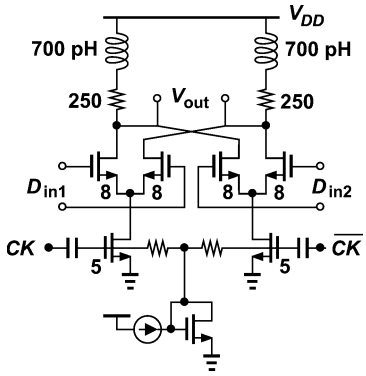

Fig. 17. MUX implementation. (Transistor widths are in microns; $L = 60$ nm).

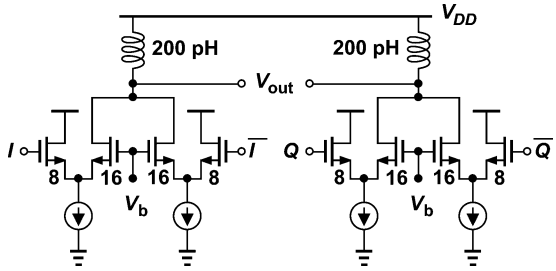

Fig. 18. Doubler implementation. (Transistor widths are in microns; $L = 60$ nm).

upon the output before the input differential pair turns on. However, the tail current of M_5–M_6—which is comparable to that of M_1–M_2—limits the voltage headroom. The circuit is therefore modified to the topology shown in Fig. 19(b). The feedforward path now exhibits a high-pass response, still a desirable behavior because the input components that we wish to feed forward lie at high frequencies.

Fig. 20(a) and 20(b), respectively, shows the simulated eye diagrams observed at the MUX and FF outputs at 80 Gb/s. Note that no buffer is inserted in the data or clock paths. Also, no effort is made to equalize the MUX and doubler delays. In these simulations, the FF is loaded by a differential pair having $8\ \mu\text{m}/0.06\ \mu\text{m}$ transistors as a representative load.

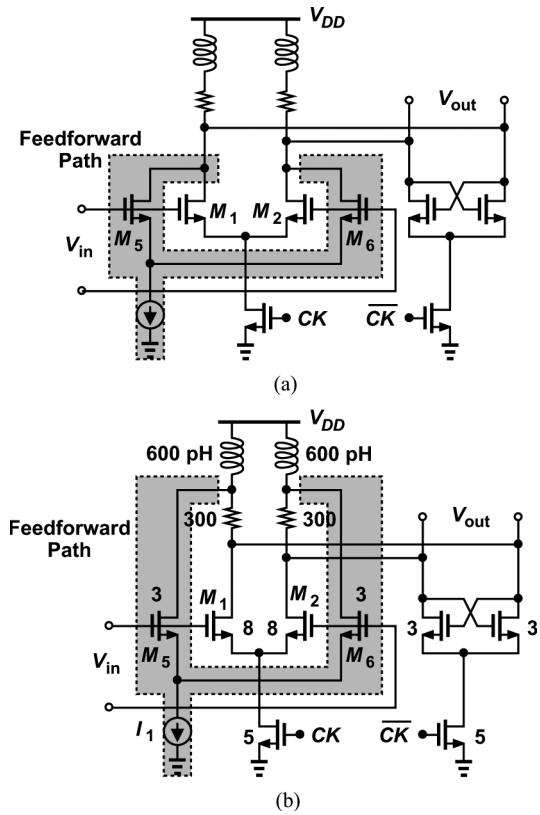

Fig. 19. (a) Latch with all-pass feedforward, (b) latch with high-pass feedforward. (Transistor widths are in microns; $L = 60$ nm, $I_1 = 1$ mA, and each clocked device carries an average current of 0.8 mA).

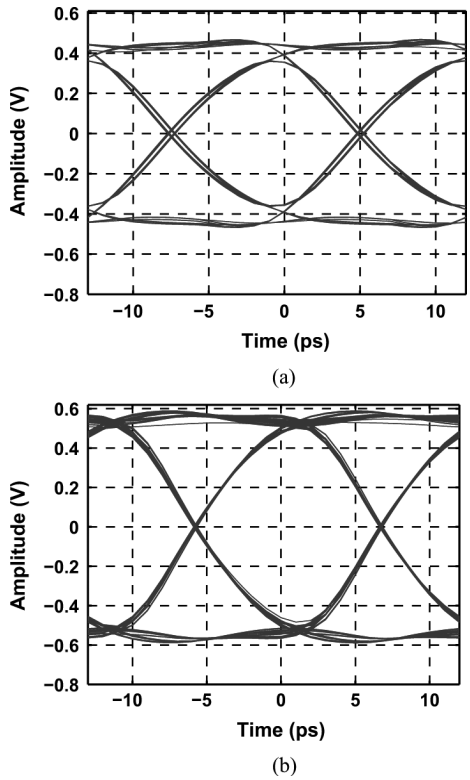

Fig. 20. Eye diagrams at the output of: (a) MUX, and (b) retiming FF.

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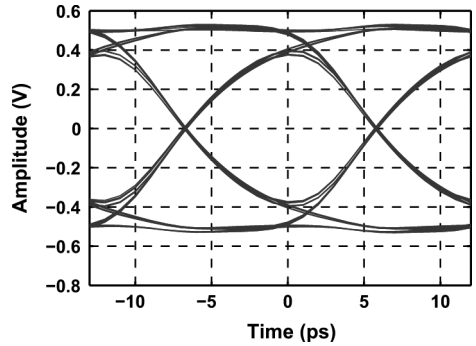

Fig. 21. FF output eye diagram without feedforward.

To demonstrate the efficacy of the feedforward technique, Fig. 21 depicts the FF output eye if M_5 and M_6 in Fig. 19(b) are removed. The eye suffers a vertical closure of 20% even though the FF presents less capacitance to the MUX.

VI. Conclusion

The design of PLLs for speeds approaching 80–100 GHz must deal with reference phase noise amplification in addition to the VCO phase noise. Also, the loop filter leakage leads to enormous systematic jitter, calling for precise cancellation techniques that can track the control voltage variations. The reference and VCO phase noise issues can be alleviated through the use of cascaded PLLs only if a moderate-frequency VCO with a very low phase noise can be realized in the first PLL. A new transmitter architecture employing a half-rate PLL has been demonstrated at 80 Gb/s in 65-nm CMOS technology.

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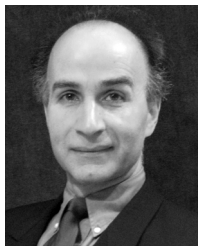

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