Design of Millimeter-Wave CMOS Radios: A Tutorial

Behzad Razavi, *Fellow, IEEE*

(Invited Paper)

***Abstract*—This paper deals with the challenges in the design of millimeter-wave CMOS radios and describes circuit and architecture techniques that lead to compact, low-power transceivers. Candidate topologies for building blocks such as low-noise amplifiers, mixers, oscillators, and frequency dividers are presented. Also, a number of radio architectures that relax the generation, division, and distribution of the local oscillator signal are reviewed. Last, integration issues for transmit and receive paths and for multiple beamforming transceivers are addressed.**

***Index Terms*—Low-noise amplifiers, Miller divider, millimeter-wave circuits, mixers, oscillators, transceiver architectures, 60-GHz band.**

I. Introduction

MILLIMETER-WAVE (mmW) CMOS transceivers have attracted heightened interest, especially in the 60-GHz band, over the past few years. Beginning with the first front end [1], numerous circuit and transceiver techniques have appeared in the literature [2]–[23], steadily refining the art and science of mmW CMOS design.

This paper describes mmW design challenges in CMOS technology and provides a tutorial overview of circuit and architecture techniques. Emphasizing that device/circuit/architecture co-design becomes even more important in the mmW regime, the paper aims to demonstrate techniques at each level of abstraction and their interdependencies.

Section II of the paper provides motivation for mmW work by considering some applications. Section III gives a brief background and Section IV addresses the design challenges. Section V introduces circuit and device techniques and Section VI deals with radio architectures.

II. Applications

The development of mmW radios began as a scientific curiosity and, even as of two years ago, appeared as a "solution looking for a problem." However, with the rapid progress in the standardization of wireless communication in the 60-GHz band by the IEEE802.15.3 Task Group 3c and the emergence of new applications, mmW circuits have swiftly become attractive.

The unlicensed band from 57 GHz to 64 GHz serves as the focus of today's mmW work. The standard is expected to allow a data rate of about 1.6 Gb/s in each 2.16-GHz channel within this band. Such data rates prove essential for transmitting uncompressed, high-quality video from a DVD player or camcorder to a TV or a server. Moreover, as the cost and power consumption of mmW transceivers decline, many other applications are likely to embrace them. For example, laptop computers can benefit from a much faster link when communicating with a (stationary) server, and hence shed most of their storage and processing capabilities, thereby approaching a "dumb" terminal.

An imminent application of 60-GHz radios relates to "quick downloads." For example, with most cell phones having a TV-quality display, a quick download link would enable a user to download a movie from a kiosk, say, in a subway station, for a nominal fee and in *a few seconds*, and play it en route to work.

Millimeter-wave circuits also find application in 77-GHz automotive radar. It is envisioned that each car will incorporate as many as 12 radars (3 on each side) to perform functions such as collision avoidance, blind spot detection, self-parking, and, eventually, autonomous driving. This application too demands a low-cost solution.

Another application that calls for even higher frequencies is imaging. Since the resolution of the images is inversely proportional to the wavelength, frequencies of 100 GHz and above are sought. Unlike visible light, millimeter waves travel through media such as dust or clothing, enabling new applications.

III. Background

Perhaps the first indication of mmW operation in CMOS technology was that provided by a 50-GHz oscillator in a 0.25-μm process [24]. Subsequently, a 40-GHz frequency divider was demonstrated in 0.18-μm technology [25]. Many other designs followed [1]–[23], [27].

The path to today's mmW CMOS radios can be characterized by two different design paradigms: (a) one followed by analog and RF designers, who prefer arbitrary interface impedances and SPICE-like simulators, and (b) another followed by microwave designers, who are more inclined to modular designs, impedance matching at each interface, and ADS-like simulators. It can also be observed that the former tend to use inductors and the latter, transmission lines (T-lines). Moreover, designs based on spiral inductors generally occupy a smaller area than those using T-lines [28]. For example, the inductor-based receiver (RX) in [7], consisting of a low-noise amplifier (LNA), an RF mixer, intermediate frequency (IF) mixers, an oscillator, and a frequency divider, occupies an active area of about 0.12 mm^2, whereas the T-line-based design in [8], comprising an LNA, an RF mixer, an oscillator, and a frequency doubler, consumes an active area of about 3.4 mm^2. Nonetheless, it is likely that these

Manuscript received September 4, 2008; revised November 11, 2008. Current version published February 4, 2009. This work was supported by Realtek Semiconductor and Skyworks. This paper was recommended by Associate Editor W. A. Serdijn.

The author is with the Department of Electrical Engineering, University of California, Los Angeles, CA 90095 USA (e-mail: razavi@ee.ucla.edu).

Digital Object Identifier 10.1109/TCSI.2008.931648

two paradigms will converge in the near future, leading to a robust, versatile design methodology.

IV. Design Challenges

Millimeter-wave CMOS radios present formidable challenges at all levels of abstraction, demanding that designers ascend and descend the device-circuit-architecture-system ladder with ease and confidence. This section describes these challenges so as to justify the techniques that follow in subsequent sections.

A. Device-Level Challenges

Active and passive devices and the interconnects tying them to one another entail issues that become only more serious as the frequency of operation enters the mmW range. Many of the issues in fact arise from the limited speed of the transistors and the limited supply voltage, both of which encourage the use of inductors or transmission lines as loads. In other words, nodes running faster than a certain frequency (e.g., roughly 15 GHz in 90-nm technology) must employ resonance. Unfortunately, the large footprint of inductors and T-lines leads to large dimensions for the building blocks and hence long high-frequency interconnects.

It is interesting to contrast the present speed and interconnect issues at 60 GHz to those encountered in the late 1990s at 5 GHz. The nMOS f_T reaches 110 GHz in the 90-nm generation—about five times that of the 0.25-μm devices used in early 5-GHz designs [29], [30]. Also, the outer dimension of inductors for 60-GHz operation (50–100 μm) is only about a factor of two smaller than that of spirals used at 5 GHz (100–200 μm).[1] In other words, the frequency of operation has scaled by a factor of 12 but the transistor speed by roughly a factor of five and the interconnect lengths by about a factor of 0.5, making the design and floor planning of the receiver much more difficult.

Another point of contrast relates to the quality factor of inductors and varactors. Well-designed symmetric spiral inductors exhibit a Q of about 10 at 5 GHz, but, according to HFSS simulations, a Q of no more than 30 at 60 GHz. For example, [28] reports a Q of 12 for 180-pH inductors at 60 GHz, and [31] a Q of 17 for 400-pH inductors at 50 GHz. Attributed to substrate loss, this saturation of Q makes the design of millimeter-wave oscillators quite difficult. Since the Q does not scale by a factor of 12 from 5 GHz to 60 GHz, the trade-offs between the phase noise, the tuning range, and the power dissipation become much more severe. Also, the Q of varactors appears to fall *below* that of inductors at millimeter-wave frequencies. For example, the measured data in [32] indicates $40 < Q < 160$ for 0.18-μm varactors at 2 GHz. Rough extrapolation therefore implies that $5 < Q < 20$ for 90-nm devices at 60 GHz.

B. On-Chip Antennas?

The short wavelength of millimeter-wave frequencies makes it possible to integrate receive and transmit antenna(s) on the chip. Integrated antennas offer significant benefits: 1) they obviate the need for expensive and lossy millimeter-wave packaging; 2) they lend themselves to differential operation, transmitting a greater power for a given voltage swing; 3) the receive and transmit paths can incorporate separate antennas to avoid the use of lossy transmit/receive switches; 4) the transmitter need not be ac-coupled to the antenna; 5) they eliminate the need for high-frequency electrostatic discharge (ESD) protection devices; 6) the antennas can serve in a beamforming array, raising the output power. The last property is particularly important because, with the low supply voltage of deep submicron devices, it is much simpler to construct a multitude of low-power transmitters than one high-power counterpart.

Unfortunately, however, on-chip antennas fabricated in standard CMOS technology with no changes to the process steps appear to suffer from a low efficiency. Since CMOS power amplifiers (PAs) too exhibit a low efficiency, the overall system efficiency may yield an impractical solution. For example, with an efficiency of 10% for the antenna and 10% for the PA, the transmitter front end would need to draw 1 W so as to transmit $+10$ dBm.

C. Modeling Challenges

Recent work on transistor modeling has been based on the measurement of fabricated devices, yielding models expressed as a black box (e.g., with S-parameters) or as a fitted physical representation with additional parasitics [37], [38]. As such, this type of model makes it exceedingly difficult to depart from the specific geometry of the fabricated devices, thereby constraining the design and layout of circuits considerably. Moreover, due to various folding and routing techniques needed to create a compact layout for a given device size, the model is not scalable. Also, measurement of MOS devices, especially those with a small width, becomes difficult at these frequencies due to errors introduced by inaccurate de-embedding from calibration structures and coupling between probes.

In order to appreciate the limitations imposed by models that are solely based on measurements, we consider a number of situations that arise in practice.

1) In a typical front end, different building blocks may require vastly different transistor geometries. For example, in the receiver reported in [7], the LNA, the RF mixer, the oscillator, and the $\div 2$ circuit employ, in the high-frequency path, transistor widths equal to 30 μm, 20 μm, 16 μm, 8 μm, 7 μm, 6 μm, 5 μm, 4 μm, and 1 μm. Model parameters extracted from a few fabricated devices would be valid for only those specific geometries, requiring extrapolation or interpolation for others—but suffering from uncertainties due to the change in the interconnects.
2) In addition to the width and number of gate fingers and the folding factor, other aspects of a transistor geometry may need to be tailored to the circuit environment. For example, the drain-source capacitance can be reduced at the cost of increasing the drain and source junction capacitances, a useful trade-off in common-gate (CG) and cascode stages. If the fabricated transistors do not include such variants, the model cannot be readily applied to these cases.

[1] At 5 GHz, stacked spirals with five to six turns were used [30] whereas at 60 GHz, it is preferable to have a single spiral with one or two turns. Thus, the outer dimensions differ by only a factor of two even the inductance values may bear a ratio of 10–15.

3) In deep-submicron technologies, most transistors are surrounded by dummy gate fingers so as to reduce mismatches resulting from the stress due to shallow trench isolation [39], [40]. The position and number of these fingers depend on the particular circuit design and layout but they affect the extrinsic connections to the device and hence its model.
4) Reliance on measurement-based models prohibits the use of additional (perhaps unrelated) interconnects *over* the transistors lest the additional couplings may not be included correctly. In complex layouts, therefore, many of the interconnects must travel *around* the transistors, suffering from unnecessary capacitance and loss.

The use of black-box S-parameter-based models in circuit simulations also faces critical issues: for complex topologies, the simulator may not converge; different interpolation methods used to handle the discrete S-parameter values yield different results; and, most importantly, S-parameters are obtained at certain bias conditions and hence cannot represent the behavior of large-signal circuits such as mixers, oscillators, dividers, and power amplifiers. A number of modeling techniques for mmW design are introduced in [41].

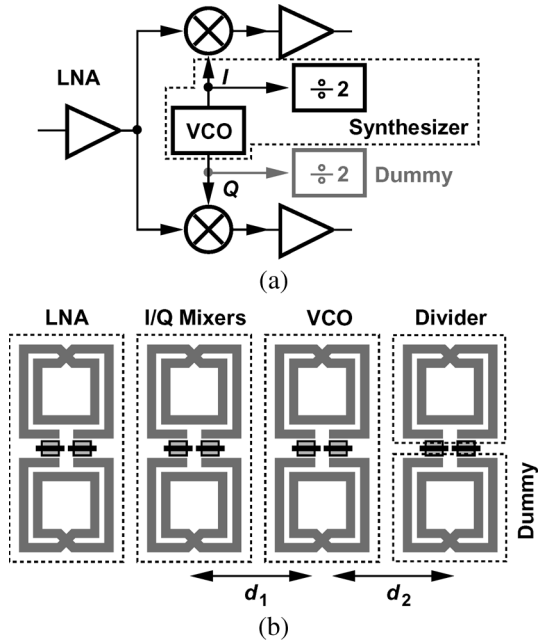


Fig. 1. (a) Direct-conversion receiver and (b) its floor plan.

D. Architecture-Level Challenges

The integration challenges that arise from limited transistor speeds and long interconnects manifest themselves in three critical tasks related to the local oscillator (LO): (1) LO (I/Q) generation; (2) LO frequency division, and (3) LO distribution. To illustrate these challenges, we consider a direct-conversion receiver architecture as a candidate. Shown in Fig. 1 along with its floor plan, such an architecture incorporates at least two inductors in the LNA, one in each mixer, two in the quadrature voltage-controlled oscillator (VCO), and at least one in the frequency divider. The dummy divider serves to maintain the balance between the I and Q outputs. The generation of I and Q phases of the LO at 60 GHz entails two issues: (a) quadrature operation typically degrades the phase noise considerably (Appendix B) and (b) for reasons mentioned above, the comparatively low tank Q results in serious design trade-offs.

The second task, namely, LO frequency division, also proves problematic in this architecture. The design of high-speed dividers that satisfy various environmental demands in a transceiver poses its own challenges (Section V).

The problem of LO distribution is apparent from the floor plan of Fig. 1(b). The quadrature outputs of the VCO must travel a distance of d_1 to reach the I/Q mixer cores and d_2 to reach the divider cores, thus experiencing significant loss and mismatch. In fact, with no buffer following the VCO, the loss of these interconnects also degrades the phase noise.

One may wonder if these interconnects can be realized as low-loss T-lines having a controlled impedance and terminated properly at the destination. Since the characteristic impedance of on-chip T-lines hardly exceeds a few hundred ohms, such an approach would *load* the VCO with a low resistive component, drastically raising the phase noise or even prohibiting oscillation. A buffer must therefore follow the VCO in this case.

The use of a VCO buffer is also required by another effect: in a direct-conversion receiver, strong in-band interferers can leak from the RF to the LO port of the downconversion mixers, thus injection-pulling the LO in the absence of a buffer. However, the use of a quadrature buffer in the architecture of Fig. 1 translates to two additional inductors and much greater difficulty in floor planning.

The analog baseband processing, too, presents many challenges. Since the RX and TX baseband chains must accommodate a bandwidth of about 800 MHz, the filters and A/D and D/A converters become difficult to design, especially if the modulation scheme poses its own linearity requirements. Extrapolation from ultra-wideband and wireless local-area-network transceivers suggests that data converters with resolutions on the order of 6 to 8 bits and sampling rates of around 2 GHz will be necessary.

V. Circuit and Device Techniques

The performance envelope of CMOS radios has been pushed to the mmW range through innovations at all abstraction levels. In this section, we describe examples of circuit and device techniques employed in our recent work [1], [7], [23]. As with the architecture-level issues illustrated in Fig. 1, we will also observe the inextricable link between circuit design and layout. The simulation results presented for these building blocks are based on device models extracted from electromagnetic simulations in Ansoft's HFSS. The details of this modeling methodology are described in [41]. A comparison of performance of various building blocks reported in the literature is provided in [42].

A. Low-Noise Amplifiers

A common-gate topology employing resonance at its input and output nodes can serve as a low-noise amplifier. Fig. 2 shows an example, where the 150-pH inductors are realized as folded microstrip lines [1]. Simulations indicate a noise figure

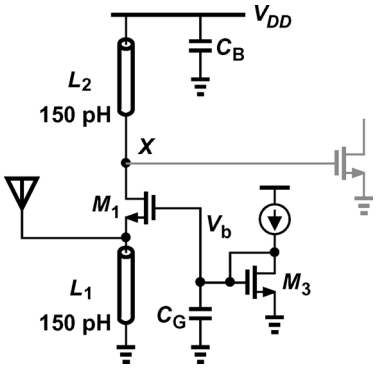


Fig. 2. Common-gate LNA.

of 4.5 dB and a voltage gain of 12 dB with a supply current of 4 mA at 60 GHz.

While considered to provide robust input matching and gain in RF design, the CG LNA of Fig. 2 faces two serious issues at very high frequencies and in deep submicron technology. First, the gate of the input transistor must see a very low-impedance return path to ground so as to avoid degrading the input match and the gain. For example, if C_G and its connections to the gate and to ground exhibit a parasitic inductance of 20 pH, an impedance of about $7j\ \Omega$ appears in series with the gate. Moreover, for the impedance of C_G to remain below, say, 5 Ω at 60 GHz, C_G must exceed 0.5 pF, requiring large dimensions. Unfortunately, the footprints of L_1 and L_2 inevitably lead to long interconnects from C_G to the gate and/or ground. Similar observations apply to the supply bypass capacitor C_B in Fig. 2, but in this case, the interconnect inductance can be absorbed by L_2.

The second issue in CG LNAs manifests itself as the intrinsic gain of transistors continues to decline in deep submicron technologies. As shown in Appendix A, the voltage gain of the circuit is bounded by the following expression:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{(g_m + g_{mb})r_O + 1}{2(1 + r_O/R_1)} \tag{1}$$

if the input remains matched to a source impedance of R_S. Here, R_1 denotes the equivalent parallel resistance of the drain tank at resonance. Thus, with $(g_m + g_{mb})r_O < 10$ and $R_1 \approx r_O$, the voltage gain hardly exceeds 2.5.

In view of the foregoing shortcomings of the CG LNA, one may consider the inductively-degenerated cascode topology, known for its low noise figure at lower frequencies but also the dependence of its input matching upon package parasitics. Depicted in Fig. 3(a), such an LNA can operate in the mmW range only if all of the inductors are integrated on the chip and the ground return paths for L_1 and L_2 display very low inductance. This can be accomplished by "nesting" L_1 and L_G [7], [43], thus localizing all of the critical connections as shown in Fig. 3(b). The magnetic coupling due to nesting alters the input matching, but it can be compensated by a slight adjustment of L_1 and L_G. Note that one terminal of L_1 is tied to the ground line located under the input signal line.

While improving the stability, the cascode device in Fig. 3(a) introduces a pole at node P, thereby adversely impacting the gain and noise figure at mmW frequencies. Since this pole is on

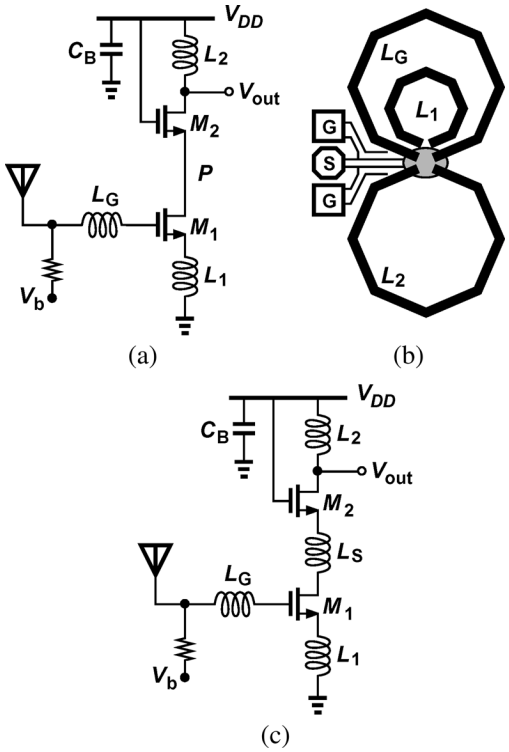


Fig. 3. (a) Cascode LNA, (b) nesting of inductors, and (c) addition of series resonance.

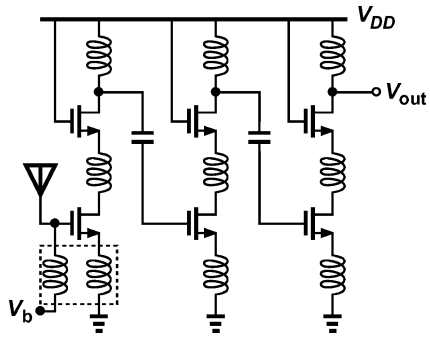


Fig. 4. LNA reported in [33].

the order of $f_T/2$, the capacitance at P both shunts a considerable portion of the RF current to ground and raises the noise contribution of M_2. This issue can be alleviated by parallel resonance [7], while facing the problem of ground return path for the dc block capacitor that must appear in series with the inductor. Alternatively, series resonance [5], [15] can be used with no need for such a capacitor [Fig. 3(c)].

Fig. 4 shows a W-band LNA designed in 65-nm technology [33]. Employing transformer feedback at the input to allow optimization for input matching and noise figure [34], the circuit consists of three cascode stages with series peaking at the cascode nodes. According to simulations, the LNA provides a noise figure of 7 dB and a gain of 17 dB while drawing a supply current of 24 mA [33].

B. Mixers

At mmW frequencies, a passive mixer followed by an IF amplifier can be designed to achieve roughly the same noise figure

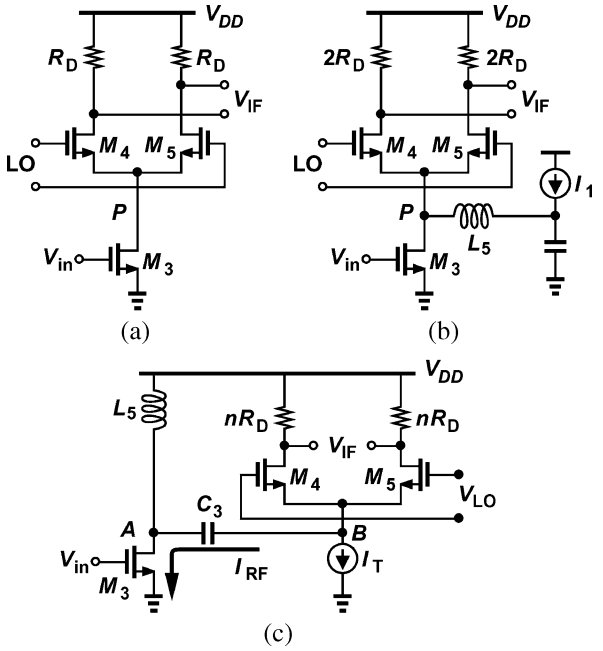


Fig. 5. (a) Conventional active mixer, (b) active mixer using resonance and auxiliary current path, and (c) active topology with capacitive coupling.

and conversion gain as an active topology does [7]. However, such a passive realization suffers from a lower input impedance than does the active mixer, heavily loading the LNA.

Fig. 5(a) shows the conventional active mixer topology. According to simulations, this circuit exhibits a noise figure of 26 dB and a conversion gain of 0 dB at an input of 60 GHz. Several mechanisms account for this poor performance. First, the total capacitance at the drain of M_3 gives rise to a pole on the order of $f_T/2$. Second, since M_4 and M_5 must carry the entire bias current of M_3, they switch quite gradually, inject noise to the output, and "waste" part of the RF current as a common-mode component. Third, the limited supply voltage allows only a small voltage drop across the load resistors and hence a low conversion gain.

To alleviate these issues, we consider the topology depicted in Fig. 5(b), where inductor L_5 resonates with the total capacitance seen at the drain of M_3 and also carries about half of the drain current of M_3 [1]. Now, most of the RF current is commutated by M_4 and M_5 because the equivalent parallel resistance of L_5 is much greater than the average resistance seen looking into the sources of the switching pair. (For the same reason, the thermal noise contributed by L_5 is negligible.) Also, carrying a smaller current, M_3 and M_4 switch more abruptly. Finally, the load resistors can be doubled. As a result, the noise figure falls to about 18 dB and the conversion gain rises to 12 dB.

Unfortunately, due to its small dimensions, transistor M_3 in Fig. 5(b) incurs a large mismatch with respect to I_1, thus creating substantial variations in the current flowing from the switching pair. The topology depicted in Fig. 5(c) [44] avoids this issue by isolating the bias current of $M_4 - M_5$ from that of the input transconductor. In this design, optimization of noise figure and gain yields $I_{D3} = 8.5$ mA whereas $I_T = 0.75$ mA, revealing that the conventional active mixer (with the switching pair carrying the same current as the input device) is far from optimum. The circuit achieves a simulated noise figure of 12.5 dB and a voltage conversion gain of 10.2 dB.

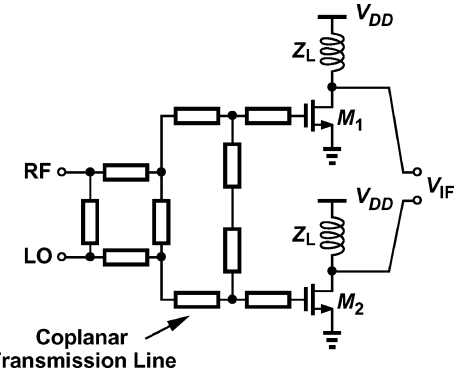


Fig. 6. Mixer reported in [2].

As a single-balanced mixer, the topology of Fig. 5(c) can produce a large LO component at the output, potentially desensitizing the IF mixers in a heterodyne chain. The use of load inductors with resonance at the IF can attenuate the LO feedthrough. Also, the small ratio of I_T/I_{D3} reduces the LO feedthrough by the same factor.

Fig. 6 depicts an alternative mixer topology [2]. Here, the LO and RF signals are combined by a passive network and subsequently applied to two common-source stages. Large-signal drive of M_1 and M_2 causes them to mix the LO and RF components, thus producing an IF current that is converted to voltage by the load Z_L. Designed in 0.13-μm technology for operation at 60 GHz, the mixer exhibits a conversion loss of 2 dB and a noise figure of 13.8 dB while consuming 2.4 mW.

C. Oscillators

As argued in Section IV, direct conversion faces three difficult issues related to the LO. In other words, the LO frequency in a, say, 60-GHz radio may lie well below 60 GHz (Section VI). Nonetheless, it is beneficial to develop high-frequency oscillators for future systems operating at hundreds of gigahertz.

The oscillators reported in the literature for operation at 60 GHz and above mostly employ a cross-coupled transistor pair with various resonator structures [4], [10], [13], [21], [45]. We describe a different technique here that has led to fundamental oscillation at 128 GHz in 90-nm CMOS technology [23]. Consider the passive fourth-order *LC* circuit shown in Fig. 7(a), where all of the components are ideal. The transfer function from the input current to the output voltage can be expressed as

$$H(s) = \frac{-L_2 s}{L_1 L_2 C_1 C_2 s^4 + [(L_1 + L_2)C_1 + L_2 C_2]\, s^2 + 1}. \quad (2)$$

For the special case $L_1 = L_2 = L$ and $C_1 = C_2 = C$, the transfer function exhibits two imaginary poles at

$$\omega_{p2,p2'} = \pm j \sqrt{\frac{3+\sqrt{5}}{2LC}}. \quad (3)$$

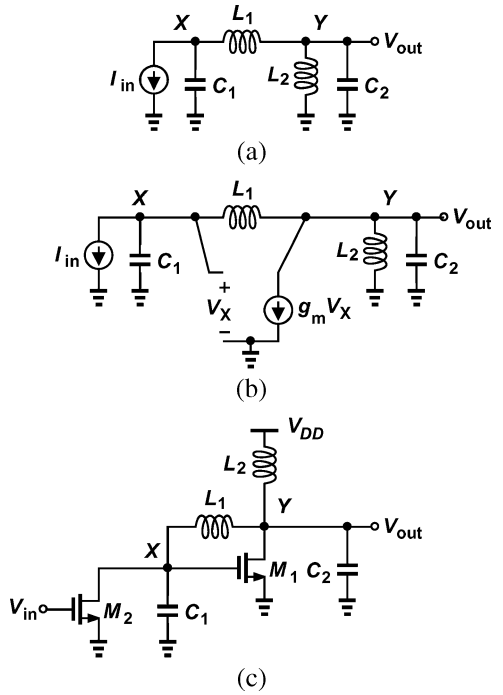


Fig. 7. (a) Fourth-order passive network, (b) addition of transistor to compensate for the loss of inductors, and (c) voltage amplifier.

The magnitude of $\omega_{p2,p2'}$ is 62% greater than the resonance frequency of second-order tanks, a critical advantage of the proposed technique.

It is possible to analyze the effect of the loss of L_1 and L_2 at ω_{p2} [23]. It can also be proved that a transistor inserted into the circuit as shown in Fig. 7(b) can compensate for this loss and place the circuit at the edge of oscillation. The required transconductance is given by

$$g_m \approx \frac{3\sqrt{5}+5}{2} \cdot \frac{1}{R} \tag{4}$$

$$\approx \frac{5.85}{R}, \tag{5}$$

where R denotes the parallel equivalent resistance of each inductor at ω_{p2}.

While theoretically capable of oscillation, the circuit of Fig. 7(b) provides gain by a single transistor, facing possible start-up failure in a manner similar to the Colpitts topology. We therefore add another voltage-to-current converting transistor at the input as shown in Fig. 7(c). It can be proved that this circuit still oscillates at ω_{p2} if the input and output are shorted and each transistor is half as wide as that in Fig. 7(b) and provides a transconductance equal to

$$g_m = \frac{3\sqrt{5}+5}{4} \cdot \frac{1}{R}, \tag{6}$$

Fig. 8 shows the resulting differential oscillator topology.

The use of several inductors in the oscillator of Fig. 8 leads to difficulties in the layout. While L_2 and L_4 can be realized as a single symmetric structure, the *floating* elements L_1 and L_3 would require long interconnects (longer than the radius of one inductor) at either X_1 and X_2 or Y_1 and Y_2. Fortunately, this

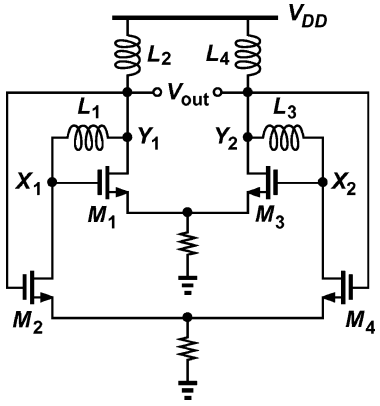


Fig. 8. Oscillator based on inductive feedback.

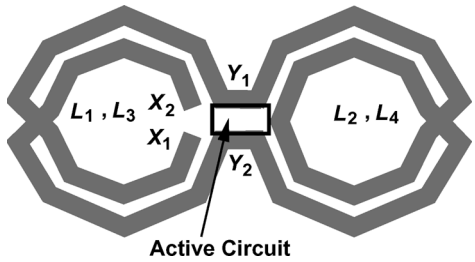


Fig. 9. Inductor geometries for oscillator.

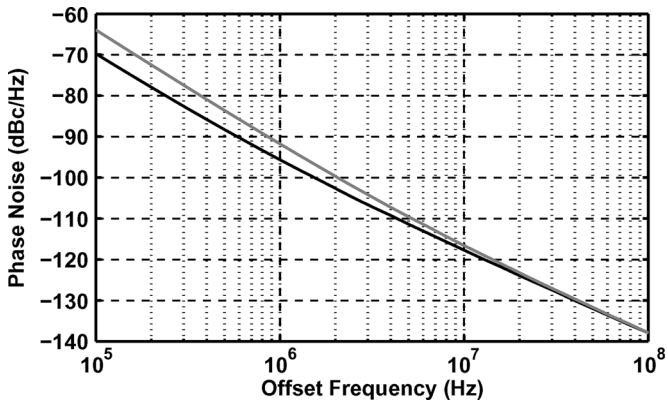


Fig. 10. Simulated phase noise of the inductive-feedback oscillator (black line) and cross-coupled oscillator (gray line).

issue can be resolved by the layout style illustrated in Fig. 9, where L_1 and L_3 also form a symmetric inductor that is broken at its point of symmetry so as to produce nodes X_1 and X_2. The four critical nodes are thus placed in close proximity of one another.

To tune the frequency, varactors must be tied from nodes X_1, X_2, Y_1, and Y_2 to the control voltage. By virtue of inductive feedback, the circuit can drive heavy capacitive loads and operate from a low supply voltage.

Fig. 10 compares the simulated phase noise of this oscillator with that of a standard cross-coupled topology at 80 GHz, assuming a given inductor design, a given power consumption, and a given buffer. Interestingly, the inductive feedback suppresses the flicker noise contribution of M_1 and M_3 to the phase noise because a low-frequency voltage perturbation in series

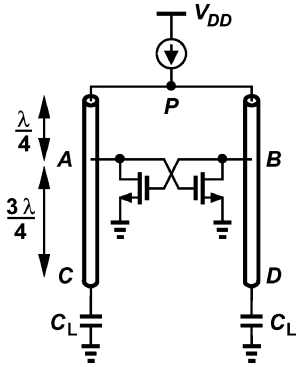


Fig. 11. Oscillator reported in [10].

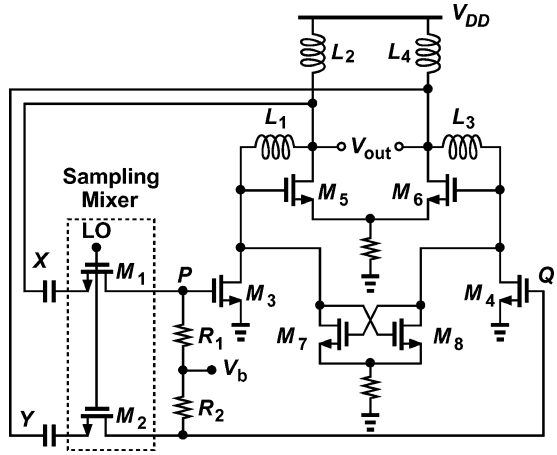


Fig. 12. Miller divider based on inductive-feedback amplifier.

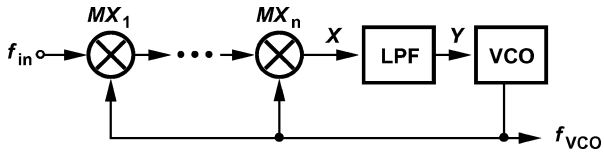


Fig. 13. Basic heterodyne PLL.

with the gate of, say, M_1, cannot change the phase difference between V_{X1} and V_{Y1}. Note that, for the new oscillator to operate at 80 GHz, it must be loaded with a much greater capacitance than the load seen by the cross-coupled topology (as indicated by the 62% speed advantage derived above).

Fig. 11 shows an oscillator that addresses the issue of load capacitance presented by subsequent stages (e.g., frequency dividers or mixers) [10]. The circuit employs two transmission lines of length equal to 3/4 of the wavelength. Differential operation establishes a short-circuit termination at node P, producing standing waves with peak swings at nodes A and B *and* at C and D. With the load capacitance, C_L, tied to the latter nodes, rather than to the former, the maximum oscillation frequency is increased substantially. Realized in 90-nm technology and used in a 75-GHz PLL, the oscillator exhibits a phase noise of -88 dBs/Hz at 100-kHz offset and consumes 8 mW [10].

D. Frequency Dividers

Divide-by-two circuits have also kept up with oscillator frequencies. Flip-flop dividers [20], injection-locked topologies [3], [22], and Miller realizations [7], [23], [25] have been reported.

Frequency dividers must maintain proper speed and lock range while satisfying many other exacting demands imposed by their environment: their input capacitance and required input swings and common-mode level must be commensurate with the oscillator's output waveform; they must drive, with sufficient swings, the input capacitance of the next stage—another divider (and IF mixers in a heterodyne receiver); and they must avoid the use of input and output buffers as such buffers would necessitate additional inductors, further complicating the distribution of signals.

The circuit technique illustrated in Fig. 7(c) can also improve the speed of frequency dividers. Shown in Fig. 12 is a Miller topology employing the inductive feedback configuration [23]. The cross-coupled pair increases the loop gain and hence the lock range. Also, M_1 and M_2 form a differential "sampling mixer," which presents less loading to the amplifier than conventional double-balanced passive mixers. Specifically, the capacitance at node P switches periodically between X and Y in a conventional mixer, thereby introducing a resistance between these two nodes and lowering the gain of the amplifier. Here, on the other hand, the voltage is simply stored on the capacitance for a half cycle (if R_1 and R_2 are sufficiently large).

The circuit of Fig. 12 achieves high speeds even in 90-nm CMOS technology. Consuming 10.5 mW, three experimental prototypes using different inductor designs exhibit the following lock ranges: 88–104 GHz, 96–111 GHz, and 117–125 GHz.

Heterodyne phase-locking is another candidate for high-speed dividers [9]. Depicted in Fig. 13 in its simplest form, a heterodyne PLL mixes the input with the VCO output n times, generating a frequency component at X given by $f_{\rm in} - nf_{\rm VCO}$. If the circuit locks, this component must be equal to zero, and $f_{\rm VCO}$ equal to $f_{\rm in}/n$. Other divide ratios can be realized by inserting dividers in the feedback loop and/or at the input ports of the mixer [9]. A prototype realized in 0.13-μm CMOS technology operates from 64 to 70 GHz while consuming 6.5 mW.

The use of consecutive mixers in a heterodyne PLL raises the possibility of false lock due to unwanted mixing products. However, it can be shown that for divide ratios up to 4, the limited VCO tuning range prohibits false lock [9].

An example of mmW static dividers is shown in Fig. 14 [35]. The circuit employs a flip-flop with class-AB clocking [36], thus achieving a lock range of 75 to 95 GHz while consuming 16 mW in 65-nm SOI technology.

E. Power Amplifiers

Efficient CMOS power amplifiers continue to challenge designers even at lower frequencies. Recent work [37], [46] employs cascaded common-source stages to deliver power levels in the range of $+10$ to $+12$ dBm at 60 GHz. Fig. 15 shows an example for operation at 77 GHz [37]. Using microstrips for both matching and loads, the PA delivers a saturated output of 6.3 dBm and draws 142 mW from a 1.2-V supply. The lack

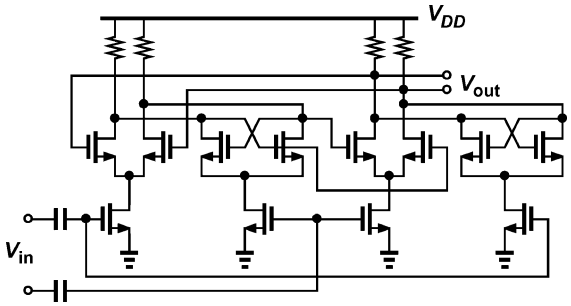


Fig. 14. Divider reported in [35].

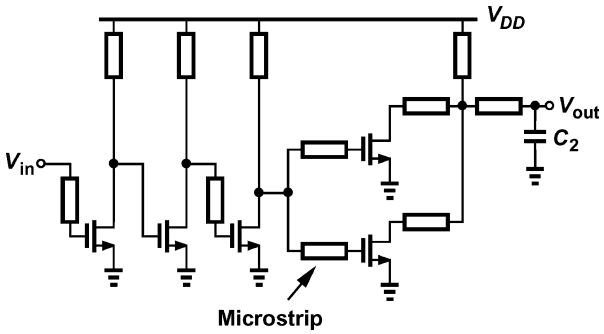


Fig. 15. PA reported in [37].

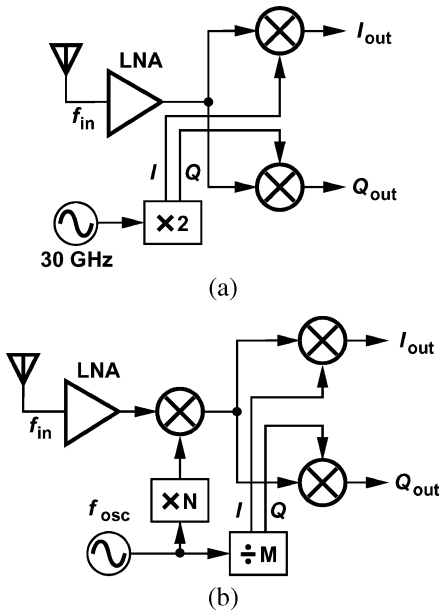


Fig. 16. (a) Direct-conversion receiver with frequency doubler. (b) Heterodyne receiver with frequency multiplier and divider.

of cascode devices, however, raises concern regarding voltage stress on the output transistors [17]. For example, in 90-nm technology, the devices begin to degrade for a terminal voltage difference of about 1.2 V, imposing a very small output swing if the drains are directly tied to $V_{\rm DD}$. As [17] indicates, if the supply voltage is reduced to 0.7 V so as to avoid voltage stress, the saturated output power falls from $+11.5$ dBm to $+8.5$ dBm and the efficiency from 8.5% to 7%.

The approach to higher efficiencies is likely to assume two paths: PA designers will continue to push the art with new circuit and device techniques, and radio architects will employ innovative beamforming methods while using small, efficient PAs.

VI. Transceiver Architectures

A. Comparison of Architectures

As mentioned in Section IV, the LO-related challenges prove so severe at millimeter-wave frequencies that the choice of architecture becomes closely intertwined with the synthesizer design. In particular, the generation of baseband I and Q signals proves a challenging task. For example, the direct-conversion receivers in [14] and [16] mix the RF signal with only one (differential) phase of the LO, generating a single baseband output. Such receivers can operate with only amplitude-modulated signals.

To ameliorate these difficulties, a direct-conversion receiver can employ a 30-GHz LO and a frequency doubler [Fig. 16(a)]. While simplifying the task of division, this approach suffers from other drawbacks: 1) CMOS doublers tend to be quite lossy at these frequencies, raising the LO noise floor, necessitating post-amplification to achieve sufficient swings, and consuming additional inductors; 2) typical doubler topologies do not produce quadrature outputs, calling for additional (lossy) quadrature separation stages; 3) the distribution of the 60-GHz quadrature phases around large layout geometries such as inductors still proves difficult.

The generation and distribution of quadrature phases can be eased by opting for a heterodyne architecture. Fig. 16(b) illustrates a general case employing $Nf_{\rm osc}$ for the first downconversion and $f_{\rm osc}/M$ for the second, thus requiring $f_{\rm osc} = f_{\rm in}M/(MN+1)$. This architecture must deal with the loss of the frequency multiplier and the problem of image rejection. For example, the receiver in [47] incorporates $N=3$ and $M=2$, placing the image at $5f_{\rm in}/7$. Thus, for $f_{\rm in}=64$ GHz, the image lies at 45.7 GHz, experiencing only some attenuation if the front end must accommodate frequencies as low as 57 GHz. For the receiver in [7], $N=1$, $M=2$, and hence $f_{\rm LO}=2f_{\rm in}/3$. Located at $f_{\rm in}/3$, the image is suppressed by the selectivity of the antenna and the RF front end. Nevertheless, $f_{\rm LO}$ is still relatively high.

The foregoing observations apply to transmitters as well. Direct upconversion entails similar issues with respect to I/Q generation (from a 60-GHz LO or a multiplier), division, and distribution. Two-step upconversion must deal with the problem of image (if the second upconversion does not employ a single-sideband mixer), which can corrupt the transmitted signal constellation, thus raising the error vector magnitude.

Fig. 17(a) shows a transceiver architecture that relaxes the LO-related issues while avoiding frequency multiplication [30]. Placing the image around zero, this approach incorporates the lowest possible LO frequency and provides a "clean" frequency plan and a compact design. This "half-RF" architecture, however, exhibits a number of drawbacks.

The first drawback relates to the third harmonic of the LO. Illustrated in Fig. 17(b) for the receive path, this effect manifests itself if an asymmetrically-modulated input is mixed with

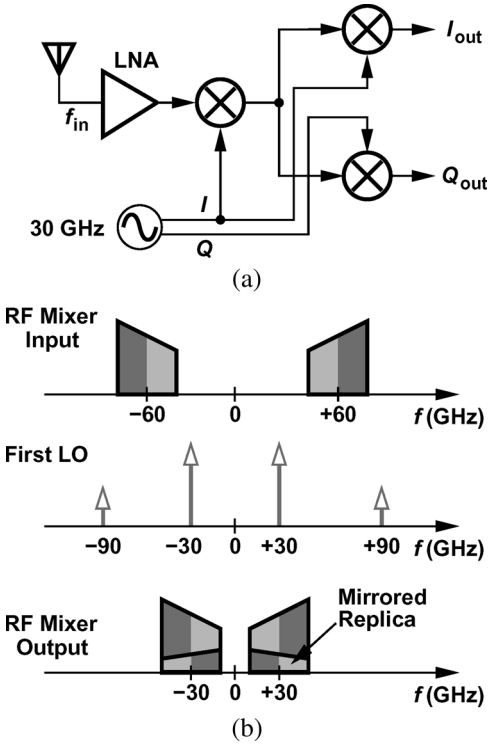


Fig. 17. (a) Half-RF heterodyne transceiver architecture and (b) receiver spectra.

$f_{\rm LO} = 30$ GHz and $3f_{\rm LO} = 90$ GHz. The latter also downconverts the signal to $f_{\rm IF} = 30$ GHz but superimposes on the desired channel its "mirrored replica," a corruption that cannot be undone by subsequent stages. A similar phenomenon occurs in a half-RF transmitter. Since hard switching in the mixers inevitably yields a third harmonic for the LO, and since most modulation schemes exhibit asymmetric spectra, this phenomenon proves serious.

The effect of the third harmonic can also be expressed analytically. Writing a general bandpass signal as $x_{\rm RF}(t) = {\rm Re}\{x_{\rm BB}(t)\exp(+j\omega_{\rm RF}t)\}$, where $x_{\rm BB}(t)$ denotes the baseband signal, multiplying it by an LO waveform approximated by $\cos\omega_{LO}t + \alpha\cos 3\omega_{\rm LO}t$, and translating the IF signal to baseband, we obtain [48]

$$x_{\rm BB,I}(t) = {\rm Re}\left\{x_{\rm BB}(t) + \alpha x^*_{\rm BB}(t)\right\} \quad (7)$$
$$= (1+\alpha){\rm Re}\left\{x_{\rm BB}(t)\right\} \quad (8)$$
$$x_{\rm BB,Q}(t) = {\rm Im}\left\{x_{\rm BB}(t) + \alpha x^*_{\rm BB}(t)\right\} \quad (9)$$
$$= (1-\alpha){\rm Im}\left\{x_{\rm BB}(t)\right\}. \quad (10)$$

The factors $1+\alpha$ and $1-\alpha$ can be viewed as an I/Q gain mismatch of $(1+\alpha)/(1-\alpha) = 2$ for $\alpha = 1/3$. This 6-dB mismatch proves difficult to correct in the analog domain (due to nonlinearity and noise issues) or in the digital domain (due to the additional dynamic range required of the baseband analog-to-digital converters). Similar observations apply to the transmit path as well.

Another drawback of the half-RF receiver shown in Fig. 17(a) stems from the inevitable result that the first IF is equal to $f_{\rm LO}$. Thus, the LO-IF feedthrough of the RF mixer cannot be filtered, potentially desensitizing the IF mixers. This issue makes it difficult to utilize a single-balanced RF mixer, which is the preferred choice if the LNA is single-ended. The next section presents a modified version of this architecture that alleviates these issues.

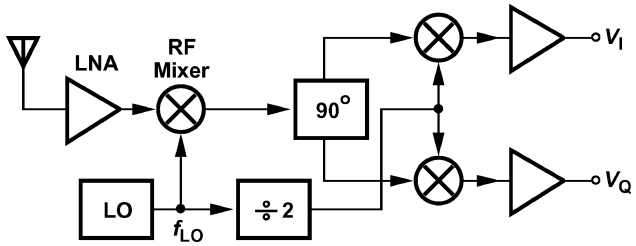


Fig. 18. RX architecture using $f_{LO} = 2f_{\rm in}/3$.

B. Architecture Examples

Fig. 18 depicts the receiver architecture used in [7]. In a manner similar to that in [49], the receiver mixes the input with a nominal LO frequency of 40 GHz, generating an IF of 20 GHz. The IF signal is then separated to quadrature phases and mixed with $f_{\rm LO}/2$ to produce the baseband outputs. With $f_{\rm LO} = (2/3)f_{\rm in}$, an input band of B requires an LO range of $(2/3)B$. Also, the image bandwidth is equal to $B/3$. [It can be proved that if $f_{\rm LO} = \alpha f_{\rm in}$, then the image bandwidth is equal to $(2\alpha - 1)B$.]

The heterodyne architecture of Fig. 18 greatly simplifies the three LO-related tasks mentioned in Section IV: 1) generation occurs at 40 GHz with no need for quadrature phases; 2) frequency division also occurs at 40 GHz, permitting a broadband design; and 3) distribution of the differential 40-GHz LO is much simpler than that of quadrature 60-GHz components. Note that no LO buffer is necessary as interferers in the vicinity of 40 GHz are suppressed by the selectivity of the front-end (including the antenna).

Unlike typical designs, the receiver performs quadrature separation in the signal path rather than in the LO path. This choice eases the design of the 40-GHz divide-by-two circuit, hence lowering the risk to the operation of the overall receiver. It is possible to divide $f_{\rm LO}$ by four and drive the IF mixers with the resulting components [50]. This approach, however, places the image closer to the signal, yielding a lower image rejection ratio and possibly raising the noise figure due to the downconversion of the noise in the image band. Similarly, in a transmitter, the upconverted image would be relatively close to the signal, corrupting the output.

Fig. 19 shows another receiver example [2], wherein $f_{\rm osc} = 29$ GHz and $N = 2$, producing an IF of 2 GHz. (To produce quadrature baseband signals, the IF would need to be mixed with the quadrature phases of a 2-GHz oscillator.) In this architecture, the small difference between $f_{\rm RF}$ and $f_{\rm LO} = 2f_{\rm osc}$ leads to an *in-band* image. Consequently, the image thermal noise generated by the antenna, the LNA and the input stage of the mixer is downconverted to the IF, raising the RX noise figure by about 3 dB. (For this reason, low-IF receivers employ some means of image rejection, which also requires quadrature LO phases and faces the architecture-level challenges described in Section IV-D.)

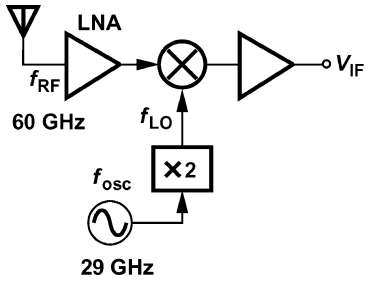


Fig. 19. Receiver reported in [2].

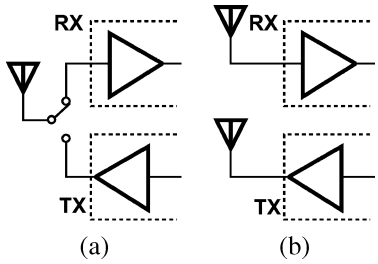


Fig. 21. Interface between transceiver and antenna(s) (a) using a T/R switch and (b) using dedicated antennas.

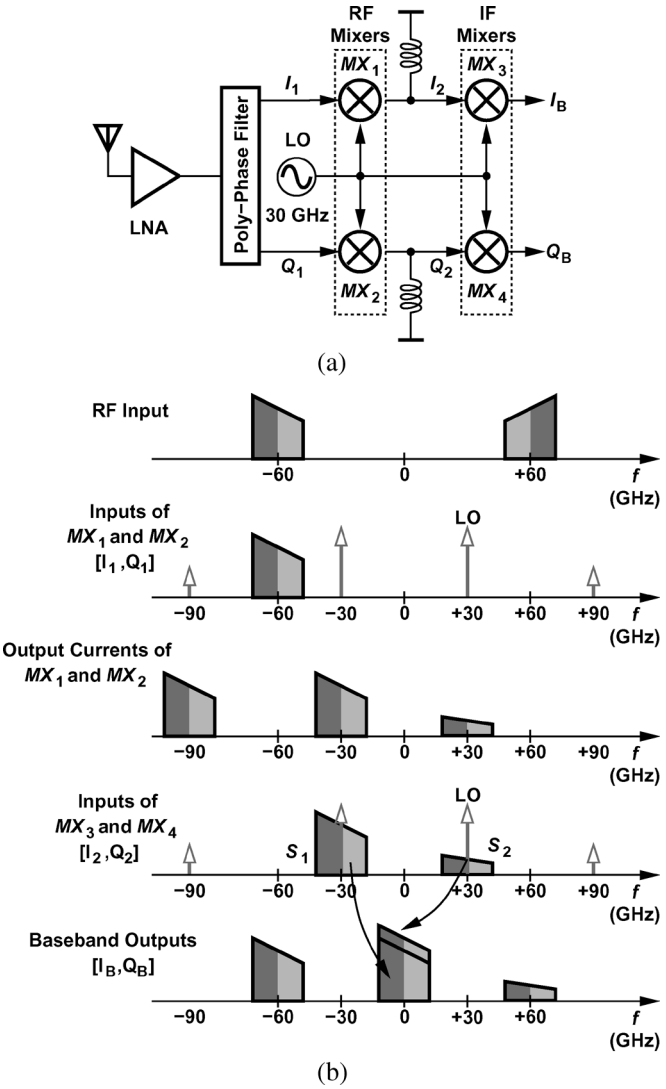


Fig. 20. (a) Modified half-RF RX. (b) Spectra along the RX chain.

Fig. 20(a) shows a modified half-RF architecture [15]. In order to avoid the mirrored replica effect illustrated in Fig. 17, this architecture eliminates the positive or negative part of the RF signal spectrum. Here, the mixing of the RF signal with $3f_{\rm LO}$ does produce a 30-GHz replica at IF, but the replica is not mirrored with respect to the desired IF signal. The input is applied to an LNA and subsequently a polyphase filter (PPF) so as to create a complex signal having negative (or positive) frequency content. The one-sided spectrum is then downconverted twice using mixers that are driven by a real (rather than quadrature) 30-GHz LO.

Fig. 20(b) illustrates the signal spectra at different points along the receiver. The one-sided spectrum at the inputs of MX_1 and MX_2 is mixed with $f_{\rm LO}$ and $3f_{\rm LO}$, generating replicas at -30 GHz, -90 GHz, and $+30$ GHz in the output currents of the two mixers. The bandpass loads of MX_1 and MX_2 suppress the -90-GHz component, applying only S_1 and S_2 to the IF mixers. Upon downconversion to baseband, S_2 constructively adds to S_1.

The one-sided spectrum assumed for the RF signal in the above analysis occurs only in the absence of mismatches. It can be shown that, with a gain mismatch of $\Delta A/A$ and a phase mismatch of $\Delta\theta$, the ratio of the mirrored replica to the desired signal is given by:

$$\left|\frac{x^*_{BB}}{x_{BB}}\right| = \left|\frac{\left(1+\frac{\Delta A}{A}\right)e^{j\Delta\theta}-1}{\left(1+\frac{\Delta A}{A}\right)e^{j\Delta\theta}+1}\right| \tag{11}$$

which is identical to the image-rejection ratio (IRR) of image-reject receivers. In other words, the proposed architecture attenuates the mirrored replica by a factor equal to IRR.

VII. T/R Switch, Beamforming, and Packaging

Following our bottom-up study in the previous sections, we now address several issues at a higher abstraction level. First, how should the RX and TX interface with an off-chip antenna? The use of a transmit/receive (T/R) switch [Fig. 21(a)] allows sharing a single antenna, but the switch parasitics and voltage stress severely degrade the performance at mmW frequencies. Alternatively, the RX and TX paths can incorporate dedicated antennas [Fig. 21(b)] but at the cost of a larger form factor. It may be possible to choose the spacing between the two antennas smaller than a quarter of wavelength so long as their mutual coupling negligibly alters or is utilized in defining their impedance.

The next issue relates to the use of multiple transceivers and antennas for beamforming. For up to four transceivers, one can envision that each side or corner of the chip carries one set of mmW input/output (I/O) signals. (To avoid a T/R switch, four "double" antennas must be placed at the corners.) For larger arrays, however, the distribution of signals becomes much more difficult. For example, a 4×4 array requires routing four sets of I/O signals from each side of the chip to four antennas [Fig. 22(a)]. With the quarter-wavelength spacing necessary

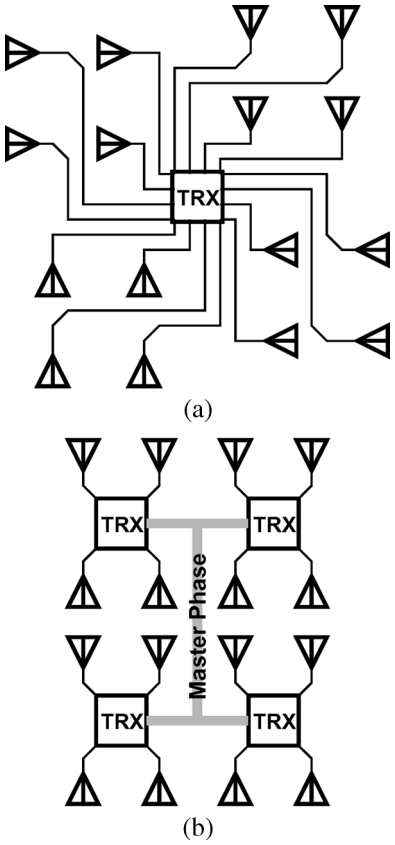


Fig. 22. Beamforming arrray using (a) one or (b) four transceiver chips.

between adjacent antennas, such a configuration entails very long and *unequal* interconnects and suffers from a high loss and considerable coupling. Fig. 22(b) shows a more practical partitioning, where four TRX chips drive a 4×4 array with short, equal interconnects and minimal coupling. In this case, however, a master LO phase must be distributed among the four chips, or oscillators with very low jitter must be included on each chip and phase-locked to a single reference with minimal path mismatch. (Jitter differences among the oscillators can smear the signal constellation in beamforming.)

The packaging of the foregoing systems will also present formidable challenges. It is expected that the antennas are printed on a low-loss substrate and each TRX is flip-bonded to the substarte so as to avoid bond wires. The complexity of such a system encourages antenna-package-transceiver co-design to achieve a high overall performance.

VIII. Conclusion

Millimeter-wave CMOS radio research continues to offer a fertile ground for innovation. A number of circuit and architecture techniques have been described in this paper that ameliorate the challenges in mmW design, but many issues still remain. Systematic modeling of the devices, methodologies for simulation of large transceivers and their layouts, coupling among various building blocks through the power lines and the substrate, packaging, antennas, transmit/receive switches, and high-efficiency power amplifiers are among critical tasks that must be addressed.

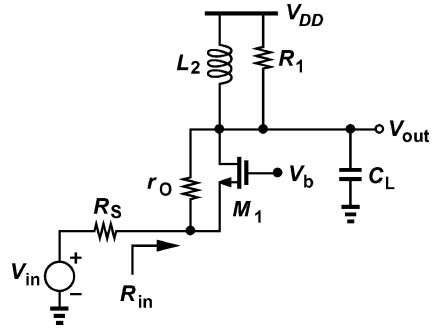


Fig. 23. Effect of transistor output impedance on CG stage.

Appendix A

In the presence of channel-length modulation, the input impedance of a common-gate stage heavily depends on the load impedance. For the CG stage shown in Fig. 23, we have

$$R_{\text{in}} = \frac{R_1 + r_O}{1 + (g_m + g_{mb})r_O} \tag{12}$$

where R_1 denotes the equivalent parallel resistance of the tank at resonance. Also, the voltage gain is given by [51]

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{(g_m + g_{mb})r_O + 1}{r_O + (g_m + g_{mb})r_O R_S + R_S + R_1} R_1. \tag{13}$$

Equating R_{in} to the antenna resistance, R_S, yields

$$R_S + (g_m + g_{mb})r_O R_S = R_1 + r_O \tag{14}$$

which can be substituted in (13) to obtain

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{(g_m + g_{mb})r_O + 1}{2(1 + r_O/R_1)}. \tag{15}$$

This result reveals a fundamental limit: for, say, $R_1 \approx r_O$, the gain is on the order of $[(g_m + g_{mb})r_O + 1]/4$, i.e., roughly one-fourth of the transistor intrinsic gain. With the low intrinsic gain of deep-submicron devices, it becomes increasingly difficult to achieve a reasonable voltage gain while ensuring input matching.

Appendix B

Quadrature oscillators suffer from a higher phase noise than their non-quadrature counterparts. Consider the coupled oscillators shown in Fig. 24. We measure the phase noise in two configurations: (1) with "anti-phase" coupling so that the two oscillate in quadrature, and (2) with "in-phase" coupling so that the two operate in phase (as if two oscillators are placed in parallel). Consuming equal powers and running at nearly equal frequencies, the two configurations permit a fair comparison of the phase noise.

Fig. 25 plots the simulated phase noise for operation at $f_{osc} = 60$ GHz with a tank Q of 15, a tail current of 1 mA, and a coupling factor of 25%. The quadrature configuration exhibits a higher phase noise for offsets up to tens of megahertz. According to simulations, 60% of the phase noise at 1-MHz offset arises from the flicker noise of the coupling transistors in the quadrature configuration. By contrast, 50% of the in-phase configuration's phase noise at 1-MHz offset is due to the thermal

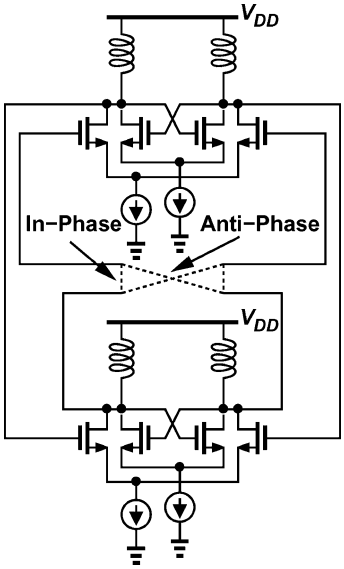


Fig. 24. Two oscillators coupled to operate in quadrature or in phase.

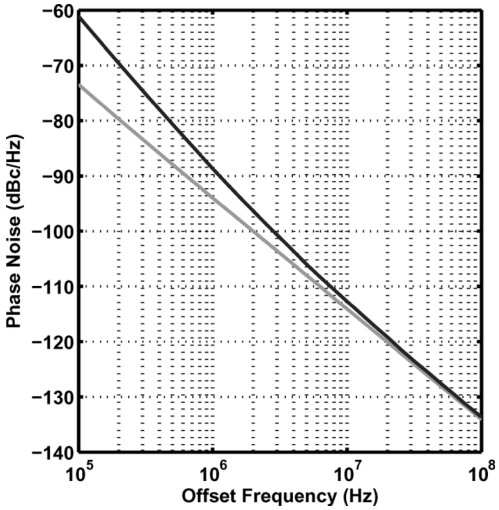


Fig. 25. Simulated phase noise of oscillators in quadrature operation (black line) and in-phase operation (gray line).

noise of the tanks and another 22% due to the thermal noise of the cross-coupled transistors.

ACKNOWLEDGMENT

Chip fabrication was provided by TSMC.

REFERENCES

[1] B. Razavi, "A 60-GHz direct-conversion CMOS receiver," in *ISSCC Dig. Tech. Papers*, Feb. 2005, pp. 400–401.

[2] S. Emami, C. H. Doan, A. M. Niknejad, and R. W. Broderson, "A 60-GHz downconverting CMOS single-gate mixer," in *RFIC Dig. Tech. Papers*, Jun. 2005, pp. 163–166.

[3] K. Yamamoto and M. Fujishima, "70-GHz CMOS harmonic injection-locked divider," in *ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 600–601.

[4] D. Huang, W. Hant, N.-Y. Wang, T. W. Ku, Q. Gu, R. Wong, and M.-C. F. Chang, "A 60 GHz CMOS VCO using on-chip resonator with embedded artificial dielectric for size, loss, and noise reduction," in *ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 314–315.

[5] T. Yao, M. Gordon, K. Yau, M. T. Yang, S. P. Voinigescu, and , "60-GHz PA and LNA in 90-nm RF CMOS," in *RFIC Dig. Tech. Papers*, Jun. 2006, pp. 147–150.

[6] P. Mayr, C. Weyers, and U. Langmann, "90 GHz 65 nm CMOS injection-locked frequency divider," in *ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 198–199.

[7] B. Razavi, "A millimeter-wave CMOS heterodyne receiver with on-chip LO and divider," in *ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 188–189.

[8] S. Emami, C. H. Doan, A. M. Niknejad, R. W. Broderson, and , "A highly-integrated 60-GHz CMOS front-end receiver," in *ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 190–191.

[9] B. Razavi, "Heterodyne phase locking: A technique for high-frequency division," in *ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 428–429.

[10] J. Lee, "A 75-GHz PLL in 90-nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 432–433.

[11] B. Heydari, M. Bohsali, E. Adabi, A. M. Niknejad, and , "Low-power mm-wave components up to 104 GHz in 90-nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 200–201.

[12] B. Martineau, A. Cathelin, F. Danneville, A. Kaiser, G. Dambrine, S. Lepilliet, F. Gianesello, and D. Belot, "80-GHz low-noise amplifiers in 65-nm CMOS SOI," in *Proc. ESSCIRC*, Sep. 2007, pp. 348–351.

[13] K. Ishibashi, M. Motoyoshi, N. Kobayashi, and M. Fujishima, "76-GHz CMOS VCO with 7% frequency tuning range," in *VLSI Circuits Symp. Dig. Tech. Papers*, Jun. 2007, pp. 176–177.

[14] T. Mitomo, R. Fujimoto, N. Ono, R. Tachibana, H. Hoshino, Y. Yoshihara, Y. Tstustumi, and I. Seto, "A 60-GHz CMOS receiver with frequency synthesizer," in *VLSI Symp. Dig. Tech. Papers*, Jun. 2007, pp. 172–173.

[15] A. Parsa and B. Razavi, "A 60-GHz CMOS receiver using a 30-GHz LO," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 190–191.

[16] B. Afshar, Y. Wang, and A. M. Niknejad, "A robust 24-mW 60-GHz receiver in 90 nm standard CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 182–183.

[17] M. Tanomura, Y. Hamada, S. Kishimoto, M. Ito, N. Orihashi, K. Maruhashi, and H. Shimawaki, "TX and RX front ends for the 60-GHz band in 90 nm standard bulk CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 558–559.

[18] E. Laskin, M. Khanpour, R. Aroca, K.-W. Tang, P. Garcia, S. Voinigescu, and , "A 95 GHz receiver with fundamental-frequency VCO and static frequency divider in 65 nm digital CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 180–181.

[19] C. Weyers, P. Mayr, J. W. Kunze, and U. Langmann, "A 22.3 dB voltage gain 6.1 dB NF 60 GHz LNA in 65 nm CMOS with differential output," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 192–193.

[20] D. D. Kim, J. Kim, and C. Cho, "A 94 GHz locking hysteresis-assisted and tunable CML static divider in 65 nm SOI CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 460–461.

[21] E. Seok, C. Cao, D. Shim, D. Arenas, D. Tanner, C.-M. Hung, and K. K. O, "A 410 GHz CMOS push-push oscillator with an on-chip patch antenna," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 472–473.

[22] K.-H. Tsai, L.-C. Cho, J.-H. Wu, and S.-I. Liu, "3.5 mW W-band frequency divider with wide locking range in 90 nm CMOS technology," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 466–467.

[23] B. Razavi, "A millimeter-wave circuit technique," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2090–2098, Sep. 2008.

[24] H. Wang, "A 50-GHz VCO in 0.25- μm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2001, pp. 372–373.

[25] J. Lee and B. Razavi, "A 40-GHz frequency divider in 0.18-um CMOS technology," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2003, pp. 259–262.

[26] M. Tiebout, H.-D. Wohlmuth, and W. Simburger, "A 1-V 51-GHz fully-integrated VCO in 0.12-um CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2002, pp. 238–239.

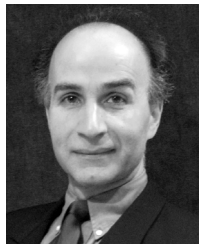
[27] L. Franca-Neto, R. Bishop, and B. Bloechel, "64 GHz and 100 GHz VCOs in 90 nm CMOS using optimum pumping method," in *ISSCC Dig. Tech. Papers*, Feb. 2004, pp. 444–445.

[28] K. Scheir, P. Wamback, Y. Rolain, and G. Vandersteen, "Design and analysis of inductors for 60 GHz applications in a digital CMOS technology," in *Proc. 69th ARFTG Microwave Measurement Conf.*, Jun. 2007.

[29] H. Samavati, H. Rategh, and T. H. Lee, "A 5-GHz CMOS wireless LAN receiver front end," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 765–772, May 2000.

[30] B. Razavi, "A 5.2-GHz CMOS receiver with 62-dB image rejection," *IEEE J. Solid-State Circuits*, vol. 36, no. 5, pp. 810–815, May 2001.

[31] T. Dickson, M. A. LaCroix, S. Boret, D. Gloria, R. Beerkens, and S. P. Voinigescu, "30–100 GHz inductors and transformers for millimeter-wave (BI)CMOS integrated circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 1, pp. 123–133, Jan. 2005.
[32] S.-S. Song, J. Han, M. Je, K. Han, and H. Shin, "RF modeling of an MOS varactor and MIM capacitor in 0.18- μm CMOS technology," *J. Korean Phys. Soc.*, vol. 41, pp. 922–926, Dec. 2002.
[33] K. W. Tang, M. Khanpour, P. Garcia, C. Garnier, and S. P. Voinigescu, "65-nm CMOS W-band receivers for imaging applications," in *Proc. CICC*, Sep. 2007, pp. 749–752.
[34] J. Bergervoet, K. Harish, G. van der Weide, D. Leenaerts, R. van de Beek, H. Waite, Y. Zhang, S. Aggarwal, C. Razzell, and R. Roovers, "An interference-robust receive chain for UWB radio in SiGe BiCMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2005, pp. 200–201.
[35] D. Kim, J. Kim, and C. Cho, "A 94-GHz locking-hysteresis-assisted and tunable CMOS static divider in 65-nm SOI CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 460–461.
[36] J. Lee and B. Razavi, "A 40-Gb/s clock and data recovery circuit in 0.18-um CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2181–2190, Dec. 2003.
[37] T. Suzuki, Y. Kawano, M. Sato, T. Hirose, and K. Joshin, "60 and 77 GHz power amplifiers in standard 90 nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 562–563.
[38] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.
[39] M. Miyamoto, H. Ohta, Y. Kumagai, Y. Sonobe, K. Ishibashi, and Y. Tainaka, "Impact of reducing STI-induced stress on layout dependence of MOSFET characteristics," *IEEE Trans. Electron Devices*, vol. 51, no. 3, pp. 440–443, Mar. 2004.
[40] P. G. Drennan, M. L. Kniffin, and D. R. Locascio, "Implications of proximity effects for analog design," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2006, pp. 169–176.
[41] C.-K. Liang and B. Razavi, "Systematic transistor and inductor modeling for millimeter-wave design," *IEEE J. Solid-State Circuits*, to be published.
[42] Cathelin, B. Martineau, N. Seller, S. Douyere, J. Gorisse, S. Pruvost, C. Raynaud, F. Gianesello, S. Montusclat, S. P. Voinigescu, A. M. Niknejad, D. Belot, and J. P. Schoellkopf, "Design for millimeter-wave applications in silicon technologies," in *Proc. ESSCIRC*, Sep. 2007, pp. 464–471.
[43] B. Razavi, "CMOS transceivers for the 60-GHz band," in *RF IC Symp. Dig. Tech. Papers*, Jun. 2006, pp. 231–234.
[44] B. Razavi, "A 900-MHz CMOS direct-conversion receiver," in *Dig. Symp. VLSI Circuits*, Jun. 1997, pp. 113–114.
[45] H.-H. Hsieh and L. H. Lu, "A 63-GHz VCO in 0.18- μm CMOS technology," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2007, pp. 178–179.
[46] D. Chowdhury, P. Reynaert, and A. Niknejad, "A 60 GHz 1 V + 12.3 dBm transformer-coupled wideband PA in 90 nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 560–561.
[47] S. K. Reynolds, B. A. Floyd, U. R. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, and M. Soyeur, "A silicon 60-GHz receiver and transmitter chipset for broadband communications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2820–2831, Dec. 2006.
[48] A. Parsa and B. Razavi, "A new transceiver architecture for the 60-GHz band," *IEEE J. Solid-State Circuits*, to be published.
[49] A. Zolfaghari, A. Y. Chan, and B. Razavi, "A 2.4-GHz 34-mW CMOS transceiver for frequency-hopping and direct-sequence applications," in *ISSCC Dig. Tech. Papers*, Feb. 2001, pp. 418–419.
[50] S. A. Sanielevici, K. R. Cioffi, B. Ahrari, P. S. Stephenson, D. L. Skoglund, and M. Zargari, "A 900-MHz transceiver chipset for two-way paging applications," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2160–2168, Dec. 1998.
[51] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2000.



Behzad Razavi (F'03) received the B.S.E.E. degree from Sharif University of Technology, Tehran, Iran, in 1985 and the M.S.E.E. and Ph.D.E.E. degrees from Stanford University, Stanford, CA, in 1988 and 1992, respectively.

He was with AT&T Bell Laboratories and Hewlett-Packard Laboratories until 1996. Since 1996, he has been Associate Professor and subsequently Professor of electrical engineering with the University of California, Los Angeles. His current research includes wireless transceivers, frequency synthesizers, phase-locking and clock recovery for high-speed data communications, and data converters. He was an Adjunct Professor with Princeton University, Princeton, NJ, from 1992 to 1994 and with Stanford University in 1995. He is the author of *Principles of Data Conversion System Design* (IEEE Press, 1995), RF MICROELECTRONICS (Prentice-Hall, 1998) (translated to Chinese, Japanese, and Korean), *Design of Analog CMOS Integrated Circuits* (McGraw-Hill, 2001) (translated to Chinese and Japanese), *Design of Integrated Circuits for Optical Communications* (McGraw-Hill, 2003), and *Fundamentals of Microelectronics* (Wiley 2006), and the editor of *Monolithic Phase-Locked Loops and Clock Recovery Circuits* (IEEE Press, 1996) and *Phase-Locking in High-Performance Systems* (IEEE Press, 2003).

Prof. Razavi is an IEEE Distinguished Lecturer. He was the recipient of the Beatrice Winner Award for Editorial Excellence at the 1994 ISSCC, the Best Paper Award at the 1994 European Solid-State Circuits Conference, the Best Panel Award at the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, and the Best Paper Award at the IEEE Custom Integrated Circuits Conference in 1998. He was the corecipient of both the Jack Kilby Outstanding Student Paper Award and the Beatrice Winner Award for Editorial Excellence at the 2001 ISSCC. He received the Lockheed Martin Excellence in Teaching Award in 2006 and the UCLA Faculty Senate Teaching Award in 2007. He was also recognized as one of the top ten authors in the 50-year history of ISSCC. He served on the Technical Program Committees of the International Solid-State Circuits Conference (ISSCC) from 1993 to 2002 and VLSI Circuits Symposium from 1998 to 2002. He has also served as Guest Editor and Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, and the *International Journal of High Speed Electronics*.