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The Low Dropout Regulator

The low-dropout (LDO) regulator is an essential power management circuit in today's systems on chip (SOCs). Much to grammarians' chagrin, the noun *regulator* has been dropped, and the circuit is simply called the *LDO*. The need for supply voltage regulation, of course, goes back many decades. Shown in Figure 1 is an example from 1969 that incorporates a pnp transistor at 28 and a feedback loop to stabilize the output voltage at 27 [1]. Similar concepts were previously implemented using vacuum tubes [2], but it was the availability of both p- and n-type semiconductor devices that paved the way for a low-voltage drop from the input to the output.

The emphasis on a low-voltage dropout began to emerge in the 1980s in automotive electronics, as microprocessors found their way into vehicles. Requiring a tightly controlled supply of $5\,\text{V} \pm 0.25\,\text{V}$, the processors had to operate with a vehicle battery voltage that would drop from 12 V to approximately 5.5 V when the ignition turned on [3]. The original LDOs were discrete circuits or relied on off-chip capacitors. Our study here focuses on fully integrated LDOs. For more details, the reader is referred to the vast literature on the subject (e.g., [4]–[7]).

The Need for LDOs

An SOC employs numerous building blocks, some sensitive to supply voltage variations and supply noise and some generating substantial noise on their supply lines because of internal switching. The question facing designers is which supply lines to share. For example, consider the standard fractional-N synthesizer shown in Figure 2, which consists of a phase/frequency detector (PFD), a charge pump (CP), a loop filter, a voltage-controlled oscillator (VCO), a divider, and a digital $\Delta\Sigma$ modulator. In such an environment, we must deal with two difficulties: 1) despite the use of off-chip and on-chip bypass (decoupling) capacitors, the external supply, $V_{DD,ext}$, still contains significant noise, and 2) the five main building blocks cannot simply share one supply line provided by the LDO because their transient currents carry various unwanted frequency components. The PFD/CP cascade experiences switching at a rate of f_{REF} but with some randomization because of the $\Delta\Sigma$ action. If shared with V_{DD3}, the PFD and CP supplies would modulate the VCO frequency, corrupting the output. Similarly, the divider and the $\Delta\Sigma$ modulator draw transient currents from V_{DD4} and V_{DD5}, respectively, that exhibit both deterministic tones and random noise. In the extreme case, conservative designers opt for five different LDOs here, especially if the source of fractional spurs is difficult to identify in simulations.

For another example, let us consider the generic successive-approximation-register (SAR) analog-to-digital converter (ADC) shown in Figure 3. The comparator, the logic, and the digital–analog converter form a feedback loop that successively updates V_{DAC} so that it approaches V_{in}. The reference generator provides a low-noise

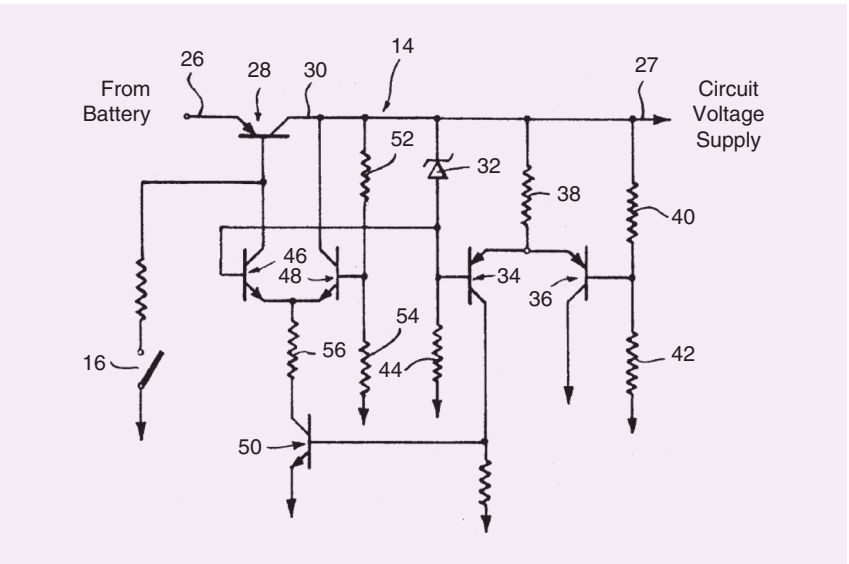

FIGURE 1: The LDO proposed by Delatorre.

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reference voltage that has a low output impedance. In this system, the transient currents drawn from V_{DD1} and V_{DD2} are a function of V_{in} and CK. That is, they carry harmonics of both V_{in} and CK. Therefore, it is difficult to share V_{DD1} and V_{DD2} or V_{DD2} and V_{DD3}.

Basic LDO Topology

The basic structure of a voltage regulator is shown in Figure 4. The unregulated, possibly noisy input, V_{in}, is applied to a pass transistor, whose current flow is controlled by the operational amplifier (op amp) A_1 such that $V_X = V_{out} R_2/(R_1 + R_2)$ remains close to V_{REF}. In today's LDO design, it is desirable to keep the dropout, $V_{in} - V_{out}$, lower than 100 mV.

In addition to the dropout, a multitude of other parameters become critical in on-chip LDOs.

1) The power-supply rejection ratio (PSRR), also known as *line regulation*, defined as $\partial V_{out}/\partial V_{in}$: This effect arises from two paths, the pass transistor and the supply of A_1.
2) Output noise, $V_{n,out}$: In the absence of input noise, the LDO itself produces noise at the output, a serious issue if, for example, the VCO in Figure 2 or the reference generator in Figure 3 is sensitive to noise in its supply voltage.
3) Load regulation, defined as $\partial V_{out}/\partial I_L$ in Figure 4: While the bias currents in the VCO of Figure 2 and the reference generator of Figure 3 are relatively constant, the transient currents in the other blocks can cause significant bounce in the LDO output voltages. This effect is directly related to the LDO's output impedance. We predict that load regulation degrades at high frequencies.
4) Power consumption and area: Both of these parameters are of concern when an SOC employs a large number of LDOs.

We should also remark that a poor phase margin (PM) associated with the LDO's feedback loop can manifest itself in some of the foregoing parameters. For example, in some frequency range, it may degrade the PSRR, introduce peaking in $V_{n,out}$, and deteriorate the load regulation.

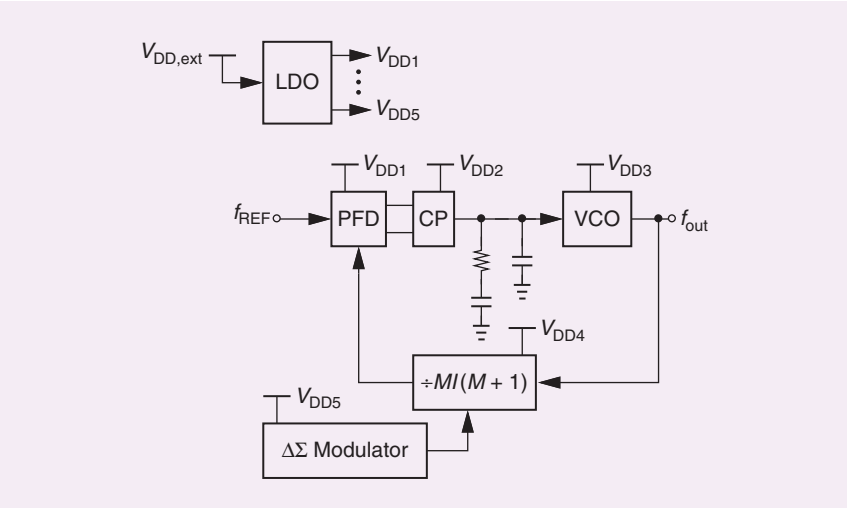

FIGURE 2: Fractional-N synthesizer.

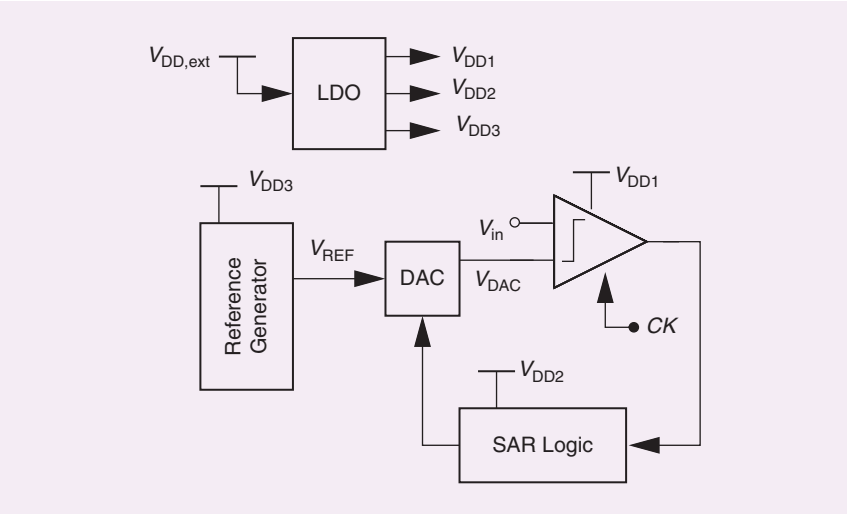

FIGURE 3: SAR ADC.

Choice of Pass Transistor

The pass transistor in Figure 4 can act as a controlled current source or as a source follower. Each choice presents its own pros and cons in terms of the dropout voltage, PSRR, load regulation, and output noise. We study these two cases in the following sections. A third possibility is to allow the pass transistor to behave as a controlled resistor, but such a choice generally proves inferior.

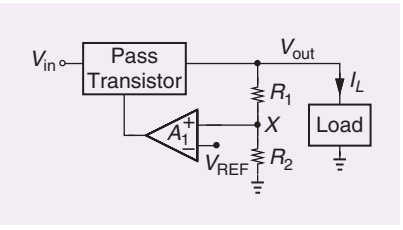

FIGURE 4: The basic LDO topology.

Pass Transistor as Current Source

Let us begin with the case in Figure 5(a), where the PMOS device, M_1, operates in the saturation region, acting as a controlled current source. The dropout, $V_{in} - V_{out}$, is equal to the source-drain voltage of M_1 and can be minimized by choosing a wide transistor. We wish to determine $\partial V_{out}/\partial V_{in}$ and $\partial V_{out}/\partial I_L$, assuming

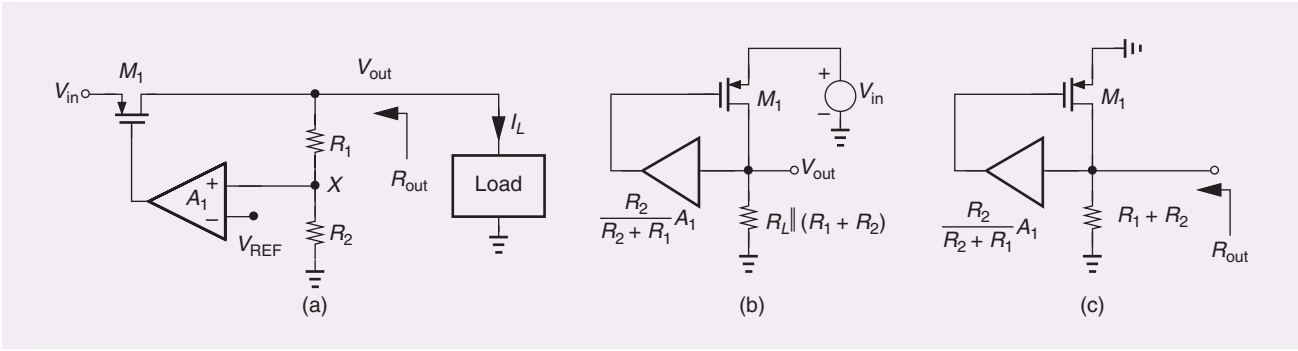

FIGURE 5: (a) The LDO using a controlled current source, (b) a model for finding PSRR, and (c) a model for finding the output resistance.

for now that op amp A_1 has infinite supply rejection. To this end, we should first compute the loop gain, A_{LG}. If we attribute a small-signal resistance, R_L, to the load, breaking the loop at X yields

$$A_{LG} = A_1 g_{m1}[R_L \| (R_1 + R_2)] \frac{R_2}{R_1 + R_2}. \quad (1)$$

The op amp equivalently boosts the transconductance of M_1.

To find $\partial V_{out}/\partial V_{in}$, we construct the small-signal model shown in Figure 5(b). Here, M_1 senses a gate-source voltage equal to $[A_1 R_2/(R_1 + R_2)]\, V_{out} - V_{in}$ and, thus, produces a small-signal current given by

$$I_{D1} = g_{m1}\left(\frac{A_1 R_2}{R_1 + R_2} V_{out} - V_{in}\right). \quad (2)$$

Upon flowing through $R_L \| (R_1 + R_2)$, this current translates to $-V_{out}$. It follows that

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}[R_L \| (R_1 + R_2)]}{1 + A_1 g_{m1}[R_2 \| (R_1 + R_2)] \frac{R_2}{R_1 + R_2}} \quad (3)$$

$$= \frac{g_{m1}[R_L \| (R_1 + R_2)]}{1 + A_{LG}}. \quad (4)$$

Of course, we can also predict this result by viewing M_1 and $R_L \| (R_1 + R_2)$ in Figure 5(b) as a common-gate stage having an open-loop gain of $g_{m1}[R_L \| (R_1 + R_2)]$, which is then placed in a negative-feedback loop and experiences a gain reduction by a factor of $1 + A_{LG}$. Typically, $A_{LG} \gg 1$, and

$$\frac{V_{out}}{V_{in}} \approx \left(1 + \frac{R_1}{R_2}\right)\frac{1}{A_1}, \quad (5)$$

suggesting that the PSRR can be improved by maximizing A_1.

For load regulation, $\partial V_{out}/\partial I_L$, we recognize that this quantity is, in fact, the output impedance of the LDO, R_{out}, in Figure 5(a). Drawing the circuit as in Figure 5(c) and observing that M_1 resembles a diode-connected device but with a transconductance boosted to $g_{m1} A_1 R_2/(R_1 + R_2)$, we have

$$R_{out} = \frac{1}{g_{m1} A_1 \frac{R_2}{R_1 + R_2}} \| (R_1 + R_2). \quad (6)$$

The first term in the parallel combination is much less than the second, yielding

$$R_{out} \approx \left(1 + \frac{R_1}{R_2}\right)\frac{1}{g_{m1} A_1}. \quad (7)$$

From the load regulation standpoint, too, we must maximize A_1.

The PMOS pass transistor in Figure 5(a) exhibits a finite output resistance, r_{O1}, allowing V_{in} to propagate to V_{out} and degrade the PSRR. This phenomenon can be viewed as simple voltage division between r_{O1} and R_{out}

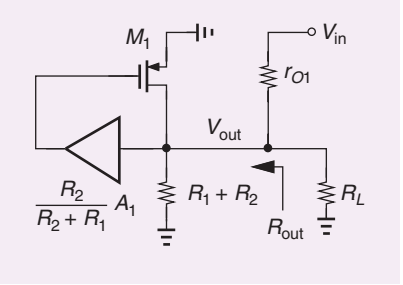

FIGURE 6: The effect of transistor output resistance on PSRR.

(Figure 6) and expressed as $V_{out}/V_{in} = R_{out}/(r_{O1} + R_{out}) = (1 + R_1/R_2)/(g_{m1} r_{O1} A_1 + 1 + R_1/R_2)$, where we have assumed $R_L \gg R_{out}$. This result is lower than that in (5) by approximately a factor of $g_{m1} r_{O1}$ and, thus, negligible.

The LDO output noise is also of interest. Modeling the noise of M_1 by a gate-referred voltage, $\overline{V_{nM}^2}$, and that of A_1 by an input-referred source, $\overline{V_{nA}^2}$ [Figure 7(a)], we note that the former can be divided by A_1^2 and placed in series with the latter [Figure 7(b)]. With a high loop gain, the circuit keeps V_X close to V_Y, producing

$$\overline{V_{n,out}^2} = \left(1 + \frac{R_1}{R_2}\right)^2 \left(\overline{V_{nA}^2} + \frac{\overline{V_{nM}^2}}{A_1^2}\right). \quad (8)$$

The contribution of M_1 is minimized by increasing A_1. Two other noise components can be readily included in this equation: that due to R_1 and R_2, modeled as $4kT(R_1 \| R_2)$, and that present in V_{REF} in Figure 5(a) (e.g., from a bandgap circuit). Both are simply added to $\overline{V_{nA}^2}$.

If V_{in} or I_L in Figure 5(a) contains high-frequency fluctuations, the results obtained previously must be revisited. Specifically, because amplifier A_1 contains at least one pole, we can replace, in the previous equations, the gain A_1 with $A_0/(1 + s/\omega_0)$, where ω_0 denotes the pole frequency. Thus, (5) changes to

$$\frac{V_{out}}{V_{in}} \approx \left(1 + \frac{R_1}{R_2}\right)\frac{1}{A_0}\left(1 + \frac{s}{\omega_0}\right), \quad (9)$$

and (7) changes to

$$Z_{out} \approx \left(1 + \frac{R_1}{R_2}\right)\frac{1}{g_{m1} A_0}\left(1 + \frac{s}{\omega_0}\right). \quad (10)$$

As sketched in Figure 8, both the PSRR and the load regulation begin to degrade beyond ω_0. Since the LDO exhibits an inductive output impedance, we also expect significant ringing at the output in the time domain if the load contains capacitive components that draw transient currents. Moreover, (8) reveals that the noise contributed by M_1 rises as $|A_1|$ falls with frequency. In summary, the seemingly low-frequency LDO calls for high-gain, broadband, low-noise op amps. For example, with $\omega_0 = 2\pi(10\,\text{MHz})$ and $A_0 = 100$, the op amp must have a gain-bandwidth product of 1 GHz.

The rising output impedance in Figure 8 indicates that high-speed switching in the load produces a large amount of noise in the LDO output voltage. This issue is ameliorated by tying a smoothing capacitance, C_M, from V_{out} in Figure 5(a) to the ground so as to provide a low-impedance path for transient currents (Figure 9). Now, $|Z_{\text{out}}|$ falls at high frequencies.

Can we avoid the peaking in $|Z_{\text{out}}|$? This would be possible if we could choose $1/(C_M\omega_0)$ approximately equal to the low-frequency impedance, $(1 + R_1/R_2)(g_{m1}A_0)^{-1}$. However, owing to the low value of the latter, C_M would need to be very large. For example, if $\omega_0 = 2\pi(10\,\text{MHz})$, $1 + \text{R}_1/\text{R}_2 = 2$, $g_{m1} = 1/(10\,\Omega)$, and $A_1 = 100$, we have $Z_{\text{out}}(\omega = 0) = 0.2\,\Omega$ and $C_M \approx 80\,\text{nF}$. With a more practical value of, for instance, 10 pF, the peak is drastically higher.

Another difficulty related to C_M in Figure 9 is that the pole formed at the output node reduces the PM. In the previously mentioned example, an 80-nF C_M places this pole near ω_0, leaving the feedback loop with two dominant poles. Although $C_M = 10\,\text{pF}$ appears benign, the op amp contains additional poles and may still suffer from PM degradation.

To investigate the issue, we first remark that M_1 in Figure 5(a) is typically a wide transistor, presenting a large gate capacitance to A_1. We break the loop, as shown in Figure 10, noting a pole at the op amp output given by $1/(C_G R_{\text{op}})$ and another at the LDO output equal to $1/\{[R_L \| (R_1 + R_2)]C_M\}$. The latter can be problematic because $R_L \| (R_1 + R_2)$ is a large resistance. Designed for a high gain, the op amp contains other poles as well, making frequency compensation difficult. This is the principal drawback of the topology.

The op amp supply rejection is another challenge, as the single-ended output of A_1 in Figure 5(a) generally changes significantly with the supply. We can quantify this effect in an LDO environment, as depicted in Figure 11(a). If A_1 generates at its output a noise voltage equal to $\beta V_{n\text{DD}}$, where β is the op amp PSRR, we can refer this quantity to the input of A_1, concluding that

$$\frac{V_{n,\text{out}}}{V_{n\text{DD}}} \approx \left(1 + \frac{R_1}{R_2}\right)\frac{\beta}{A_1}. \tag{11}$$

Thus, the op amp design must maximize β/A_1.

The preceding calculation is rather pessimistic as it assumes that V_{nDD} and the noise in V_{in} are uncorrelated. If A_1 is supplied from V_{in}, V_{nDD} is the same as the noise in V_{in}, requiring that we reexamine our derivation. As a simple example, let us implement the op amp as a five-transistor operational transconductance amplifier (OTA) and feed it from V_{in} [Figure 11(b)]. We note that 1) node P tracks V_{in} through the diode-connected device, M_c, and 2) the symmetry of the OTA topology means that V_F must remain equal to V_P, i.e., it tracks V_{in} as well. It follows that, to the first order, the gate-source voltage of M_1 does *not* change with V_{in}, a remarkable property of this LDO topology. Also, at very high input frequencies, the gate-source capacitance of M_1 bootstraps V_F to V_{in}, still maintaining a constant V_{GS} for M_1. In other words, the overall LDO supply rejection can be higher than those of the main path and the op amp.

Looking back at the regulator in Figure 1, we observe that the amplifier (transistors 48 and 46) and their

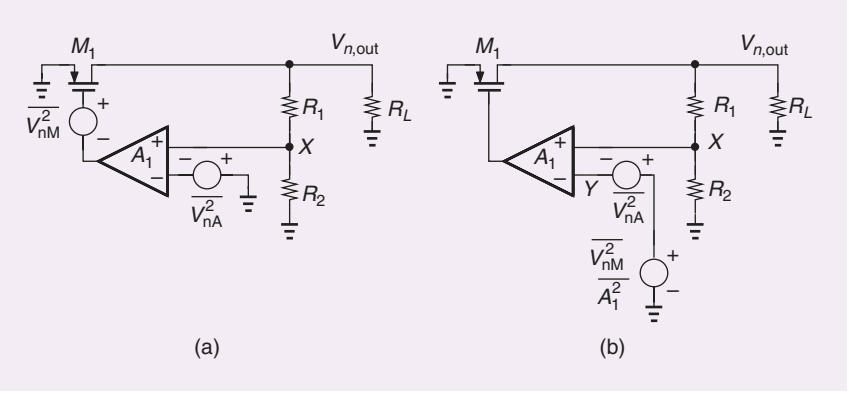

FIGURE 7: (a) The LDO circuit including noise sources and (b) the LDO with noise of M_1 referred to the op amp input.

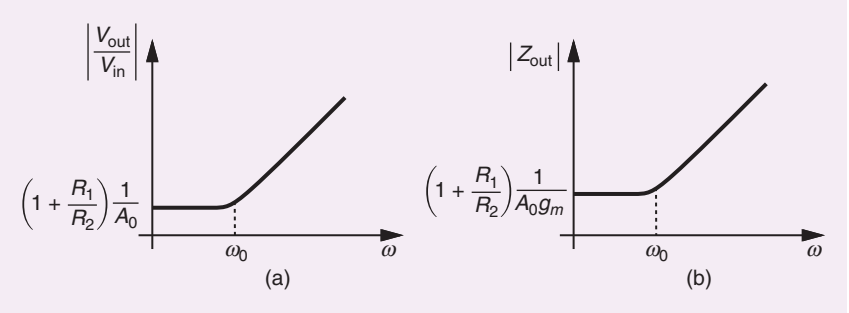

FIGURE 8: (a) The frequency behavior of an LDO PSRR and (b) the output impedance for a one-pole op amp.

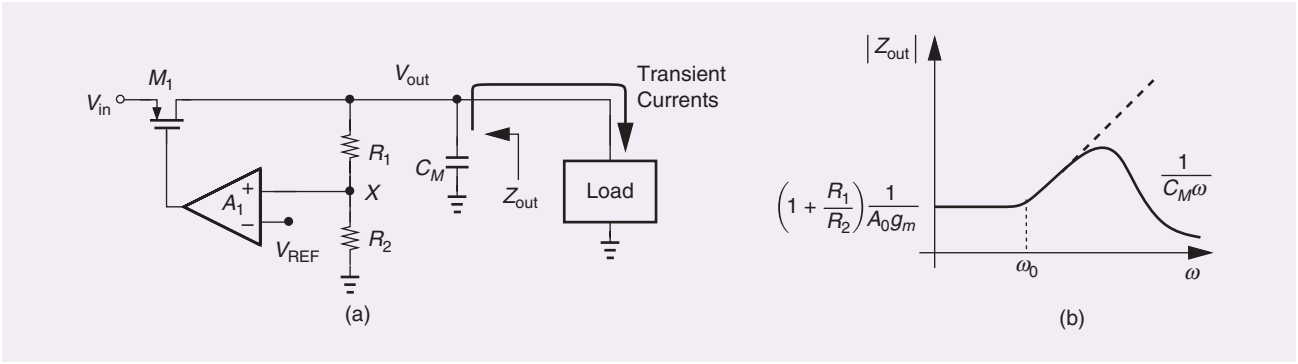

FIGURE 9: The use of a smoothing capacitor to absorb load transient currents.

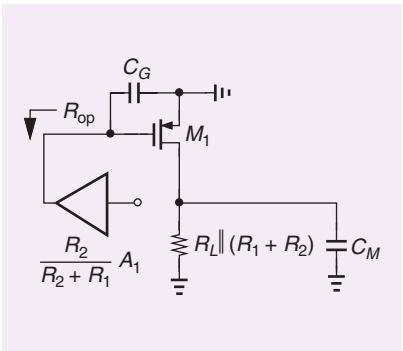

FIGURE 10: The open-loop LDO including capacitances.

bias current source (transistor 50) are supplied by the output rather than by the input. Since the output exhibits much less fluctuation, this method elegantly solves the op amp supply rejection problem.

Pass Transistor as Source Follower

Another class of LDOs employs a source follower as the pass transistor [Figure 12(a)]. One important advantage of the follower-based circuit is its superior PSRR. In fact, neglecting channel-length modulation in M_1 leads to $\partial V_{out}/\partial V_{in} \rightarrow 0$ because drain voltage changes have no effect on the source voltage for a transistor operating in saturation. This point stands in contrast to (5) for the previous LDO.

The follower in Figure 12(a) incurs a substantially greater dropout voltage than does the current source in Figure 5(a) if A_1 is supplied from V_{in}. This is because, at most, V_F can be equal to the supply voltage of A_1 and V_{out} can be equal to $V_{in} - V_{GS1}$. The key point is that the dropout includes the threshold voltage of M_1 in this case. As a remedy, a local CP can generate a higher supply voltage for the op amp [5] so that V_F is high enough to place M_1 at the edge of saturation.

We now repeat for this structure the analyses carried out in the previous section. Let us neglect the body effect of M_1 and first compute $\partial V_{out}/\partial I_L$ (i.e., the LDO output impedance). If $R_1 + R_2$ is sufficiently large and $r_{O1} = \infty$, we can simply divide the open-loop output impedance, $1/g_{m1}$, by one plus the loop gain:

$$R_{out} \approx \frac{1/g_{m1}}{1+\frac{R_2}{R_1+R_2}A_1}. \tag{12}$$

The second term in the denominator is much greater than the first, yielding

$$R_{out} \approx \left(1+\frac{R_1}{R_2}\right)\frac{1}{g_{m1}A_1}, \tag{13}$$

the same as the output impedance of the previous topology.

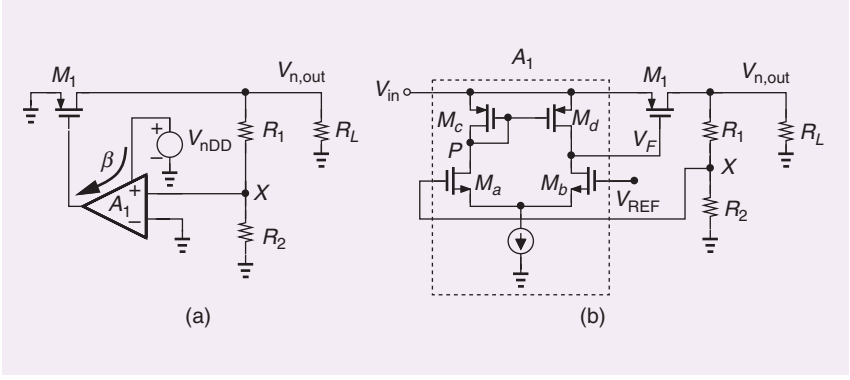

FIGURE 11: (a) The effect of op amp PSRR on the LDO PSRR and (b) the implementation example illustrating input noise cancellation.

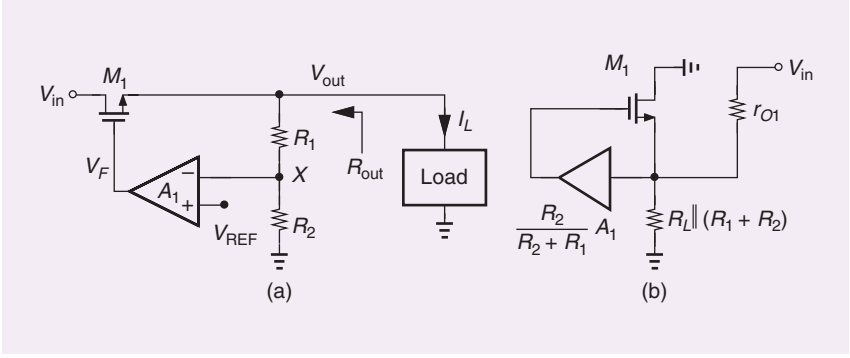

FIGURE 12: (a) The LDO using a source follower and (b) the effect of transistor output resistance on the PSRR.

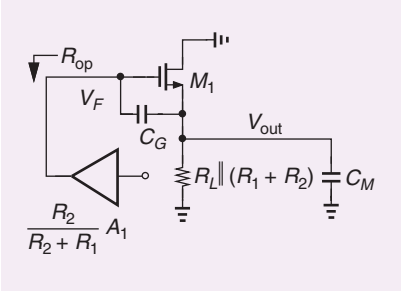

FIGURE 13: The open-loop follower-based LDO including capacitances.

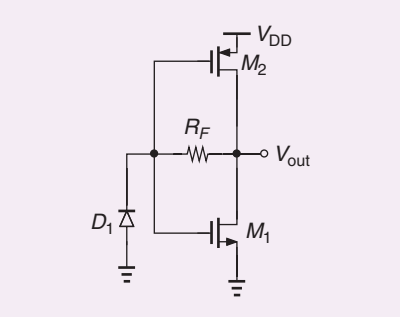

FIGURE 14: The TIA using an inverter.

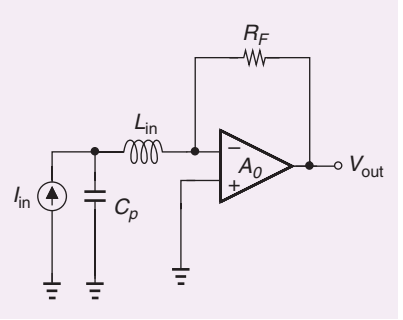

FIGURE 15: The TIA with series peaking.

With $r_{O1} < \infty$, we employ the model shown in Figure 12(b), assuming $(R_1 + R_2) \| R_L$ is large enough, to obtain

$$\frac{V_{out}}{V_{in}} = \frac{R_{out}}{R_{out} + r_{O1}} \tag{14}$$

$$\approx \left(1 + \frac{R_1}{R_2}\right) \frac{1}{g_{m1} r_{O1} A_1}. \tag{15}$$

Compared to (5), the follower-based LDO has a factor of $g_{m1} r_{O1}$ advantage in PSRR. The output noise of this LDO is found as illustrated in Figure 7 for the previous topology:

$$\overline{V_{n,out}^2} = \left(1 + \frac{R_1}{R_2}\right)^2 \left(\overline{V_{nA}^2} + \frac{\overline{V_{nM}^2}}{A_1^2}\right). \tag{16}$$

Thus, the two structures have the same output noise.

The prior calculations predict that the PSRR, output impedance, and output noise of the follower-based LDO exhibit the same general frequency-domain behavior as those of the current-source-based topology. However, the source follower leads to different results. Drawing the open-loop LDO as in Figure 13, we recognize that the output pole is roughly equal to $1/(g_{m1}^{-1} C_M)$, which assumes a much higher value than that in Figure 10. Moreover, because of the source follower's bootstrapping of C_G, the op amp does not see this entire capacitance. For example, if the gain from V_F to V_{out} is 0.7, we can apply the Miller theorem to C_G, concluding that about 30% of this capacitance loads the op amp. Thus, the follower-based LDO generally provides a greater compensated bandwidth than does the current-source-based topology. In both LDO structures, we first select the smoothing capacitor to obtain the desired load regulation at a given frequency (e.g., at the switching frequency of the divider in Figure 2) and then compensate the loop by adjusting the op amp's dominant pole.

Questions for the Reader

1) How does C_M shape the PSRR of the circuit in Figure 9?
2) The op amp gain in Figure 12(a) falls at high frequencies. Can we place a capacitor in parallel with R_1 to counteract this effect and maintain a relatively constant loop gain?

Answers to Last Issue's Questions

1) Calculate the input-referred noise current of the transimpedance amplifier (TIA) shown in Figure 14. Does this noise increase or decrease if we consider channel-length modulation?

   Let us assume $\lambda = 0$. We first compute the circuit's transimpedance to be $1/(g_{m1} + g_{m2}) - R_F \approx -R_F$. Next, we find the output noise voltage resulting from R_F and the two transistors as $4kTR_F + 4kT\gamma/(g_{m1} + g_{m2})$. Dividing the latter by R_F^2 gives the input-referred noise current:

$$I_{n,in}^2 = \frac{4kTR_F + 4kT\gamma/(g_{m1} + g_{m2})}{R_F^2}. \tag{17}$$

   In the presence of channel-length modulation, the gain and the output noise voltage drop by the same factor. Thus, the input-referred noise current does not change.

2) How should L_{in} be chosen in Figure 15 so that we have $\omega_{-3dB} \approx [\sqrt{2}(1 + A_0)] R_F C_p$? For this second-order system, we select a damping factor $\zeta = \sqrt{2}/2$, which leads to

$$\sqrt{\frac{L_{in}}{C_p}} = \frac{R_F}{A_0 + 1}. \tag{18}$$

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