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The Design of Broadband I/O Circuits

The transport of high-speed data to and from chips requires input–output (I/O) interfaces with a commensurately wide bandwidth. In addition to the parasitic capacitances that the output driver in a transmitter (TX) and the input stage in a receiver (RX) present to the signal path, both interfaces must also deal with the capacitances associated with electrostatic discharge (ESD) protection devices. The I/O design thus becomes increasingly more challenging as greater speeds are sought. In this article, we design I/O circuits for a data rate of 40 Gb/s with a single-ended voltage swing of 0.5 V_{pp} while focusing on the use of T-coils. The reader is referred to [1]–[5] for background information.

General Considerations

The output pin a generic broadband TX incurs three capacitances arising from the driver circuit, the ESD device, and the pad. Shown in Figure 1(a) is an example with the respective values $C_{dr} = 100$ fF, $C_E = 300$ fF, and $C_p = 70$ fF. The network drives a transmission line having a characteristic impedance of $R_L = 50\,\Omega$ and employs a back-termination resistor, $R_T = 50\,\Omega$, so as to absorb signal components that are reflected from the far end of the line. Suppressing "secondary" reflections, R_T does increase the power consumption by a factor of 2, but it proves necessary for data rates above a few gigabits per second.

To transmit broadband data, the output structure of Figure 1(a) must provide a bandwidth approximately equal to 70% of the data rate, 28 GHz in our case, so as to introduce negligible intersymbol interference (ISI). The ISI manifests itself as both vertical and horizontal eye closure. Moreover, the circuit must exhibit acceptable output impedance matching to suppress secondary reflections. As a rule of thumb, we seek an output return loss, S_{22}, lower than −10 dB for frequencies up to the "Nyquist rate," 20 GHz in our case.

Unfortunately, the parasitics in Figure 1(a) prohibit the circuit from meeting either of the two criteria. The −3-dB bandwidth is limited to $1/[2\pi(R_T \| R_L) C_{tot}] = 13.5$ GHz, where $C_{tot} = 470$ fF. Also,

$$S_{22} = \left| \frac{Z_{22} - R_L}{Z_{22} + R_L} \right| \tag{1}$$

$$= \frac{R_T C_{tot} \omega}{\sqrt{4 + R_T^2 C_{tot}^2 \omega^2}}, \tag{2}$$

which reaches a value of $1/\sqrt{2} \equiv -3$ dB at the −3-dB bandwidth. Figures 1(b) and 1(c) plot the output eye diagram and S_{22}, respectively. In our simulations, we assume that the 40-Gb/s data has 10-ps rise and fall times.

The eye in Figure 1(b) has a vertical opening of about 64% of the nominal swing, which may appear adequate in some applications. But we must bear in mind that the input port on the receive side suffers from similar effects, exacerbating both the bandwidth and return loss issues. As illustrated in Figure 2(a), the RX presents the same C_E and C_p values along with an input capacitance, C_{in}, which we assume to be 50 fF. For a short connection between the TX and the RX, the overall bandwidth falls to about 7.2 GHz, yielding the received eye diagram shown in Figure 2(b). The vertical opening is about 24%, and the peak-to-peak jitter is around 9.4 ps. The performance further degrades if the transmission line is longer, as depicted in Figure 2(c) for a length of 25 cm.

The use of T-coils can dramatically increase the bandwidth and improve the return loss in both TXs and RXs. The penalty is the area consumed by the T-coil inductors.

T-Coil Circuit Topologies

Before delving into analysis and design, we should distinguish among several different T-coil circuit structures as they exhibit somewhat different properties. The classic T-coil configuration, originally realized in discrete form [1] and also analyzed in [3], is depicted in Figure 3(a). This circuit is driven by a current source at one end of the T-coil, delivers its output across C_E, and lacks back termination; thus, it can primarily serve as an interstage gain block and not as an output driver. Illustrated in Figure 3(b), the second topology is

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driven by a current source across the capacitor, provides back termination, and delivers a current to R_L. We will employ this structure for "current-mode" outputs. Figure 3(c) shows the third realization, where the back-termination resistor, R_T, is driven by a voltage source; this arrangement will serve as a "voltage-mode" output stage. Finally, Figure 3(d) presents an input port in which a T-coil is driven by a transmission line and delivers the signal to the RX across C_E. Note that the parasitic capacitances appear at different ports of the T-coil network in different I/O configurations.

Properties of T-Coils

The most important property of T-coils in I/O design is that they can absorb a large parasitic capacitance and yet provide a constant resistive input or output impedance across a wide frequency range. We investigate this point by turning to Figure 4(a) and recognizing that, if the

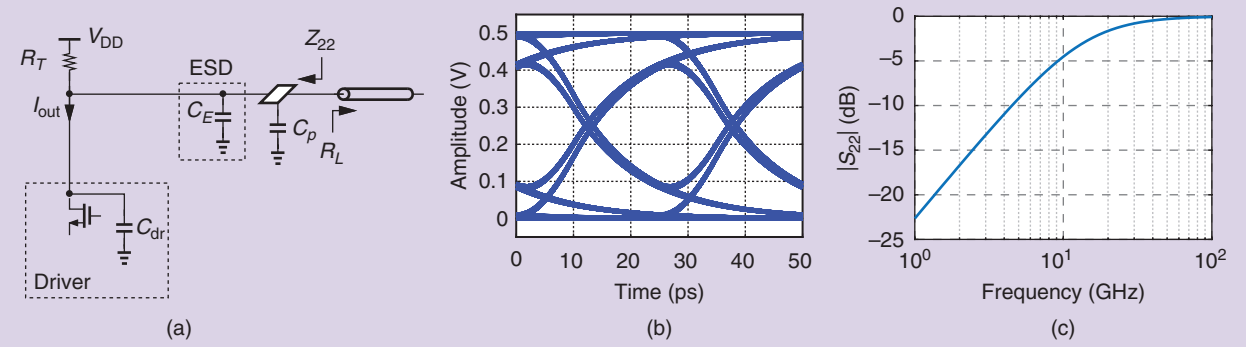

FIGURE 1: (a) A generic TX output stage, (b) its output eye diagram, and (c) its output return loss.

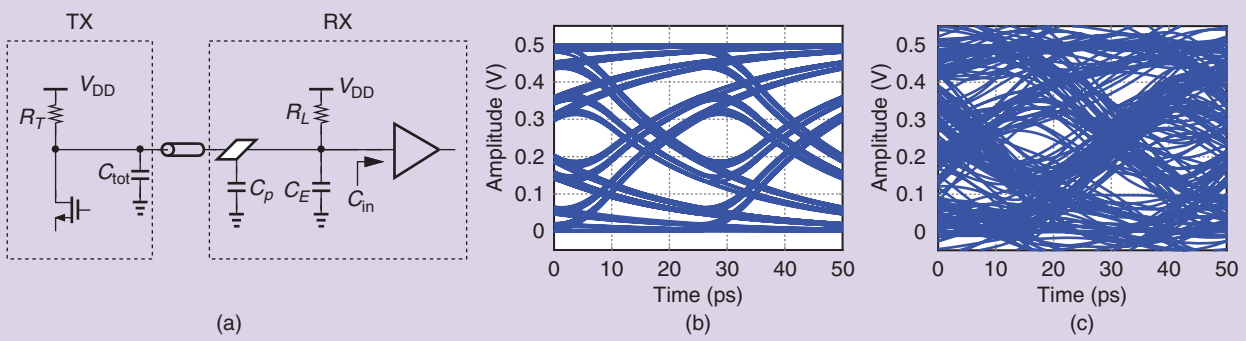

FIGURE 2: (a) A simple TX/RX link, (b) the received eye diagram for a short transmission line, and (c) the received eye diagram for a 25-cm transmission line.

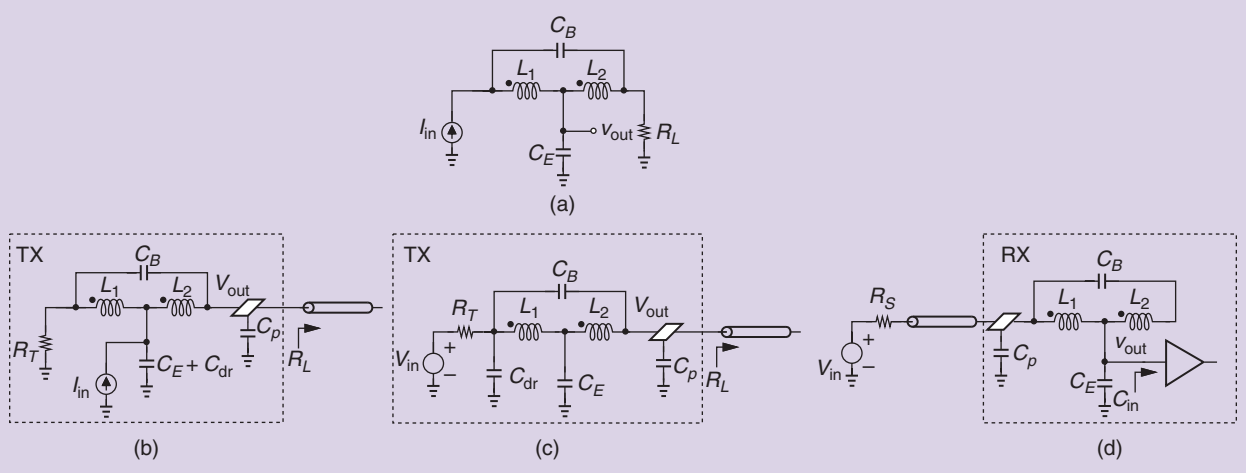

FIGURE 3: (a) A classic T-coil-based gain stage, (b) a T-coil-based current-mode driver, (c) a T-coil-based voltage-mode driver, and (d) an input stage using a T-coil.

impedance seen by I_{in} is equal to R_L at all frequencies, then $|V_{out1}| = |V_{in}|$ because the real power delivered by I_{in} is dissipated by only resistor R_L. That is, the transfer function V_{out1}/I_{in} must display an all-pass response and hence an infinite bandwidth. We wish to obtain the conditions that yield such a behavior. We assume hereafter that $L_1 = L_2 = L$ and denote their mutual inductance by M.

From basic circuit theory, we know that two coupled inductors sharing a terminal can be represented by three uncoupled ones [Figure 4(b)]. In the next step of our simplification, we perform a Δ-Y transformation on the two equal inductors and C_B, as depicted in Figure 4(c). Here,

$$Z_1 = \frac{(L+M)s \cdot \frac{1}{C_B s}}{(L+M)s + \frac{1}{C_B s} + (L+M)s} \tag{3}$$

$$= \frac{(L+M)s}{2(L+M)C_B s^2 + 1} \tag{4}$$

and

$$Z_T = \frac{(L+M)s \cdot (L+M)s}{(L+M)s + \frac{1}{C_B s} + (L+M)s} \tag{5}$$

$$= \frac{(L+M)^2 C_B s^3}{2(L+M)C_B s^2 + 1}. \tag{6}$$

Dividing I_{in} between the two branches, we have

$$\frac{V_{out1}}{I_{in}} = \frac{Z_T - Ms + \frac{1}{C_E s}}{Z_T - Ms + \frac{1}{C_E s} + Z_1 + R_L} R_L. \tag{7}$$

It follows from (4) and (6) that

$$\frac{V_{out1}}{I_{in}} = \frac{N}{D} R_L, \tag{8}$$

where

$$N = (L-M)^2 C_E^2 s^4 + 2(L-3M)C_E s^2 + 4 \tag{9}$$

$$D = (L-M)^2 C_E^2 s^4 + 8R_L C_E (L+M) C_B s^3 + 2(3L-M)C_E s^2 + 4R_L C_E s + 4. \tag{10}$$

As expected, $V_{out1}/I_{in} \to R_L$ at both very low and very high frequencies. For an all-pass response, $|V_{out1}/I_{in}|$ must remain independent of ω. Equating the square of this quantity to unity yields

$$[(L-M)^2 C_E^2 \omega^4 - 2(L-3M)C_E \omega^2 + 4]^2 = [(L-M)^2 C_E^2 \omega^4 - 2(3L-M)C_E \omega^2 + 4]^2 + [-8R_L C_E (L+M) C_B \omega^3 + 4R_L C_E \omega]^2 \tag{11}$$

and hence

$$R_L^2 C_E = 2(L+M) \tag{12}$$

$$2R_L^2 C_B = L - M. \tag{13}$$

These results can be recast in terms of the coupling coefficient between the inductors, $k = M/\sqrt{L_1 L_2} = M/L$:

$$L = \frac{R_L^2 C_E}{2(1+k)} \tag{14}$$

$$C_B = \frac{1-k}{1+k} \cdot \frac{C_E}{4}. \tag{15}$$

We should make two remarks. First, (14) and (15) contain three unknowns, L, C_B, and k, suggesting some flexibility in the choice of the T-coil parameters. As explained next, k is typically selected around 0.5 for a well-behaved transient response. Second, the conditions stipulated by (14) and (15) allow us to decompose D in (10) into a product of two second-order polynomials:

$$D = \frac{1}{R_L^2 C_B}[2(L+M)R_L C_B s^2 + (L+M)s + R_L] \times [2(L-M)C_E C_B R_L s^2 + (L-M)C_E s + 4R_L C_B]. \tag{16}$$

This factorization proves useful in the following analysis.

We also recognize in Figure 4(c) that $I_{in} = V_{out1}/R_L + V_{out2} C_E s$ and, thus,

$$\frac{V_{out2}}{I_{in}} = \left(1 - \frac{V_{out1}}{I_{in} R_L}\right) \frac{1}{C_E s} \tag{17}$$

$$= 4 \frac{2(L+M)R_L C_B s^2 + (L+M)s + R_L}{D}. \tag{18}$$

This transfer function exhibits a low-pass response and reduces to a second-order system if (14) and (15) hold; the decomposition in (16) reveals the common factor between the numerator and the denominator. It follows that

$$\frac{V_{out2}}{I_{in}} = \frac{4R_L^2 C_B}{2(L-M)C_E C_B R_L s^2 + (L-M)C_E s + 4R_L C_B}. \tag{19}$$

Expressing the denominator in the form of $s^2 + 2\zeta\omega_n s + \omega_n^2$ we have

$$\omega_n^2 = \frac{2}{(L-M)C_E} \tag{20}$$

$$= \frac{2}{L(1-k)C_E} \tag{21}$$

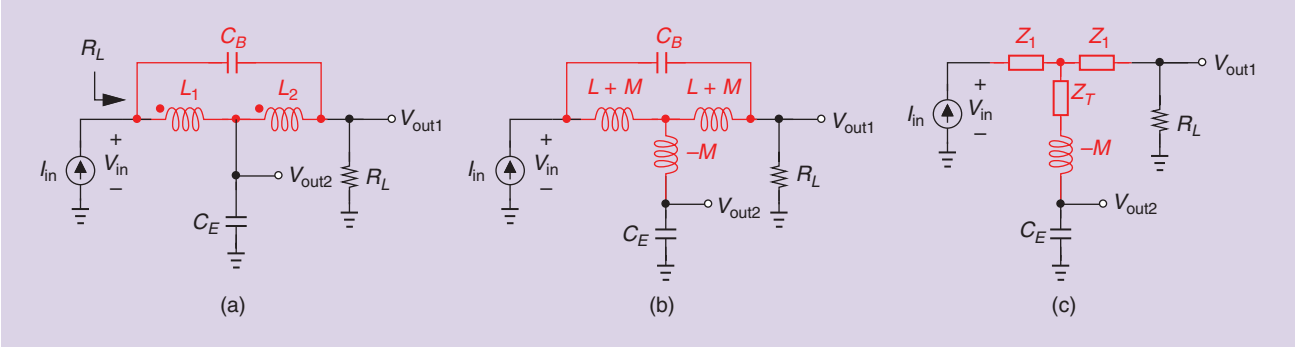

FIGURE 4: (a) A T-coil network driven by a current source, (b) a simplification using three uncoupled inductors, and (3) a simplification using a Δ-Y transformation.

and

$$\zeta^2 = \frac{L+M}{4(L-M)} \tag{22}$$

$$= \frac{1+k}{4(1-k)}. \tag{23}$$

In practice, we choose ζ according to the desired time response of the second-order system. For example, $\zeta = \sqrt{3}/2$ yields a uniform group delay [1], [2] and $k = 0.5$. More aggressive values of ζ, e.g., $\zeta = 1$, offer greater bandwidths but also higher k values, a difficult condition for on-chip inductors to meet.

In summary, for the basic T-coil to present a constant input or output resistance, we have in Figure 4(a)

$$L_1 = L_2 = \frac{R_L^2 C_E}{3} \tag{24}$$

$$C_B = \frac{C_E}{16\zeta^2} \tag{25}$$

$$k = \frac{4\zeta^2 - 1}{4\zeta^2 + 1}. \tag{26}$$

We hereafter assume $\zeta = \sqrt{3}/2$ and $k = 0.5$.

Current-Mode Drivers

The current-mode driver of Figure 3(b) merits some remarks. Suppose $C_p = 0$. Drawing the structure as shown in Figure 5(a), we recognize the symmetry of this arrangement, predicting that nodes A and B have the same voltage and can therefore be shorted to each other [Figure 5(b)]. This leads to the simplified topology in Figure 5(c), a series-peaked circuit. We then conclude that 1) C_B has no role in the transfer function V_{out1}/I_{in}, a point of contrast to the behavior of the circuit in Figure 3(a), and 2)

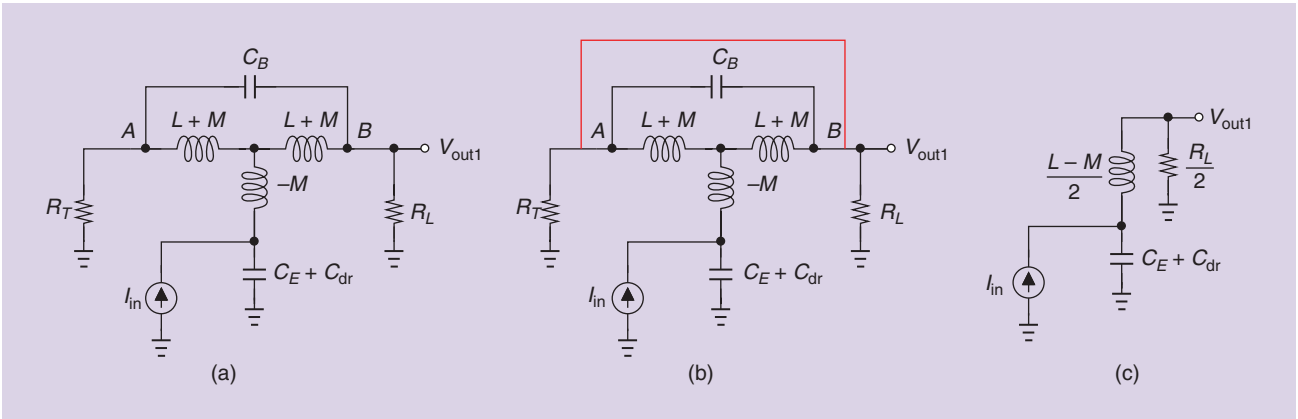

FIGURE 5: (a) A basic current-mode driver, (b) its equivalent circuit, and (c) its further simplified topology.

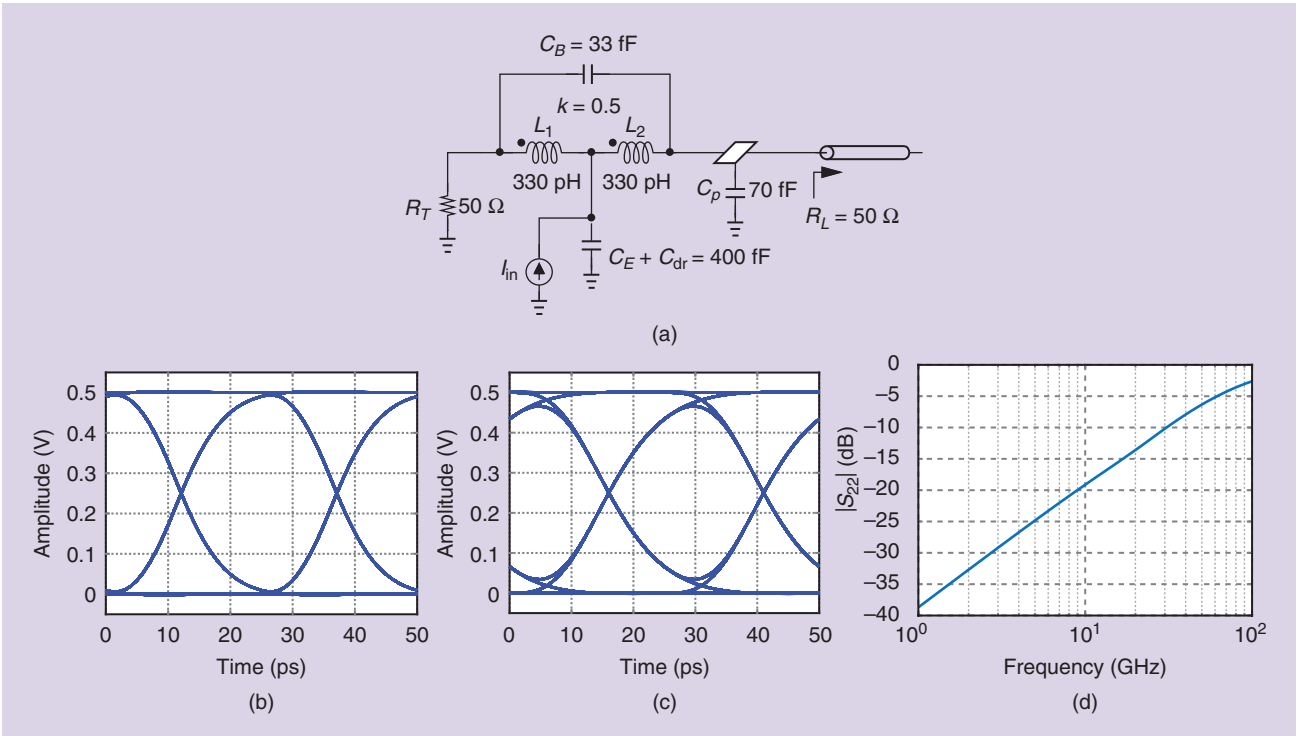

FIGURE 6: (a) A current-mode driver design, (b) its output eye diagram with C_p = 0, (c) its output eye diagram with C_p = 70, and (d) its output return loss with C_p = 70 fF.

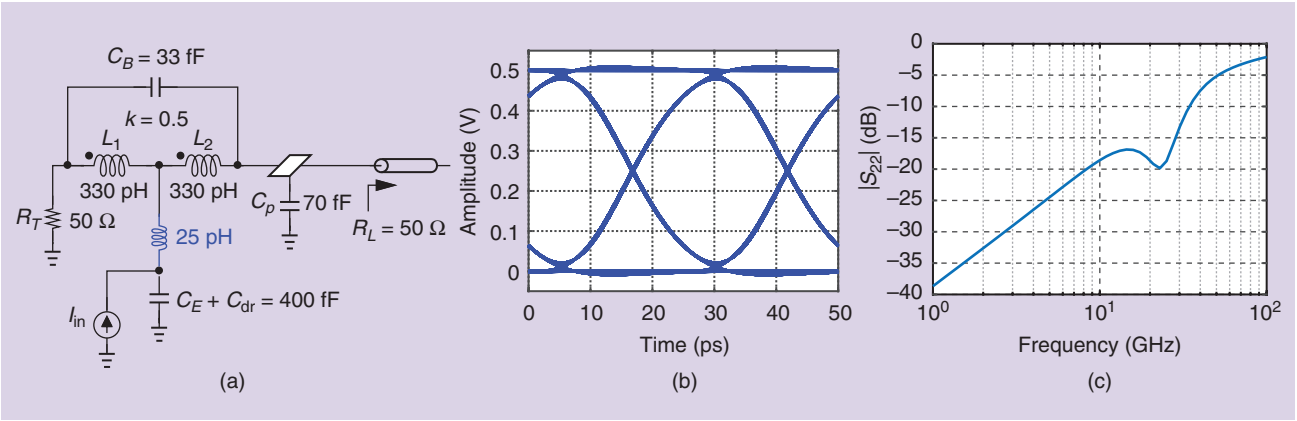

FIGURE 7: (a) The addition of a series-peaking inductor to a current-mode driver, (b) the resulting eye diagram, and (c) the corresponding output return loss.

this network improves the bandwidth only as much as series peaking does. The T-coil's principal role here is therefore to achieve broadband matching.

The design specifications mentioned earlier and the topology of Figure 3(b) lead to the basic current-mode design shown in Figure 6(a). In this case, the driver's capacitance is merged with C_E, necessitating from (14) an inductance of 330 pH and from (15) a bridge capacitance of 33 fF. The pad capacitance appears at the output node and has not been taken into account in our previous derivations. Figures 6(b) and 6(c) plot the output eye diagram with $C_p = 0$ and $C_p = 70$ fF, respectively, displaying some vertical closure due to this parasitic. Figure 6(d) shows that $|S_{22}| < -10$ dB for frequencies up to 30 GHz if $C_p = 70$ fF.

The effect of C_p on the performance can be ameliorated by applying series peaking to the driver current source. As illustrated in Figure 7(a), a 25-pH inductor precedes the center tap of the T-coil. Depicted in Figures 7(b) and 7(c), respectively, the eye height and S_{22} show some improvement. Values greater than 25 pH further enhance these aspects but raise the jitter. Comparing the results in Figure 7 to those in Figure 1, we observe the remarkable performance improvement afforded by T-coils.

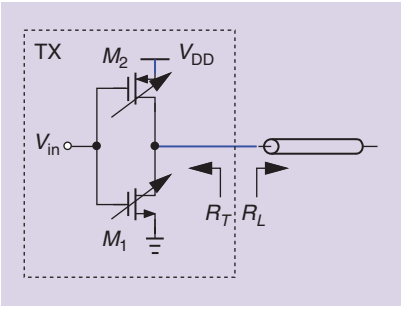

FIGURE 8: A basic voltage-mode driver.

Voltage-Mode Drivers

Broadband TXs can employ voltage-mode output interfaces to save power. Illustrated in Figure 8(a) [4], the idea is to design a CMOS inverter such that it provides a Thevenin resistance of $R_T = R_L$ when M_1 or M_2 is on. It can be shown that, for a given output voltage swing, this approach consumes one-fourth the power of its current-mode counterpart. The widths of M_1 and M_2 are programmable to compensate for process, voltage, and temperature (PVT) variations. Consequently, the inverter output node sustains a heavy capacitance. This approach suffers from two disadvantages with respect to current-mode drivers: it requires rail-to-rail input data swings, which are difficult to generate at very high speeds, and it draws large transient currents from the supply, necessitating a great deal of bypass capacitance.

The basic T-coil-based voltage-mode driver exhibits a transfer function similar to (8). This point is justified by considering Figure 9(a). We note that, if (14) and (15) are satisfied, the T-coil presents an input resistance equal to R_L at all frequencies, creating $I_{in} = V_{in}/(R_T + R_L)$.

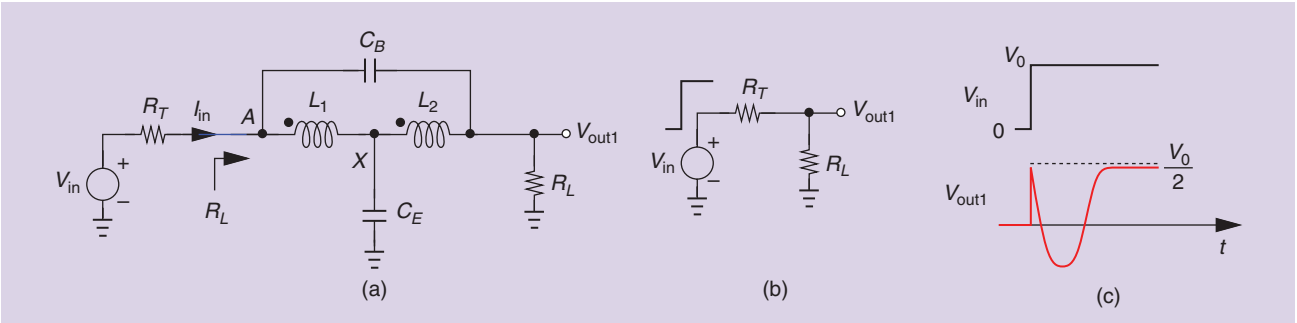

FIGURE 9: (a) A voltage-mode driver with a step input, (b) its equivalent circuit at $t = 0^+$, and (c) its waveforms.

Since $V_{out1}/V_{in} = (V_{out1}/I_{in})(I_{in}/V_{in})$, we conclude that V_{out1}/V_{in} and V_{out1}/I_{in} simply differ by a factor of $R_T + R_L$.

The use of a T-coil in a voltage-mode interface entails an interesting, yet undesirable effect. Returning to the ideal topology shown in Figure 9(a) and assuming a step input, we remark that, at $t = 0^+$, the circuit reduces to the voltage divider in Figure 9(b), concluding that $V_A(0^+) = V_{out1}(0^+) = V_0/2$. Also, $V_X(0^+) = 0$. Thus, C_E begins to charge through both L_1 and L_2, pulling V_{out1} *down* [Figure 9(c)]. In fact, with the component values chosen earlier, V_B drops to *negative* values before returning to $V_0/2$, an effect that severely closes the eye.

Fortunately, this issue is alleviated by three factors in the more realistic network of Figure 3(c): the finite rise and fall times of V_{in}, the driver output capacitance, and the pad capacitance. The first two slow down the charging action of C_B, allowing some of its current to flow through L_2 rather than through R_L. As a result, the initial jump at $t = 0^+$ is less than $V_0/2$. Moreover, C_p forms a voltage divider with C_B, further attenuating this jump.

The foregoing effect is also verified by writing (8) as $1 + P/D$, where P is a third-order polynomial, and observing that the circuit translates an input step to an output step. It is interesting to note that the current-mode network of Figure 5(a) does not suffer from this phenomenon: a step in I_{in} is initially absorbed by $C_E + C_{dr}$ and does not yield a step at the output. Equation (19) confirms this point as well.

Figure 10(a) shows the design of our voltage-mode output interface. The T-coil values are computed from (14) and (15) so as to accommodate an ESD capacitance of 300 fF. Figures 10(b) and 10(c) plot the output eye diagram and $|S_{22}|$, respectively. The latter remains below –10 dB up to 20 GHz. In a manner similar to the series peaking method of Figure 7(a), we can place a 25-pH inductor in series with C_E so as to raise the –10-dB frequency of $|S_{22}|$ by a few gigahertz.

Input Interface

The input network of Figure 2(a) can greatly benefit from a T-coil structure, as illustrated in Figure 3(d). Shown in Figure 11(a), the T-coil drives $C_E + C_{in} = 350$ fF and, according to (14) and (15), employs $L_1 = L_2 = 290$ pH and $C_B = 30$ fF. We observe that, if $C_p = 0$, this circuit presents a constant resistive impedance equal to R_T to

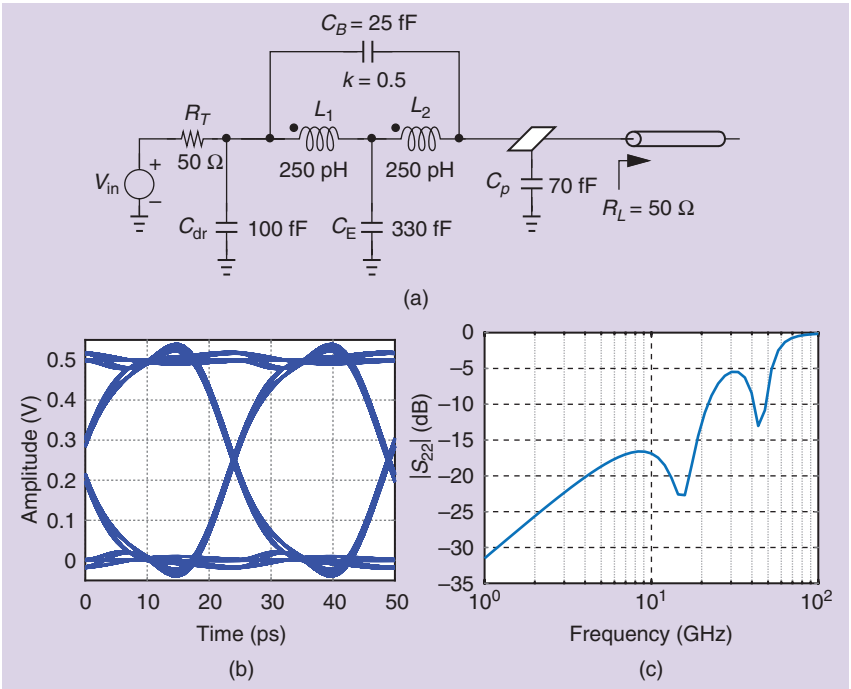

FIGURE 10: (a) A voltage-mode driver design, (b) its output eye diagram, and (c) its output return loss.

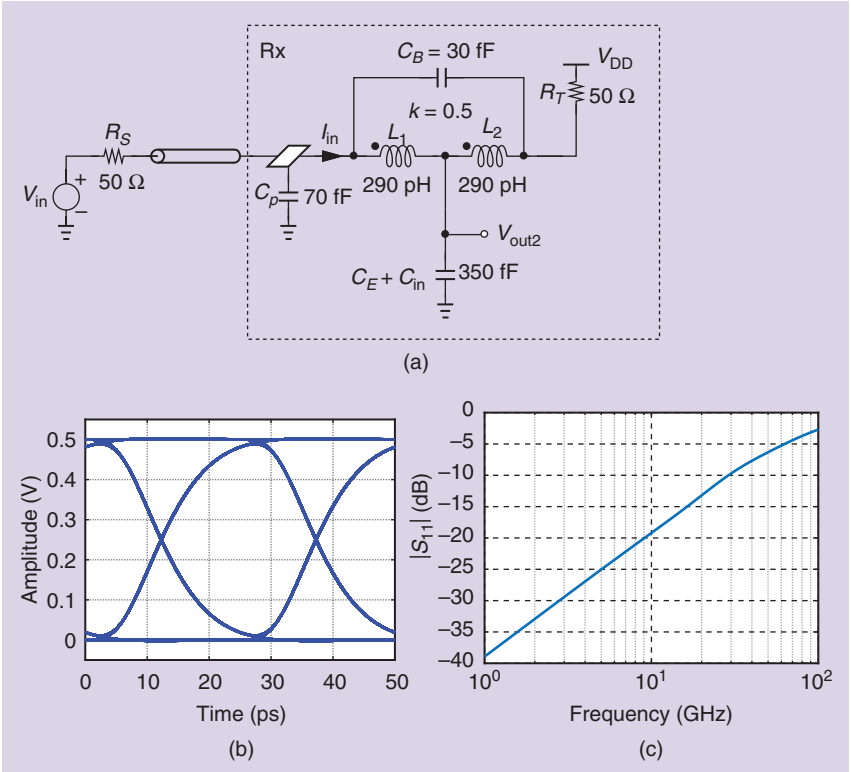

FIGURE 11: (a) An input network design, (b) its output eye diagram, and (c) its input return loss.

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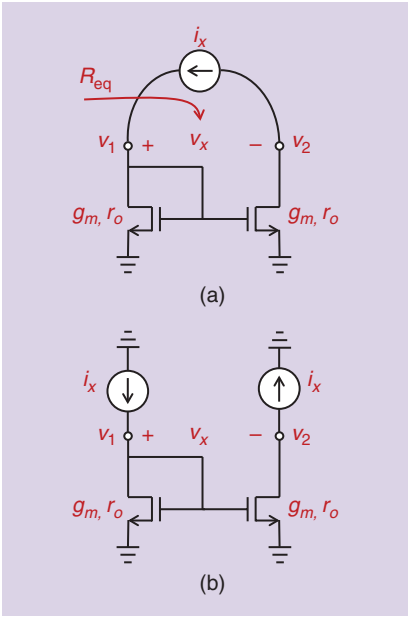

FIGURE 6: (a) Measuring the output resistance between the two nodes of a current mirror using a test current source. (b) Splitting the test current source into two single-ended current sources.

$$v_x = v_{1l} + v_{1r} - (v_{2l} + v_{2r})$$

$$= i_x(r_{o1} + r_{o2}).$$

Step 4: Find R_{eq} as v_x/i_x:

$$R_{eq} = r_{o1} + r_{o2}.$$

This result is indeed similar to the result we found in relation to the circuit of Figure 1.

As our final example, we determine the output resistance of a current mirror as shown in Figure 6(a). At a first glance, the output resistance may appear to be the sum of $1/g_m // r_o$, which is the resistance looking into the left node, and r_o, which is the resistance looking into the right node. However, using the step-by-step procedure we followed for the differential pair, one can verify that

$$v_x = 2r_o i_x$$

$$R_{eq} = 2r_o.$$

This result, being exact (that is, no approximation), may seem surprising. Indeed, the resistance looking into v_1 alone can be approximated with $1/g_m$ (assuming $1/g \ll r_o$). However, the resistance looking into v_2 is $2r_o$. How could this be? The answer lies in the act of mirroring, which effectively doubles the short circuit current [1] of node 2: one explicit i_x on the right side and one mirrored from the left side. When added and multiplied by r_o, they produce a voltage that is twice as large or, equivalently, a resistor that is $2r_o$ (given that we see only one i_x leaving node 2). This example also illustrates how a differential current going into the current mirror does not produce a differential (complementary) voltage at its two nodes. The reader can verify that the amplitude of v_2 is approximately $2g_m r_o$ times that of v_1.

In summary, to determine the resistance between two nodes in an LTI circuit, we apply a set of differential currents (i_x and $-i_x$) to the two nodes, measure the resulting voltage difference between the two nodes (v_x), and find v_x/i_x. Alternatively, we can apply a voltage source v_x between the two nodes, measure the current i_x that flows from one node to the other through the voltage source, and find v_x/i_x.

References

[1] A. Sheikholeslami, "Looking into a node [Circuit Intuitions]," *IEEE Solid State Circuits Mag.*, vol. 6, no. 2, pp. 8–10, Spring 2014. doi: 10.1109/MSSC.2014.2315062.

[2] A. Sheikholeslami, "Source degeneration [Circuit Intuitions]," *IEEE Solid State Circuits Mag.*, vol. 6, no. 3, pp. 8–10, Summer 2014. doi: 10.1109/MSSC.2014.2329233.

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the transmission line, thereby drawing a frequency-independent input current, $I_{in} = V_{in}/(R_S + R_T)$. It follows that $V_{out2}/V_{in} = (V_{out2}/I_{in})(R_S + R_T)^{-1}$, where V_{out2}/I_{in} is given by (19). The input interface therefore does not exhibit the effect depicted in Figure 9(c).

Figures 11(b) and 11(c) present this design's received eye diagram and $|S_{11}|$, indicating satisfactory performance. The latter remains below −10 dB up to 28 GHz.

References

[1] D. Feucht, *Handbook of Analog Circuit Design*. New York: Academic, 1990.

[2] S. Galal and B. Razavi, "10-Gb/s limiting amplifier and laser/modulator driver in 0.18um CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, pp. 2138–2146, Dec. 2003. doi: 10.1109/JSSC.2003.818567.

[3] J. Paramesh and D. J. Allstot, "Analysis of the bridged T-coil circuit using the extra-element theorem," *IEEE Trans. Circuits Syst. II*, vol. 53, pp. 1408–1412, Dec. 2006. doi: 10.1109/TCSII.2006.885971.

[4] M. Kossel et al., "A T-coil enhanced 8.5-Gb/s high-swing SST transmitter in 65-nm bulk CMOS with ¡-16 dB return loss over 10-GHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 43, pp. 2905–2920, Dec. 2008. doi: 10.1109/JSSC.2008.2006230.

[5] B. Razavi, "The bridged T-coil," *IEEE Solid-State Circuits Mag.*, vol. 7, pp. 10–13, Fall 2015. doi: 10.1109/MSSC.2014.2369332.

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