



The Design of a Millimeter-Wave Frequency Synthesizer

We have previously described the design of a voltage-controlled oscillator (VCO) and a multimodulus divider (MMD) for the 30-GHz range [1], [2]. In this article, we extend our work to develop a millimeter-wave integer-N frequency synthesizer. The reader is referred to the vast body of knowledge in this domain, e.g., [3], [4], [5]. We target the following specifications:

- output frequency range: $f_{out} = 28\text{ GHz}-32\text{ GHz}$
- output phase noise (PN): -100 dBc/Hz at 1-MHz offset
- output spur level: -50 dBc
- output jitter: $< 200\text{ fs}_{rms}$
- reference frequency: $f_{REF} = 100\text{ MHz}$
- reference PN: $S_{REF} = -170\text{ dBc/Hz}$
- power budget: 10 mW .

These quantities merit a few remarks. First, while related, PN and jitter specifications serve different purposes. The former signifies how much a receiver can tolerate blockers in the presence of reciprocal mixing, whereas the latter represents the corruption that the synthesizer imparts to the signal constellation in both the transmit path and the receive path. The desired jitter is computed conservatively by integrating the PN from a 10-kHz offset to a 1-GHz offset, but this range must be carefully chosen in conjunction with the modulation scheme and the symbol rate.

Second, with $f_{REF} = 100\text{ MHz}$, the synthesizer can provide a minimum output frequency step of the same

value. For a finer resolution, one would need to resort to fractional-N operation. Third, the circuit must incorporate a feedback divide ratio, N , of about 300. The synthesizer is designed in 28-nm CMOS technology with $V_{DD} = 0.95\text{ V}$ in the slow-slow corner at $T = 75^\circ\text{ C}$.

PN Considerations

The assumed reference PN of -170 dBc/Hz leads to a number of constraints on the design. As the synthesizer loop bandwidth, f_{BW} , is reduced, this contribution to jitter falls, but that due to the VCO rises. As a rule of thumb, we select f_{BW} to make the two contributions equal, tacitly neglecting other sources of noise. From another perspective, we multiply S_{REF} by N^2 and set the bandwidth equal to the offset frequency at which $N^2 S_{REF}$ intersects the VCO free-running PN, S_{VCO} (Figure 1). In the ideal case, the phase-locked system exhibits a PN profile that is flat up to $\pm f_{BW}$ and drops in proportion to f^2 beyond these points. One can show in such a scenario that the total integrated VCO PN is equal to

$4N^2 S_{REF} f_{BW}$. Doubling this amount to account for the reference, we obtain the rms jitter as

$$\Delta T_j = \frac{\sqrt{8N^2 S_{REF} f_{BW}}}{2\pi} T_{VCO} \quad (1)$$

where T_{VCO} denotes the output period.

Recall from [1] that our complete VCO design is as shown in Figure 2(a) and displays the PN profile shown in Figure 2(b). Since $N^2 S_{REF} \equiv -120\text{ dBc/Hz}$, we draw a horizontal line at this intercept, reaching S_{VCO} at $f_{BW} \approx 6\text{ MHz}$. Equation (1) then yields

$$\Delta T_j \approx 35\text{ fs}_{rms}. \quad (2)$$

This value is far below our 200-fs target, but our synthesizer design will face other imperfections that raise the jitter considerably.

The rigid condition $f_{BW} \approx 6\text{ MHz}$ imposes certain restrictions on the loop parameters, creating tradeoffs among the chip area, PN, and spur level. This point becomes clear later.

Another consequence of reducing f_{BW} is the long settling time. While typical phase-locked loops (PLLs) settle in roughly 50–100 reference cycles, we expect a substantially greater amount in this case. The result may still satisfy the radio standard’s requirement, but it will pose serious issues in terms of the simulation time (see the “The Concept of Loop Scaling” section).

Synthesizer Architecture

As shown in Figure 3, the integer-N synthesizer incorporates the previously

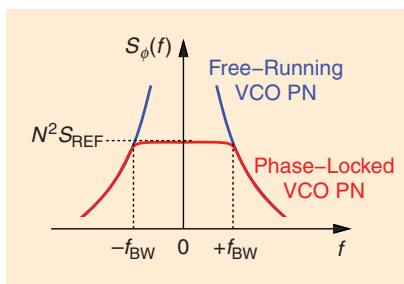


FIGURE 1: The choice of loop bandwidth.

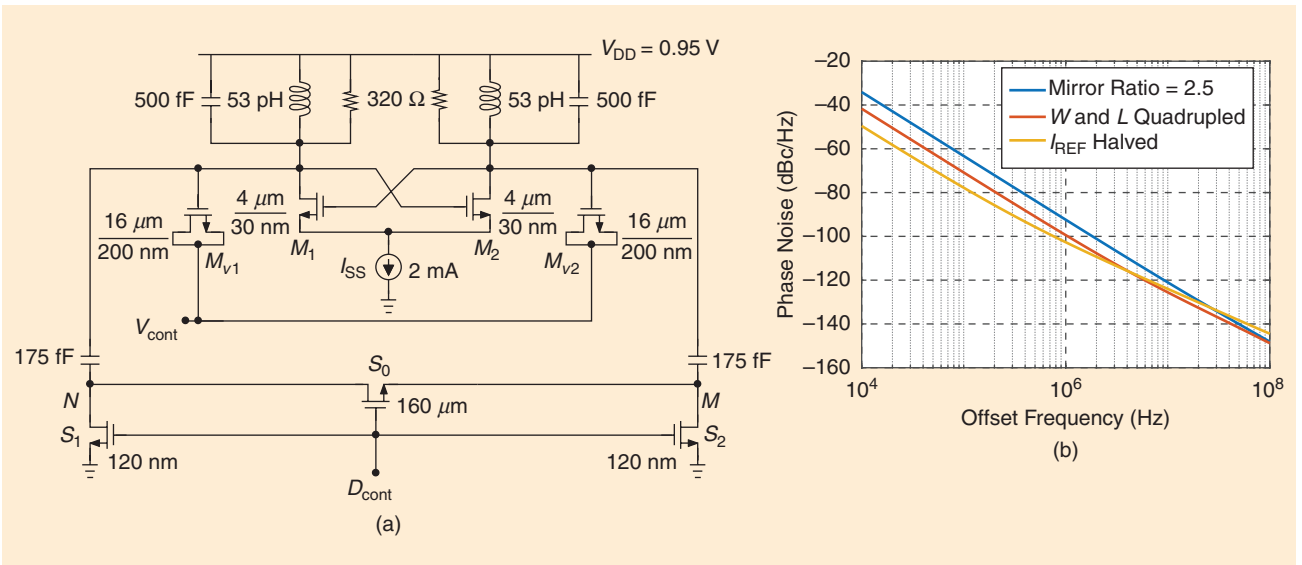


FIGURE 2: (a) The millimeter-wave VCO design and (b) its PN.

designed VCO and MMD along with a phase frequency detector (PFD), a charge pump (CP), and a loop filter. The VCO gain is denoted by K_{VCO} , and the CP current is denoted by I_p . Even though true single-phase clocking offers a lower PN for the PFD [6], we opt for a NOR-based static topology to ensure reliable operation at 100 MHz despite device leakage. We expect that the input-referred PN arising from the PFD and/or the CP may be comparable to $S_{REF} = -170$ dBc/Hz. Thus, the loop BW may need to decrease, leading to a greater integrated jitter.

The closed-loop 3-dB BW is approximately given by

$$(2\pi f_{BW})^2 = [1 + 2\zeta^2 + \sqrt{(1 + 2\zeta^2) + 1}] \omega_n^2 \quad (3)$$

where

$$\zeta = \frac{R_1}{2} \sqrt{\frac{I_p K_{VCO} C_1}{2\pi N}} \quad (4)$$

and

$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1 N}} \quad (5)$$

For well-behaved settling, we select $\zeta = 1$ and arrive at

$$f_{BW} \approx \frac{2.5\omega_n}{2\pi} \quad (6)$$

which, according to our previous estimates, should be set to about 6 MHz. That is, $\omega_n \approx 2\pi(2.4 \text{ MHz})$.

Choice of Loop Parameters

Our 30-GHz VCO provides a K_{VCO} of about $2.08 \text{ GHz/V} \equiv 13.1 \text{ grad/s/V}$. Such a high gain can translate the ripple on the control voltage to large spurs at the output. It is possible to reduce K_{VCO} by making the varactors smaller, but let us proceed with this value for now. With $N \approx 300$ in Figure 3, we must determine I_p , R_1 , C_1 , and C_2 . We begin with $I_p = 0.5 \text{ mA}$, obtaining $C_1 = 15.2 \text{ pF}$ from (5) and $R_1 = 8.7 \text{ k}\Omega$ from (4).

The choice of C_2 in Figure 3 entails a tradeoff. To suppress the CP activity and hence the ripple, we wish to maximize C_2 and can allow a value as large as $0.2C_1$ with negligible effect on the loop settling behavior. However, the pole introduced by C_2 and given by

$$\omega_{p3} = \frac{1}{R_1 \frac{C_1 C_2}{C_1 + C_2}} \quad (7)$$

causes peaking in the input-output response and in the output PN profile. Plotting the magnitude and phase of the loop transmission,

$$H(s) = 2\pi I_p \left(R_1 + \frac{1}{C_1 s} \right) \frac{K_{VCO}}{Ns} \quad (8)$$

in Figure 4, we observe that the phase margin (PM) degrades if ω_{p3} does not lie much farther than the unity-gain bandwidth, $\omega_u (\approx 2\pi f_{BW})$. Thus, we must select $\omega_{p3} \gg 2\pi f_{BW} = 2\pi(6 \text{ MHz})$.

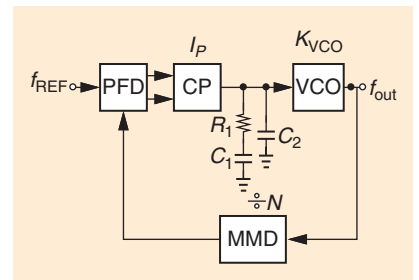


FIGURE 3: The synthesizer architecture.

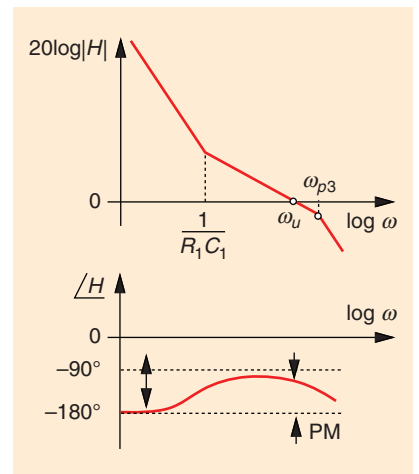


FIGURE 4: The magnitude and phase of the synthesizer's loop transmission. PM: phase margin.

With $R_1 = 8.7 \text{ k}\Omega$, we have $C_2 \approx 0.5 \text{ pF}$ if $\omega_{p3} \approx 5\omega_u$. Figure 5(a) summarizes the results, and Figure 5(b) depicts the CP design. Note that a unity current-mirror ratio in the CP avoids excessive multiplication of the diode-connected devices' noise.

The large area occupied by C_1 motivates us to increase I_p and decrease C_1 in (4) while maintaining $\zeta = 1$. For example, $I_p = 1$ mA yields $C_1 = 7.6$ pF. However, this doubles ω_n and ω_{3dB} . In other words, the 6-MHz loop bandwidth—imposed by $N^2 S_{REF}$ and S_{VCO} —creates a rigid situation in terms of C_1 and I_p , requiring that they scale in the *same* direction. If both are reduced by a factor of α , then so is ζ , which dictates that R_1 be increased by the same factor. Lowering C_2 proportionally as well, we note from (7) that ω_{p3} remains unchanged. We conclude that C_1/α , I_p/α , αR_1 , and C_2/α form a feasible solution (Figure 6). Nonetheless, a lower I_p leads to greater

CP-induced PN (see “The Concept of Loop Scaling” section).

The Need for Fast Simulations

The basic integer- N PLL can be constructed and simulated fairly quickly. However, optimization for loop dynamics and output jitter requires hundreds of simulations. Transient analyses must use a time step much less than T_{VCO} and run for a total time much longer than $T_{REF} = 1/f_{REF}$. For example, if the time step is 5 ps and the loop locks in $50T_{REF} = 500$ ns, the simulation must run for 500,000 points. This is necessary for evaluating the lock time and the output spur level.

Similarly, to obtain the output PN profile, we must perform a periodic

steady-state (pss) simulation for longer than the lock time and follow it by a periodic noise (pnoise) simulation, including a sufficient number of sidebands. Specifically, a divide ratio of $N = 300$ in our example demands about $5N = 1,500$ sidebands, leading to extremely slow pnoise analyses. With the addition of ancillary functions, e.g., voltage regulators, the task becomes nearly impossible. We resolve these issues by introducing the concept of “loop scaling.”

The Concept of Loop Scaling

To save simulation time, we wish to reduce the ratio $f_{VCO}/f_{REF} = N$. Illustrated conceptually in Figure 7, the idea is to scale f_{REF} up and the divide ratio down by the same factor, K . We envision that the loop settling time falls by K . More importantly, the lower complexity of the divider also leads to significantly faster pss and pnoise simulations.

For this concept to deliver consistent results as K decreases toward one, we must bear in mind two points. First, in view of the design effort necessary for the VCO, we prefer not to alter it or its load. Alternatively, we can replace the VCO circuit with a Verilog behavioral model and include its noise by inserting a voltage source in series with its control [7]. In any case, K_{VCO} is constant. Second, we also wish to avoid changes to the transistor-level design of the PFD and CP so that their imperfections do appear in the synthesizer output and exhibit a “scalable behavior” as a function of K . That is, I_p is constant. Third, we must keep ζ constant as well so that the loop dynamics are predictable.

Let us return to (4) and (5) and ask how the loop parameters must scale. If $N \rightarrow N/K$, we opt for $C_1 \rightarrow C_1/K$ so that ζ does not change. As a result, ω_n increases by a factor of K , and so does $f_{BW} = 2.5\omega_n/(2\pi)$. The key point here is that the settling dynamics retain their shape but become K times faster. Figure 8 summarizes our loop scaling principle. This method should not be confused with that in Figure 6.

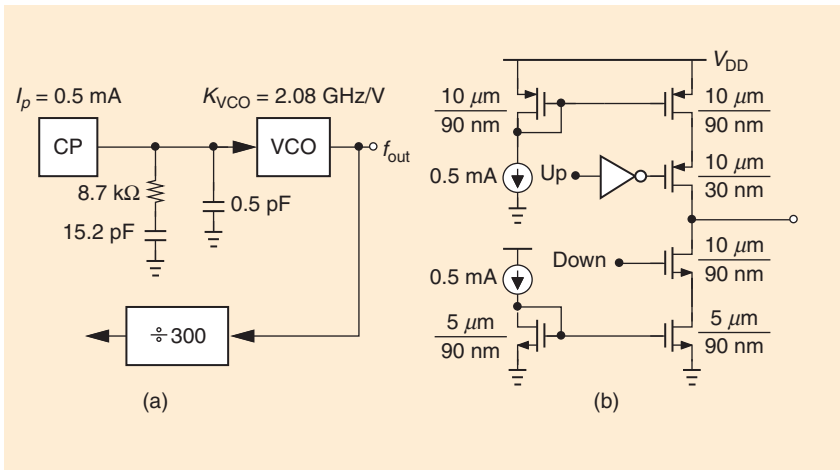


FIGURE 5: (a) Loop parameter values for $f_{BW} = 6$ MHz and (b) CP design.

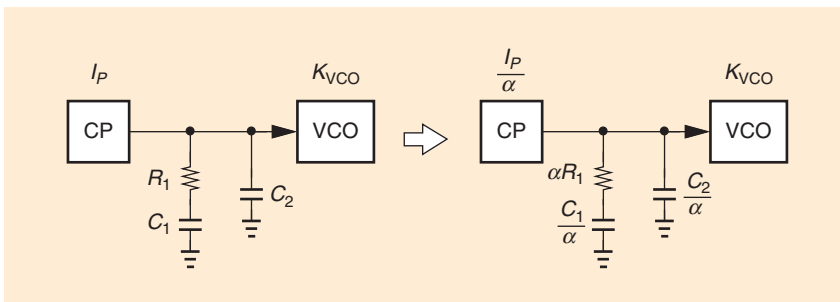


FIGURE 6: The choice of loop parameter values for a constant ζ and bandwidth.

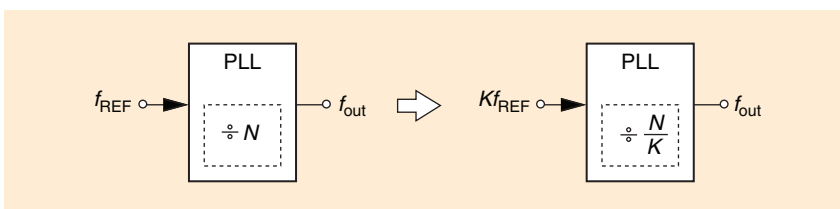


FIGURE 7: An illustration of loop scaling.

The Effect of Loop Scaling on Jitter and Spurs

Our ultimate goal is to be able to predict the performance of the unscaled loop from that of the scaled one. To this end, we construct the PN profiles of the free-running or phase-locked VCO for $K = 1$ and $K > 1$, neglecting flicker noise upconversion for simplicity. As illustrated in Figure 9, the jitter falls for $K > 1$ and is expressed from (1) as

$$\Delta T_J = \frac{\sqrt{4\left(\frac{N}{K}\right)^2 S_{REF}(Kf_{REF})}}{2\pi} T_{VCO} \quad (9)$$

$$= \frac{1}{\sqrt{K}} \frac{\sqrt{4N^2 S_{REF}^2 f_{REF}}}{2\pi} T_{VCO} \quad (10)$$

where the factor of four accounts for only the VCO contribution. That is, the VCO-induced output jitter of the scaled loop is lower by a factor of \sqrt{K} .

Additionally, the reference, the PFD, and the CP also introduce PN, which dominates the “in-band” components, i.e., those between $-f_{REF}$ and $+f_{REF}$. Lumping these contributions into S_{REF} , we observe from Figure 10 that the corresponding jitter (the square root of the area under the profile) falls by a factor of \sqrt{K} regardless of the shape of the input-output transfer function. We can then predict the output jitter as we begin with a heavily scaled loop and gradually decrease K .

The effect of loop scaling on the output reference spurs is studied as follows. Suppose a scaled PLL exhibits a certain ripple amplitude, V_r . The output spur level is given by $V_r K_{VCO}/(4\pi f_{REF})$ if we approximate the ripple by a sinusoid. We now increase C_1 and C_2 by a factor of K and decrease the reference frequency by the same factor. For a fixed PFD/CP design, the ripple amplitude falls by K , yielding a spur level equal to $(V_r/K) K_{VCO}/(4\pi f_{REF}/K) = V_r K_{VCO}/(4\pi f_{REF})$. That is, the spur level remains constant. This point holds even if the ripple is not sinusoidal.

The Choice of MMD Topology

Frequency synthesis requires an MMD whose divide ratio can change

in unity steps. Popular MMD topologies include the pulse-swallow counter and Vaucher’s structure [8]. Used for our millimeter-wave design [1], the latter also lends itself to loop scaling much more easily. This is due to its modular form. As shown in Figure 11, we can cascade two or more stages so as to scale N by a factor of

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K . The pulse-swallow counter, on the other hand, would need to be

redesigned for different K values if their complexity must be minimized.

Simulation Procedure

We perform three simulations for each choice of K so as to quantify the synthesizer’s behavior. First, we run a transient simulation and examine 1) the VCO control settling time and 2) the reference spurs in the output spectrum. We also consider the time alignment of

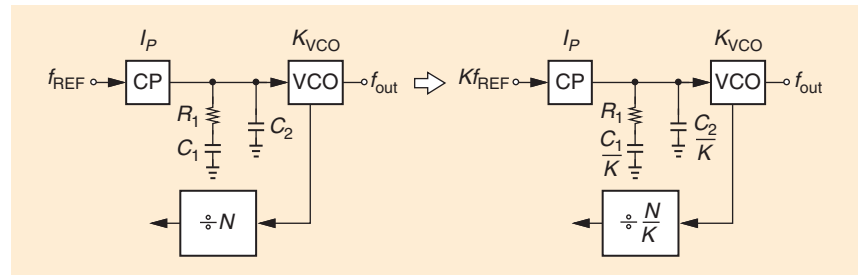


FIGURE 8: The scaling of the loop parameter values.

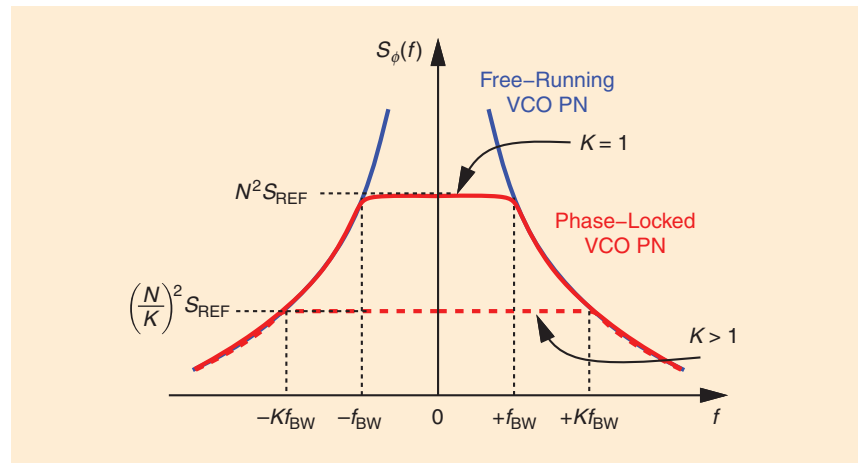


FIGURE 9: The effect of loop scaling on VCO PN.

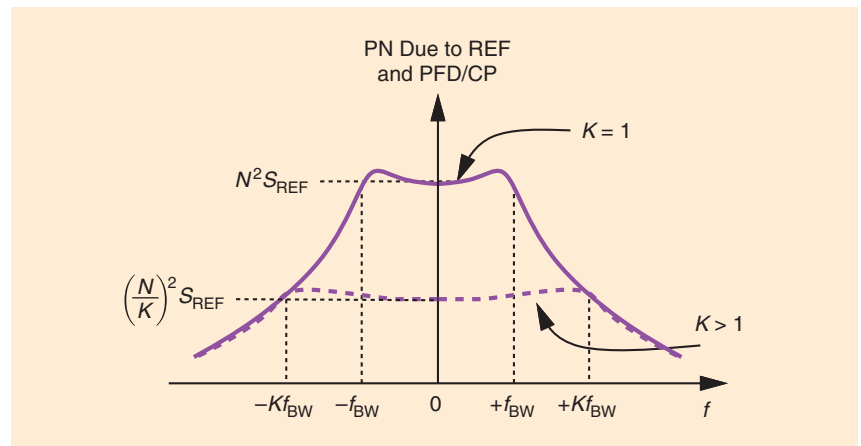


FIGURE 10: The effect of loop scaling on reference, PFD, and CP PN.

the PFD and CP output pulses in the locked condition.

Second, we carry out pss and noise simulations to determine the input-output frequency response. This is accomplished by modulating the supply of the reference buffer by thermal noise so as to impart white PN to the waveform entering the PFD (Figure 12) [7]. If this PN is tens of decibels greater than the synthesizer's intrinsic noise, the output spectrum reveals the transfer function, specifically, the 3-dB bandwidth and the amount of peaking.

Third, we perform another set of pss and noise simulations with the noise of R_D in Figure 12 set to zero, arriving at the output PN profile due to the synthesizer itself. The integral of this profile yields the rms jitter.

First Scaled Loop

We wish to reduce $N = 300$ by a large factor to allow fast simulations. But we must also bear in mind that typical static PFD designs do not operate above 5 GHz in 28-nm technology. We then select $N = 8$, $K = 300/8 = 37.5$, and $f_{REF} = 30 \text{ GHz}/8 = 3.75 \text{ GHz}$. From

the transformation depicted in Figure 8, we have $C_1 = 15.2 \text{ pF}/K = 405 \text{ fF}$ and $C_2 = 13 \text{ fF}$, the latter becoming comparable to the VCO varactors' capacitance and hence causing an error in the value of ω_{p3} . We retain the original values of $I_p = 0.5 \text{ mA}$ and $R_1 = 8.7 \text{ k}\Omega$, arriving at the design shown in Figure 13.

Figure 14 plots the oscillator control voltage, suggesting a settling time of about 15 ns. This waveform also implies a peak-to-peak ripple of about 100 mV, but much of this disturbance arises from the coupling of

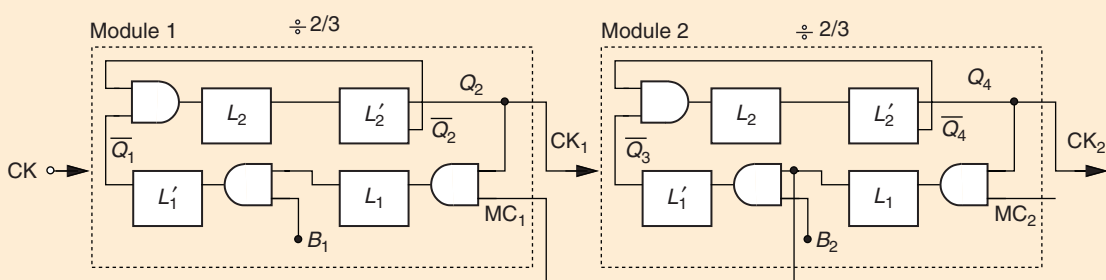


FIGURE 11: Vaucher's modular MMD. CK: clock; MC: modulus control.

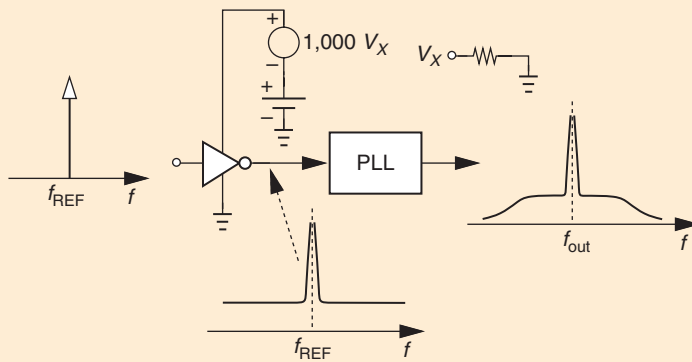


FIGURE 12: Input phase modulation for obtaining the input-output response.

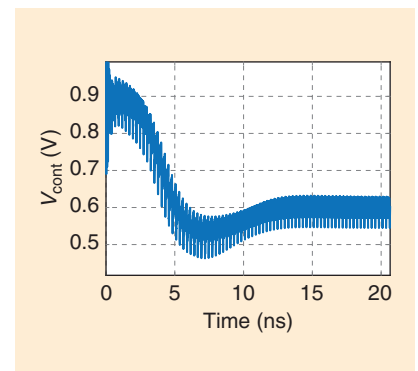


FIGURE 14: Oscillator control voltage settling.

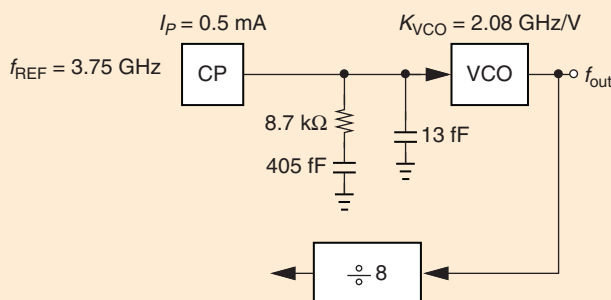


FIGURE 13: A scaled loop with a divider ratio of eight.

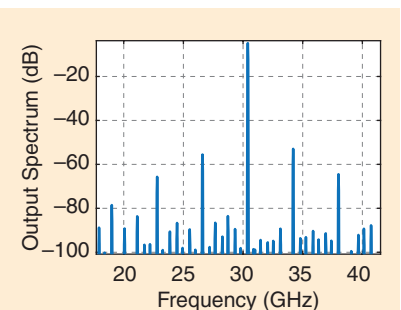


FIGURE 15: The first scaled loop output spectrum.

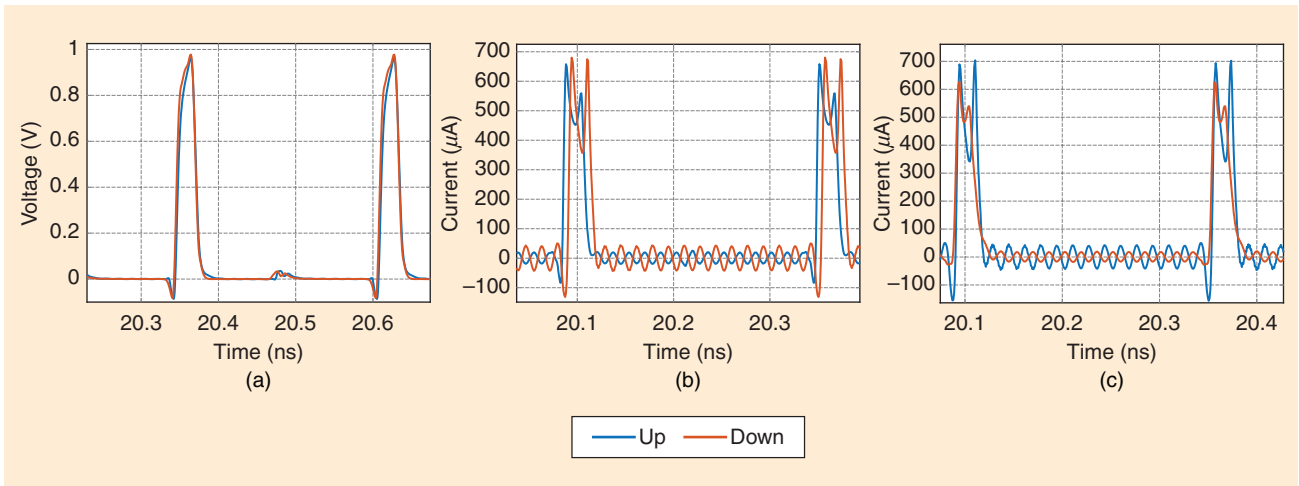


FIGURE 16: (a) PFD up and down pulses, (b) CP up and down currents, and (c) improved alignment between CP up and down currents.

the VCO's internal swings through the varactors. This phenomenon proves benign.

To find the output reference spurs, we take the fast Fourier transform (FFT) of the VCO's differential output from $t = 15$ ns to $t = 20$ ns, obtaining the spectrum shown in Figure 15 and observing a spur level of about -48 dBc, a value greater than our target. Let us delve into this issue by examining the up and down outputs of the PFD [Figure 16(a)]. They appear well aligned. But more relevant are the output current pulses generated by the CP [Figure 16(b)]. Originating from the inverter skew in Figure 5(b), the 6-ps pulsewidth difference noted here is partially responsible for the high spurs. We then insert a transmission gate in the down path and improve the situation to that depicted in Figure 16(c). The spur level falls to -51 dBc.

The next phase of our study relates to the input-output transfer function. We follow Figure 12 and reach the output spectrum shown in Figure 17. The 3-dB BW is 182 MHz, which is somewhat lower than our previous prediction of $Kf_{BW} = 37.5 \times 6 \text{ MHz} = 225 \text{ MHz}$. The response suffers from a peaking of 2.6 dB at 80 MHz.

The last part of our investigation deals with PN and jitter. Plotted in Figure 18 is the output PN profile, displaying a plateau of about -129 dBc/Hz and 0.5 dB of peaking.

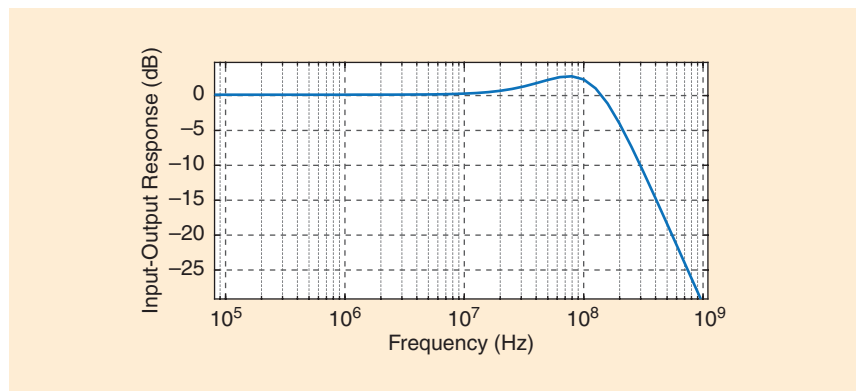


FIGURE 17: The input-output response of the first scaled loop.

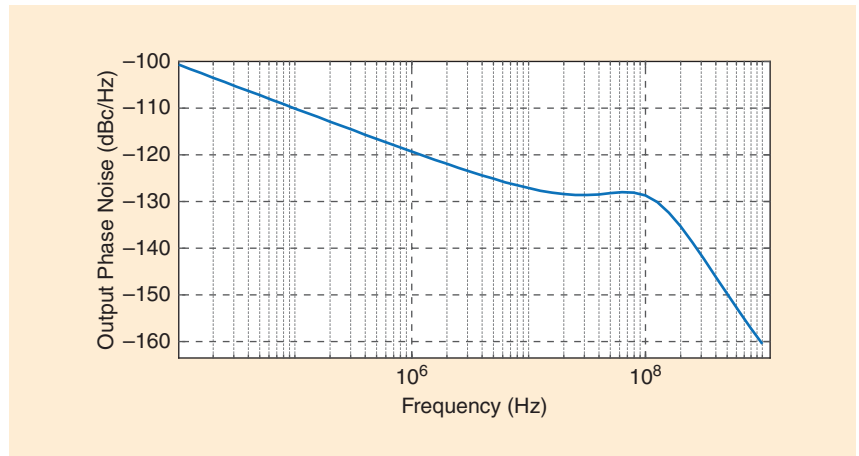


FIGURE 18: The output PN of the first scaled loop.

The PN drops by 3 dB with respect to the plateau value at $f = 147$ MHz. We call this quantity the “noise-shaping” bandwidth.

Let us check the validity of the -129 -dBc/Hz PN in the plateau region. With a noise-shaping BW of 147 MHz, we return to the VCO PN of

Figure 1(b) and predict a value less than -150 dBc/Hz at this offset. Why is there so much discrepancy? We suspect the CP noise. The in-band output PN due to the CP is given by

$$S_{\phi,CP}(f) = (4\pi^2 N^2) \frac{2\overline{I_n}}{I_p^2} \cdot \frac{T_{res}}{T_{REF}} \quad (11)$$

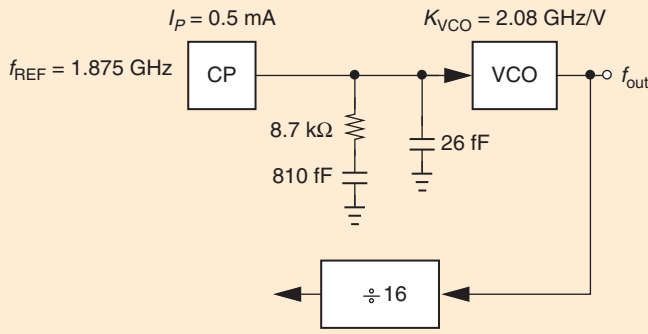


FIGURE 19: A scaled loop with a divide ratio of 16.

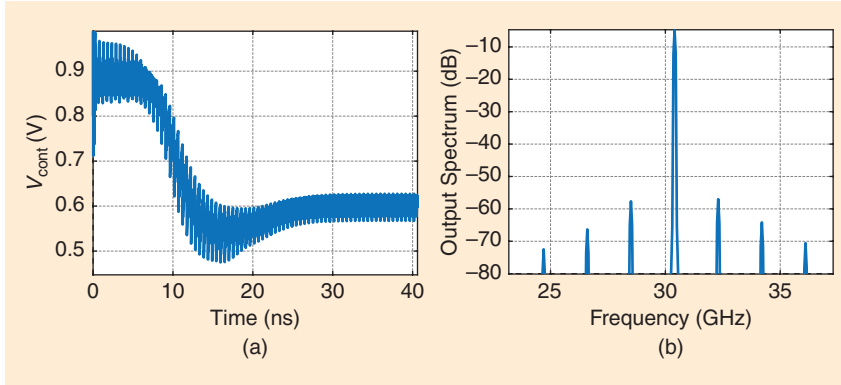


FIGURE 20: (a) Oscillator control settling of the second scaled loop and (b) the output spectrum.

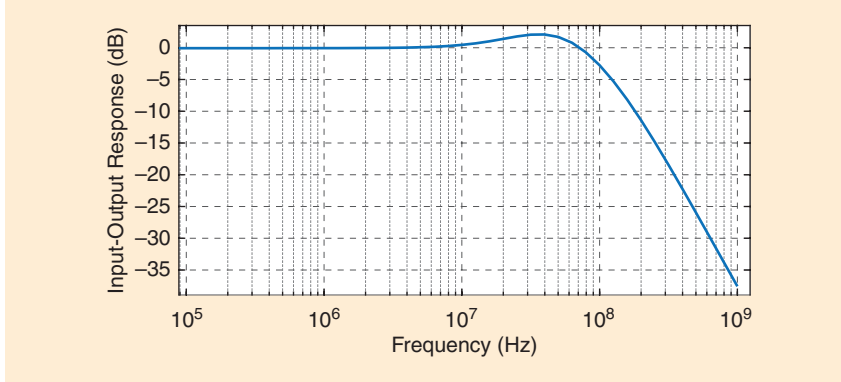


FIGURE 21: The input-output response of the second scaled loop.

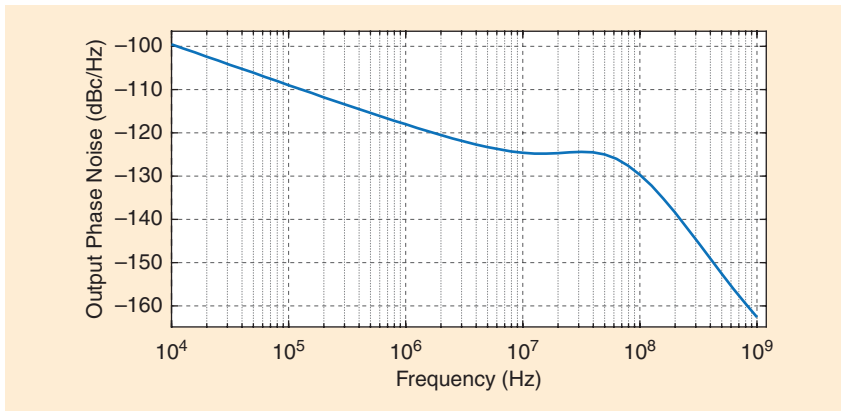


FIGURE 22: The output PN of the second scaled loop.

where $\overline{I_n^2}$ denotes the white noise of each CP current source, and T_{res} denotes the minimum pulsewidth of the up and down pulses. Also, $\overline{I_n^2} = 4kT\gamma g_m$, where $k = 1.38 \times 10^{-23} \text{ J}\cdot\text{K}$ and T is the temperature. Writing $g_m = (2I_P)/(V_{GS} - V_{TH})$, we have

$$S_{\phi,CP}(f) = (4\pi^2 N^2) \frac{16kT}{I_P(V_{GS} - V_{TH})} \cdot \frac{T_{res}}{T_{REF}} \quad (12)$$

From Figure 16(c), $T_{res} \approx 25 \text{ ps}$. Since $I_P = 0.5 \text{ mA}$, $V_{GS} - V_{TH} \approx 200 \text{ mV}$, $N = 8$, and $T_{REF} = 1/(3.75 \text{ GHz})$, we obtain

$$S_{\phi,CP}(f) = -128 \text{ dBc/Hz} \quad (13)$$

This means that the CP thermal noise dominates the output, a troublesome point to which we return later. We can also refer this amount to the input by subtracting $20 \log 8 = 18 \text{ dB}$, obtaining -146 dBc/Hz .

We recognize from Figure 18 that the PN falls at a rate of 10 dBc/Hz from $f = 10 \text{ kHz}$ to $f = 1 \text{ MHz}$. Such a signature stems from the flicker noise of the CP rather than from that of the VCO.

To compute the jitter, we find the area under the profile of Figure 18 and double it to account for the PN on both sides of the carrier:

$$\Delta T_j = \frac{\sqrt{2 \int_{10 \text{ kHz}}^{1 \text{ GHz}} S_{\phi}(f) df}}{2\pi} T_{VCO} \quad (14)$$

We have $\Delta T_j = 41 \text{ fs}_{rms}$. Note that this amount does not include the reference PN. According to our previous projection, this value translates to a jitter of $\sqrt{K} \times 41 \text{ fs}_{rms} = 250 \text{ fs}_{rms}$ for the unscaled synthesizer. It appears that the design fails to meet our target even if the reference contribution is neglected.

Second Scaled Loop

Despite missing our target specification, we continue our loop scaling efforts to see whether the parameters vary according to our projections. We now select $N = 16$, $K = 18.75$, $C_1 = 810 \text{ fF}$, $C_2 = 27 \text{ fF}$, and $f_{REF} = 1.875 \text{ GHz}$ (Figure 19). A transient simulation produces the

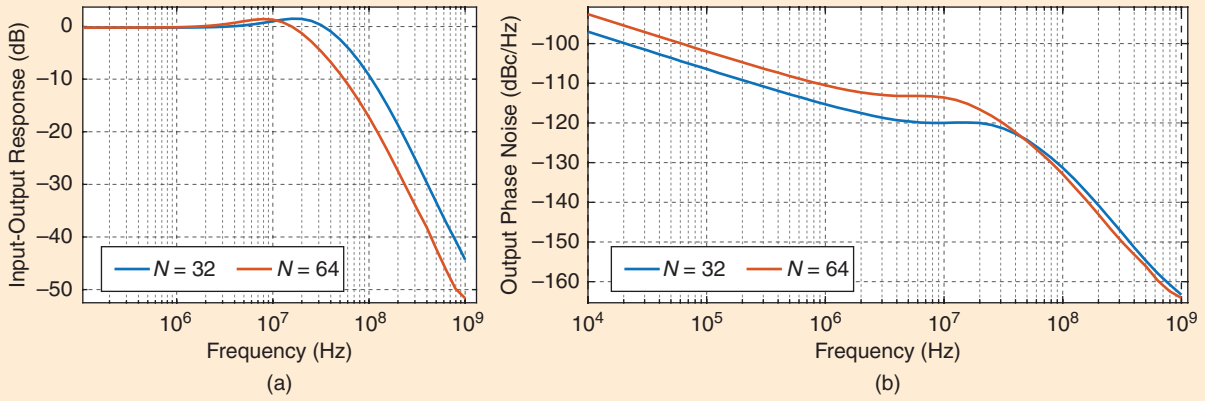


FIGURE 23: (a) The input-output responses of third and fourth scaled loops and (b) corresponding PN profiles.

settling behavior of Figure 20(a) and the output spectrum of Figure 20(b). The spur level is -52 dB, fairly consistent with our conjecture that it should remain constant.

Plotted in Figure 21 is the input-output response, displaying a BW of 103 MHz and suggesting that it is not quite halved with respect to the first scaled loop. The peaking is about 2.1 dB.

Figure 22 shows the output PN with a plateau value of -125 dBc/Hz. From (11), this should be equal to -123 dBc/Hz because N is doubled. The 2-dB discrepancy may be avoided if the number of sidebands in the pnoise analysis is increased. Integrating this profile yields a jitter of 47 fs, which is 15% (rather than a factor of $\sqrt{2}$) greater than that in the previous case.

Third and Fourth Scaled Loops

To form a clearer picture of the trends, we study two more cases with $N = 32$ and $N = 64$. For the former, we select $C_1 = 1.62$ pF, $C_2 = 54$ fF, and $f_{\text{REF}} = 937.5$ MHz. For the latter, we have $C_1 = 3.24$ pF, $C_2 = 108$ fF, and $f_{\text{REF}} = 468.75$ MHz. According to transient simulations, the output spur level remains around -51 dB.

Plotted in Figure 23(a) are the input-output responses for the two cases, yielding $f_{\text{BW}} = 54$ MHz and 26 MHz, respectively. We observe

We can return to the original loop bandwidth calculations; assume an S_{REF} dominated by the CP and reduce f_{BW} accordingly.

that the bandwidth is scaled with reasonable accuracy. Figure 23(b) depicts the output PN profiles and suggests a plateau value of -120 dBc/Hz for $N = 32$ and -113 dBc/Hz for $N = 64$. These results are fairly aligned with $S_{\phi, \text{CP}} \propto N^2$

in (11). The integrated jitter values amount to 60 fs_{rms} and 90 fs_{rms}, respectively. The scaling of the jitter is now somewhat close to the theoretical factor of \sqrt{K} .

Let us project the jitter of the unscaled loop from our last case: $\Delta T_j = 90 \text{ fs} \times \sqrt{300/64} = 195 \text{ fs}_{\text{rms}}$. We may expect that the reference PN will elevate this value considerably. However, recall from previous sections that the input-referred CP contribution is around -146 dBc/Hz, far exceeding our presumed $S_{\text{REF}} = -170$ dBc/Hz. Thus, the unscaled loop still exhibits a jitter of about 200 fs_{rms}.

The jitter that we have obtained is not minimum. We can return to the original loop bandwidth calculations; assume an S_{REF} dominated by the CP and reduce f_{BW} accordingly.

The cost is a larger area occupied by the capacitors.

References

- [1] B. Razavi, "The design of a millimeter-wave VCO [The Analog Mind]," *IEEE Solid-State Circuits Mag.*, vol. 14, no. 3, pp. 6–12, Summer 2022, doi: 10.1109/MSSC.2022.3184443.
- [2] B. Razavi, "The design of a millimeter-wave frequency divider [The Analog Mind]," *IEEE Solid-State Circuits Mag.*, vol. 14, no. 4, pp. 6–16, Fall 2022, doi: 10.1109/MSSC.2022.3205805.
- [3] D. Liao, Y. Zhang, F. F. Dai, Z. Chen, and Y. Wang, "An mm-wave synthesizer with robust locking reference-sampling PLL and wide-range injection-locked VCO," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 536–546, Mar. 2020, doi: 10.1109/JSSC.2019.2959513.
- [4] D. Yang et al., "A harmonic-mixing PLL architecture for millimeter-wave application," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3552–3566, Dec. 2022, doi: 10.1109/JSSC.2022.3209614.
- [5] T. Siriburanon et al., "A low-power low-noise mm-wave subsampling PLL using dual-step-mixing ILFD and tail-coupling quadrature injection-locked oscillator for IEEE 802.11ad," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1246–1260, May 2016, doi: 10.1109/JSSC.2016.2529004.
- [6] A. Homayoun and B. Razavi, "Analysis of phase noise in phase/frequency detectors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 3, pp. 529–539, Mar. 2013, doi: 10.1109/TCSI.2012.2215792.
- [7] B. Razavi, *Design of CMOS Phase-Locked Loops*. Cambridge, U.K.: Cambridge Univ. Press, 2020.
- [8] C. S. Vacher et al., "A family of low-power truly modular programmable dividers in standard 0.35- μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1039–1045, Jul. 2000, doi: 10.1109/4.848214.

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