RF CMOS Transceivers for Cellular Telephony

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ABSTRACT

This article describes system and circuit issues related to cellular transceivers, presenting design techniques that have provided high performance in CMOS technology. Following an overview of relevant GSM and WCDMA specifications, the article identifies four trends in RF design that have continued to improve the performance. Examples of CMOS transceivers, and circuit and device concepts are then described that meet the stringent requirements of cellular telephony.

INTRODUCTION

Two decades after its introduction, the cellular telephone continues to evolve, providing higher performance and greater functionality at a constant or even decreasing cost. The electronic section of a cell phone has gone from almost entirely discrete implementations in the early 1980s to three- or four-chip solutions today, aiming for single-chip realizations this decade.

This article deals with the problem of radio frequency (RF) transceiver design in complementary metal oxide semiconductor (CMOS) technology, emphasizing the challenges in meeting the requirements of cellular standards such as Global System for Mobile Communications (GSM) and wideband code-division multiple access (WCDMA). Following a review of specific design issues, we identify four trends that have significantly contributed to the success of RF CMOS circuits. Next, we describe examples of cellular transceivers and study RF device and circuit configurations in CMOS technology.

DESIGN ISSUES

Before focusing on challenges in CMOS technology, it is instructive to establish a background based on transceiver design considerations. Some of the system-level design parameters of RF transceivers are summarized in Fig. 1. As consumer products, cell phones principally compete on the basis of cost, and, as heavily used portable devices, power consumption. Weight and form factor also play a (mostly psychological) role in consumers' decisions.

As the major contributor to the cost, the electronic circuitry in a cell phone has evolved tremendously: the number of external components has fallen from hundreds in the early 1990s to tens today; many high-cost and expensive external components (e.g., discrete filters) have been eliminated and much greater functionality has been added to support modern communication standards. In addition to lowering the cost, this evolution has also reduced the power consumption, form factor, and weight of the handset.

The drive for lower cost and hence system-on-chip (SoC) design has inevitably brought up CMOS technology as a serious contender. The cost of low-complexity subcircuits such as amplifiers and mixers is determined by primarily packaging and testing, rather than chip area. On the other hand, with single-chip transceivers and the prospect of integrating the digital baseband processor along with the RF and analog functions, the cost equation is heavily weighted by the chip area and therefore the integrated circuit (IC) technology.

Shown in Fig. 1, the transceiver performance metrics that present difficult challenges are as follows. In the receive (RX) path, the sensitivity is given by the noise figure (NF) (approximately 8 dB in GSM[1] and 6.5 dB in WCDMA) and the tolerance of interferers (*blockers*). In the transmit (TX) path, the efficiency of the power amplifier (especially in WCDMA, where the linearity is also critical) constitutes the principal issue. Moreover, the thermal noise generated by a GSM transmitter in the receive band must be sufficiently low to negligibly corrupt other users' reception. In WCDMA, leakage of the TX output to the RX input heavily desensitizes the receiver because the two paths must operate concurrently,[2] therefore requiring a high linearity even in the front-end low-noise amplifier (LNA). The frequency synthesizer driving the RX and TX paths must also meet tough specifications. The output phase noise and sidebands of the synthesizer determine the tolerance to large blockers.

The use of CMOS technology to satisfy the above requirements has entailed extensive research on architectures, circuits, and devices. While more linear than bipolar transistors, MOS

[1] *Depending on the type of baseband demodulator, the required noise figure may need to be a few decibels lower.*

[2] *Concurrent operation provides continuous feedback between the base station and the mobile, allowing precise control of the TX output power.*

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field effect transistors (MOSFETs) suffer from more severe trade-offs between noise and power dissipation and speed and power dissipation. To relax this power penalty, new techniques at all levels of abstraction have been invented. It is important to make the following observations:

- The comparatively high thermal noise of MOSFETs makes it difficult to achieve a low noise figure (e.g., below 2.5 dB) with low power consumption. Fortunately, modern RF transceivers draw on concurrent system and circuit design, compensating for the shortcomings of one with the advantages of the other. For example, if the overall RX noise figure must not exceed 6.5 dB, an LNA NF of 2.5 dB is quite reasonable provided the gain and noise figure are properly distributed along the RX chain. Taking into account the nonlinearity of each stage, the distribution often requires trial and error and the use of level charts [1].
- The high flicker (1/f) noise of short-channel MOS devices both corrupts the signals downconverted to the baseband and gives rise to higher close-in phase noise in oscillators. These issues are resolved by proper choice of RX and synthesizer architectures.
- Many speed limitations of MOSFETs can be alleviated through the use of on-chip inductors and transformers.
- The larger mismatches between nominally-identical MOS devices results in phase and gain mismatch in transceivers. This effect is remedied by analog or digital calibration techniques.

Design Techniques

Over the past 10 years, the RF design paradigm has followed four important trends:

- Due to the integration capabilities of CMOS technology, RF transceiver architectures have markedly departed from the conventional heterodyne approach, including far greater on-chip complexity in favor of minimizing the number of external components.

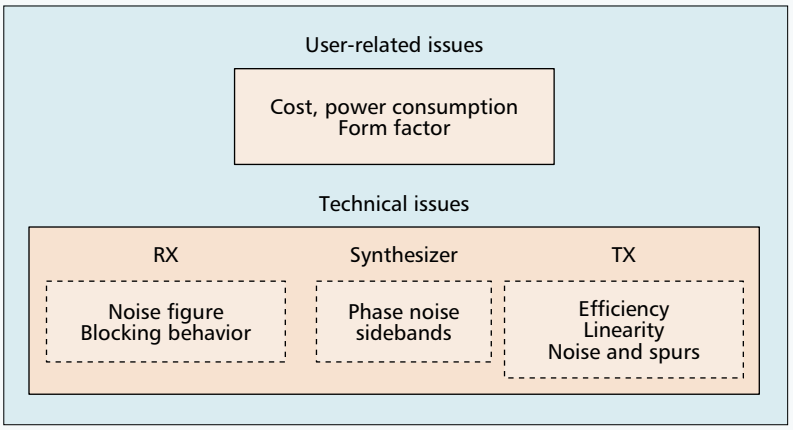

Figure 1. *RF transceiver design parameters.*

- High-resolution low-power analog-to-digital converters employing new methods of improving the dynamic range have emerged as an integral part of transceivers.
- Numerous low-voltage low-noise RF and baseband circuit techniques have been invented that circumvent the limitations of MOS transistors.
- Extensive research on passive monolithic devices such as inductors and varactors has led to accurate models and hence ease of use in circuit design.

In this section, we present design techniques that exemplify the above trends.

Transceiver Architectures

Figure 2 shows a heterodyne GSM transceiver introduced in the early 1990s [2]. The receiver downconverts the 900 MHz input to an intermediate frequency (IF) of 71 MHz and subsequently to baseband. The transmitter directly upconverts the baseband signal to RF using a carrier generated by mixing the outputs of two voltage-controlled oscillators, VCO_1 and VCO_2. Since the power amplifier (PA) output spectrum lies far from the operation frequencies of the VCOs, no injection pulling occurs.

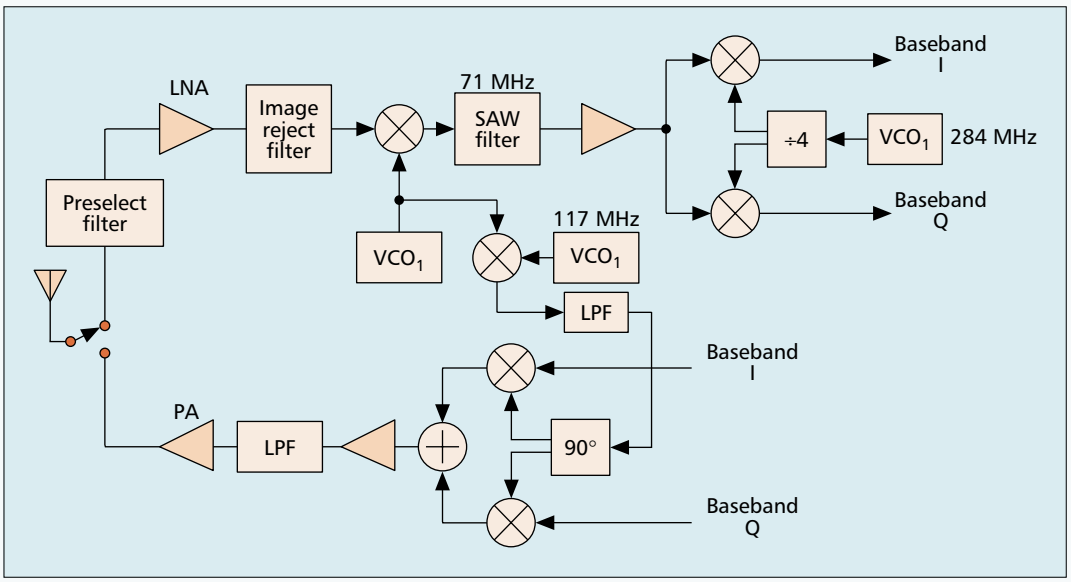

Figure 2. *An example of an early GSM transceiver.*

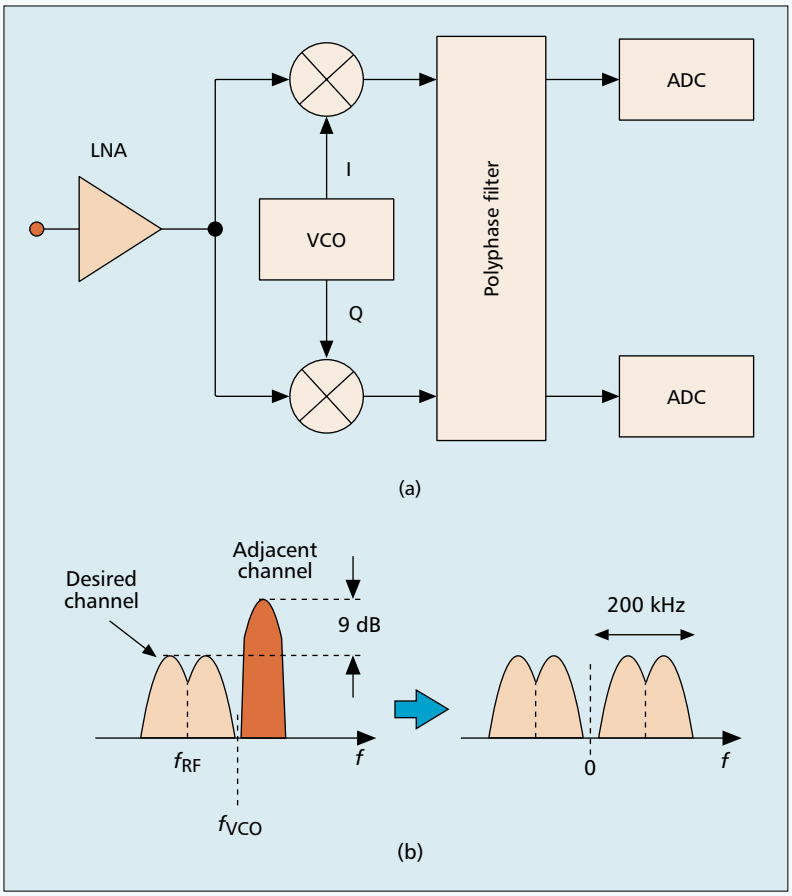

Figure 3. *a) Low-IF receiver architecture; b) input and output spectra.*

The transceiver of Fig. 2 suffers from a number of drawbacks:

- The image-reject and IF filters are bulky, expensive, low-impedance devices that raise the power dissipation in the LNA and the first mixer, respectively.[3]
- The transmitter chain amplifies the thermal noise of the upconversion mixers, thereby producing at the antenna an unacceptably high noise in the receive band unless the antenna switch is replaced by a bulky, lossy, and expensive duplex filter.

Now consider the receiver shown in Fig. 3a. Based on a "low-IF" architecture, the RX translates the desired RF channel to a center frequency of 100 kHz (Fig. 3b), positioning the image in the adjacent channel. The quadrature mixers and the subsequent stage (e.g., a polyphase filter) reject the image by a factor determined by the matching properties of the VCO phases and the other circuits in the signal path, typically about 20–30 dB. This level of image rejection is acceptable here because the GSM standard allows an adjacent-channel power at most 9 dB higher than the desired signal.

The low-IF receiver architecture is particularly suited to CMOS implementation of GSM receivers because:

- GSM's relaxed adjacent channel rejection tolerates the relatively large mismatches of MOS devices
- The translation of the desired channel (200 kHz wide) to a center frequency of 100 kHz lowers the power of 1/f noise (by about 4.7 dB).
- A high-pass filter can be used after downconversion to remove the large dc component that results from the self-mixing of the VCO output.[4]

In contrast, if the desired channel were translated to a center frequency of zero (direct conversion), both 1/f noise and dc offset removal would prove extremely difficult.

The low-IF architecture does share one issue with its direct conversion counterpart: even-order distortion in the RF path may create a low-frequency beat from two large interferers (or demodulate an amplitude-modulated interferer), with the result leaking to the baseband if the mixers or VCO signals suffer from asymmetries. This issue is resolved by various circuit techniques. Examples include differential RF circuitry and high-pass filtering before the downconversion mixer [4].

While the VCO frequency in Fig. 3a may fall relatively close to the output spectrum of the transmit path, GSM avoids the problem of oscillator injection pulling by inserting an offset between RX and TX time slots so that the two paths do not operate concurrently.

Figure 4 depicts a transmitter architecture [5, 6] for constant envelope modulation schemes such as Gaussian minimum shift keying (GMSK), which is used in GSM. The objective is to minimize the amplification of the wideband noise generated by the quadrature upconversion mixers MX_1 and MX_2. The upconverted signal X_1 is applied to a phase-locked loop (PLL) consisting of a phase/frequency detector (PFD), a low-pass filter (LPF), a VCO, an offset mixer MX_3, and a 90° phase splitter. When locked, the loop forces the phase difference between X_1 and f_{REF} to zero by modulating ϕ_1 and ϕ_2 just to cancel the phase variation of x_1 and x_Q. Thus, the VCO output also experiences a phase modulation equal and opposite to that of the baseband signals. The key point here is that with proper choice of the loop bandwidth, the wideband noise of MX_1 and MX_2 is suppressed, leaving the VCO as the primary contributor of thermal noise in the RX band. Consequently, the duplexer filter at the TX output can be replaced with a low-loss switch. In practice, frequency dividers may precede the inputs of the PFD to allow more flexibility in frequency planning.

We now consider transceivers for WCDMA applications. Low-IF reception proves difficult in this case as the adjacent channel rejection must exceed 35 dB, demanding tight I and Q matching. On the other hand, the wide channel bandwidth (5 MHz) makes direct conversion attractive because the flicker noise spectrum occupies only a fraction of the downconverted channel (±2.5 MHz). Figure 5a shows an example [7] where a chain consisting of a duplexer filter, two LNAs, and an RX filter precede quadrature downconversion mixers, baseband filtering, and variable gain amplifiers. As mentioned earlier, since the RX and TX operate concurrently, the leakage of the TX output to the RX path must be minimized. In the architecture of Fig. 5a, both the duplexer and the (off-chip) RX filter provide the necessary suppression. Alternatively, the RX can

[3] Even a $2 filter may be considered objectionable by manufacturers.

[4] The filter must still pass frequencies above a few tens of kilohertz, but circuit techniques can accommodate such a low corner frequency with no off-chip capacitors [3].

be designed for an overall 1-dB compression point higher than –18 dBm to eliminate the external filter.

In the receiver of Fig. 5a, the local oscillator (LO) runs at twice the desired channel frequency, and a divide-by-two circuit produces the I and Q phases. This practice is common both for quadrature LO generation and to avoid injection pulling of the LO by the TX output. The design achieves a noise figure of 6.5 dB (averaged over 10 kHz to 1.92 MHz) while consuming 45 mW from a 1.5 V supply in 0.13 µm CMOS technology. The RX has an input third intercept point (IP_3) of –8 dBm with an overall gain variable between 16.5 and 87.5 dB.

Figure 5b depicts a WCDMA transmitter designed in conjunction with the above receiver [8]. Using direct upconversion for simplicity, the design must deal with the problem of carrier leakage to the output, an undesirable effect because the LO/2 frequency falls in the middle of the output spectrum, distorting the signal constellation and raising the error vector magnitude (EVM). The TX therefore employs a calibration loop that measures the output in the absence of baseband signals (i.e., during power up) and introduces finely controlled offsets in the baseband amplifiers and upconversion mixers, thereby suppressing the carrier leakage. Realized in 0.13 µm CMOS technology, the transmitter delivers an output power of +2.5 dBm with an out-of-band noise of approximately –150 dBc/Hz. Consuming 68 mW from a 1.5 V supply, the circuit exhibits a carrier leakage of –35 dBc and an EVM of 4.3 percent.

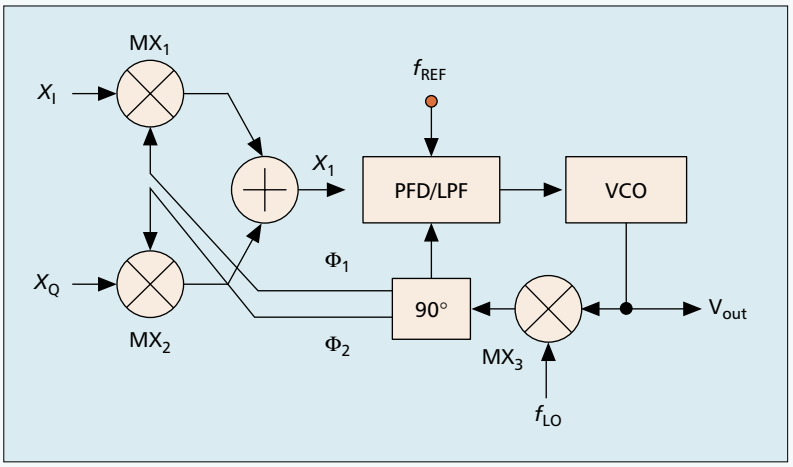

Figure 4. *Offset-PLL TX architecture [5, 6].*

A/D Converters

The complexity of modern communication standards requires that operations such as equalization and detection be performed in the digital domain. Furthermore, many functions that were

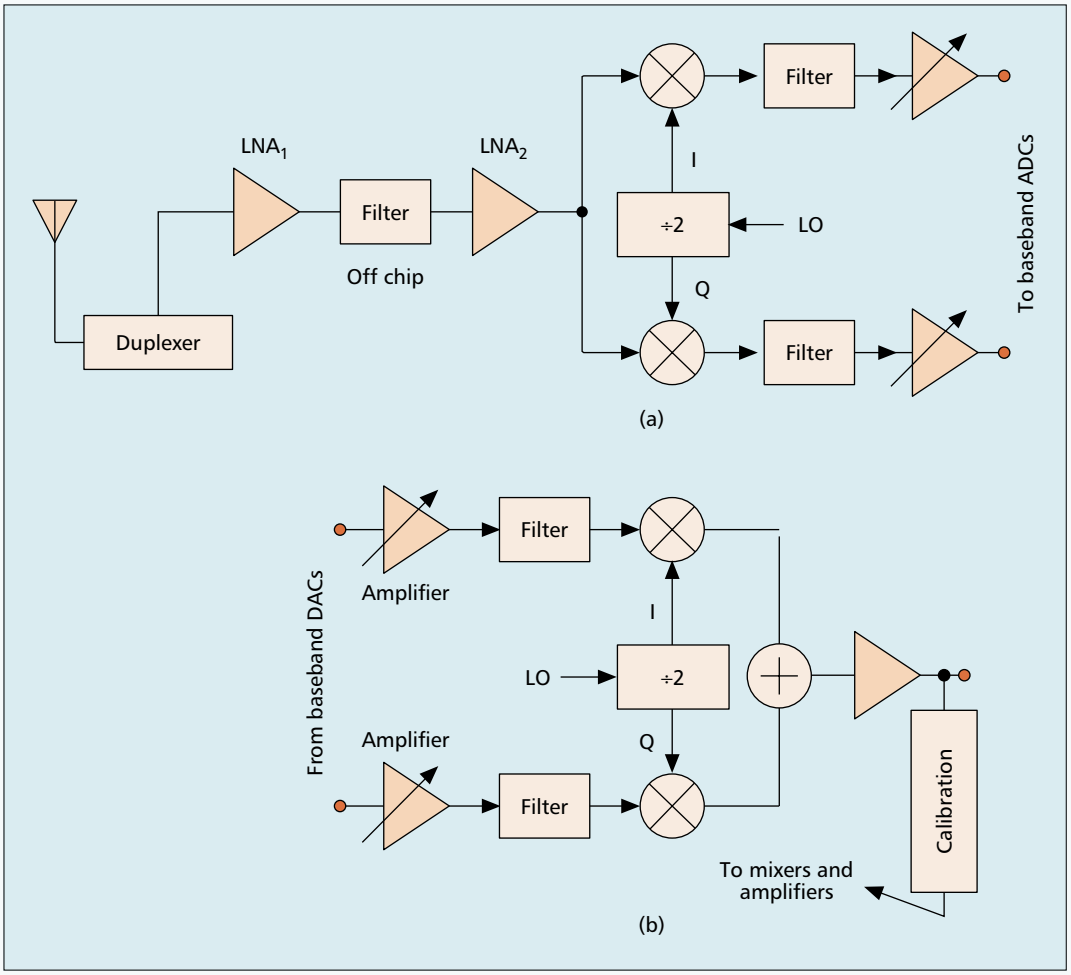

Figure 5. *a) Receiver and b) transmitter architectures for WCDMA [7, 8].*

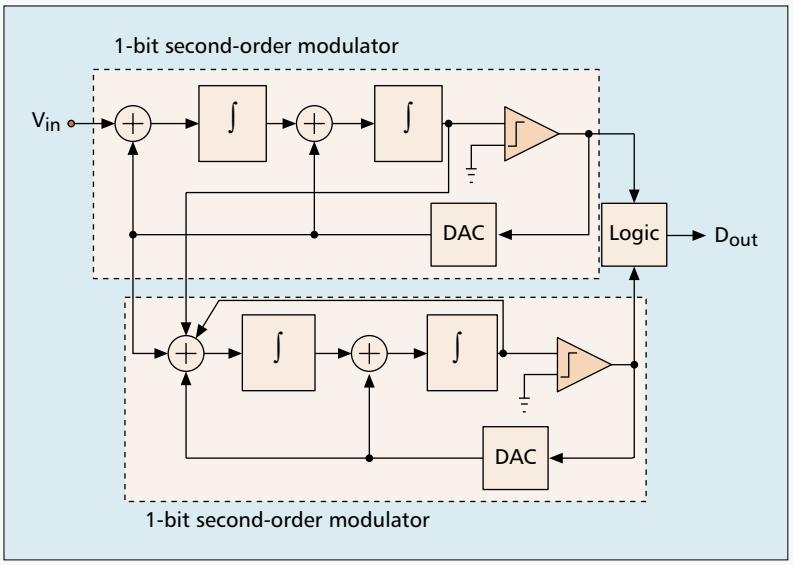

Figure 6. *A fourth-order Σ-Δ modulator for GMS receivers.*

traditionally realized in the analog domain (e.g., channel-selection filtering, frequency offset cancellation, and automatic gain control) can be implemented digitally if baseband A/D converters provide sufficient dynamic range. For these reasons, considerable research effort has been expended on improving the performance of data converters for wireless applications.

With the relative ease of realizing functions digitally, it is desirable to push the analog-to-digital interface toward the antenna. However, both the resolution and the speed required of the ADC must rise, eventually approaching infeasible levels or demanding greater power dissipation than the analog counterparts. The interface has therefore remained at relatively low frequencies, a few tens of megahertz in most cases. The advances in RF and ADC technologies may gradually shift this interface to higher frequencies, but direct digitization at the antenna appears to be an unlikely or nonoptimum solution.

Figure 6 shows an example of a low-power A/D converter designed for low-IF GSM receivers [9]. The converter employs a cascade of two 1-bit second-order oversampling Σ-Δ modulators, achieving stability while requiring reasonable capacitor matching. Oversampling the input signal by a factor of 32, the circuit suppresses the quantization noise to below the thermal noise of the first integrator, thereby reaching a dynamic range of 84 dB for an input bandwidth of 190 kHz. With a power dissipation of 5 mW from a 1.8 V supply, the converter makes it possible to replace the power-hungry polyphase filters in Fig. 3 with relaxed filtering, deferring channel selection to the digital domain. The front-end LNA and mixers must nonetheless provide a gain of about 40 dB to raise the input signal to well above the noise floor of the converter.

Circuits and Devices

The effort to achieve high RF performance in CMOS technology has extended to the circuit and device levels as well. A particularly challenging problem relates to the design of VCOs that must satisfy the stringent close-in and far-out phase noise specifications of GSM (Fig. 7a). Figure 7b shows an example of a high-performance CMOS LC VCO [10]. The circuit consists of two oscillators coupled to each other so as to operate in quadrature, thus obviating the need for 90° phase splitters or frequency dividers. Each oscillator incorporates cross-coupled N-channel MOS (NMOS) and PMOS pairs to create a negative resistance, replenishing the energy lost in the tank in each oscillation cycle.

Several aspects of this design lead to low phase noise. First, the use of both PMOS and NMOS devices allows *shaping* the rising and falling transitions of the waveform, thereby lowering the upconversion of device 1/f noise [11]. Second, the use of a differential inductor (Fig. 7c), rather than two asymmetric spirals, achieves a higher quality factor [12]. Third, the octagonal shape reduces the series resistance for a given inductance.[5] Fourth, MOS varactors provide a wider tuning range than pn junctions. Shown in Fig. 7d, such varactors do not experience forward bias and exhibit a sharper capacitance-voltage characteristic.

Designed in 0.25 mm CMOS technology and operating at 1.8 GHz, the VCO exhibits a phase noise of –132 dBc/Hz at 600 kHz offset and –143 dBc/Hz at 3 MHz offset, well exceeding GSM specifications. The circuit provides a tuning range of 17 percent and consumes 20 mW from a 2.5 V supply. This level of performance would have been quite difficult to obtain without the above four circuit and device techniques. The tuning range proves sufficient if the inductor and varactor models are accurate, but an array of small capacitors can also be added to each tank, thereby providing discrete steps in the frequency and hence a wider tuning range.

The circuit of Fig. 7b nonetheless suffers from supply dependence as it does not define the bias currents by means of constant current sources. As a result, the oscillator may translate supply noise to phase noise or spurs. Interestingly, with the advent of monolithic inductors, it is conceivable that a spiral inductor and a capacitor can form an on-chip supply filter, suppressing the noise. Large values of inductance necessary for this task can be accommodated in a small area through the use of stacked structures [13].

Conclusion

CMOS technology has gradually found its way into the cellular telephony as well as wireless local area networks, GPS receivers, and other RF applications. The potential of CMOS devices for stringent RF circuits became apparent around the 0.5 μm generation, materializing as the devices scaled down further and the system and circuit designers' understanding continued to improve. The entry barrier into CMOS technology still remains somewhat high due to concerns regarding the time to market and technology risk factors, but many companies have successfully introduced such products in the market.

One area in which CMOS technology has proven less efficient than silicon bipolar or III-V devices is power amplifiers. While nonlinear PAs with reasonable efficiency have been reported in CMOS processes, the design of linear high-effi-

[5] *The spiral's linewidth is also tapered down from outer turns to inner turns to reduce the series resistance further [10].*

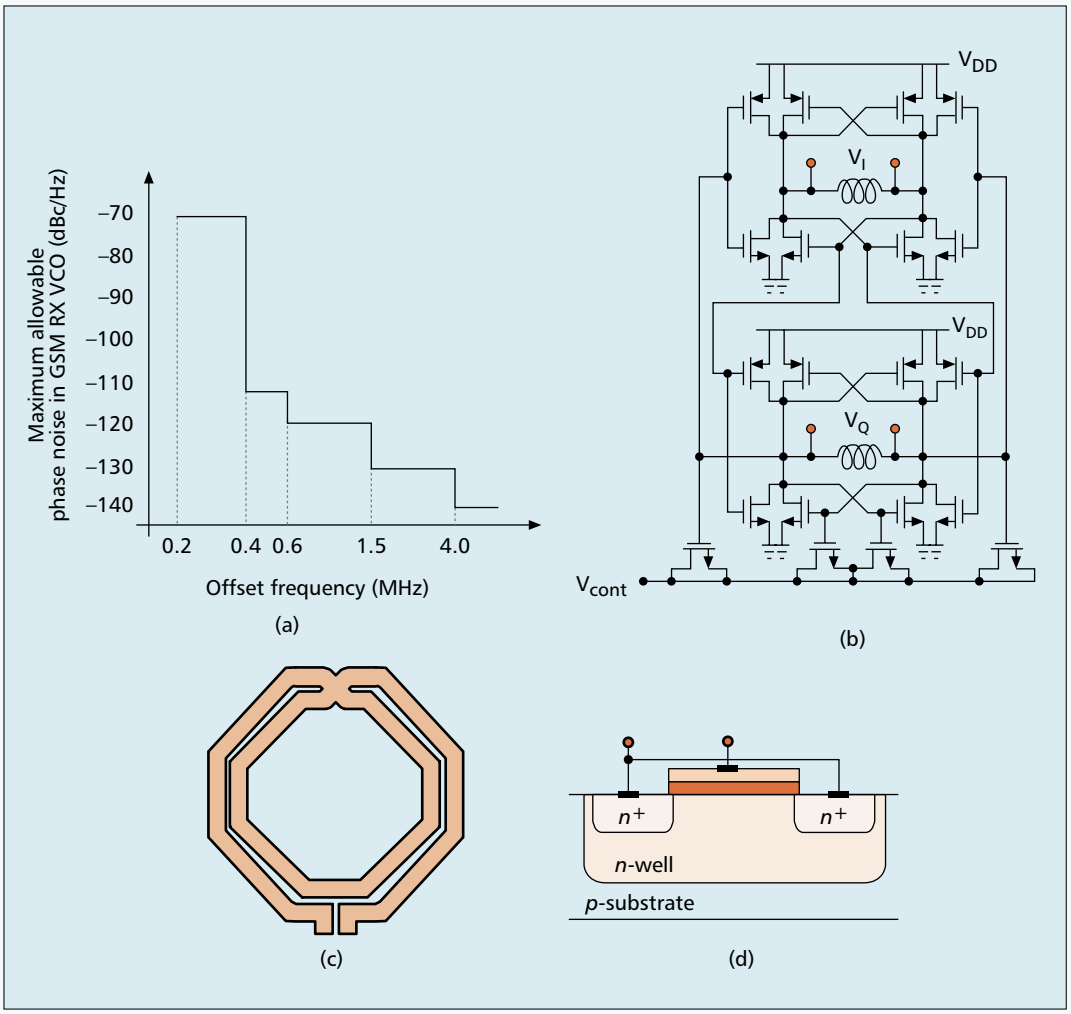

Figure 7. *a) GSM phase noise requirements of an RX oscillator; b) quadrature CMOS VCO; c) differential spiral inductor; d) MOS varactor.*

The entry barrier into CMOS technology still remains somewhat high due to concerns regarding the time to market and technology risk factors, but many companies have successfully introduced such products in the market.

ciency PAs for RF applications such as CDMA and orthogonal frequency-division multiplexing remains unresolved.

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Biography

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