A Study of Injection Locking in Oscillators and Frequency Dividers

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***Abstract*— A time-variant model provides a framework for understanding and modeling injection locking in oscillators and frequency dividers. Application of the model offers new insights and allows optimization for lock range and power consumption. Two prototypes with no tuning are realized in 28-nm CMOS technology. The first operates from 26 to 63 GHz while drawing 1.88 mW. The second achieves a range of 24–73 GHz with a power consumption of 4.76 mW.**

***Index Terms*— Frequency divider, injection locking, lock range, oscillator, time variant.**

I. Introduction

INJECTION locking finds application in high-speed systems where frequencies of interest challenge designers. For example, clock generation for wireline transmitters operating at 112 or 224 Gb/s relies on phase-locked loops (PLLs) that run at 28 or 56 GHz, depending on the serialization approach [1], [2], [3]. In addition, wireless transceivers targeting 5G systems require quadrature local-oscillator (LO) phases at 24 to 40 GHz [4], calling for robust frequency dividers that cover an input range of 48–80 GHz. For this reason, considerable efforts have been expended to widen such dividers' lock range [5], [6], [7], [13].

The principal drawback of injection locking relates to the narrow frequency range that it provides and hence the need for various tuning techniques [9], [10], [11], [12]. Unfortunately, as shown in this article (Appendix A), a PLL employing an injection-locked frequency divider (ILFD) may experience *false lock*, thereby deceiving the tuning algorithm. For this reason, it is desirable to develop ILFDs that achieve a wide *untuned* lock range.

Prior work on injection locking has significantly advanced our understanding of this phenomenon [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25]. For example, Hong and Hajimiri [21] introduced a phasor-based analysis with two assumptions: 1) the oscillator transconductance current has a constant amplitude that does not depend on the output voltage amplitude and 2) the injection is a current with a fundamental component independent of the output voltage amplitude. The switch-based topology of interest to us requires that we lift these restrictions. To this end, we express both the negative transconductance and the injector switch conductance as Fourier series. Another framework proposed in [22] and [23] employs the impulse sensitivity function (ISF), arriving at general explanations for injection locking and pulling. While providing new insights about injection locking and pulling phenomena, this approach also relies on two assumptions. First, the charge injected into the oscillator's load is much less than the maximum charge swing. This point does not hold in our circuits as, to achieve a wide lock range, we make the injection current comparable to the transconductance current. Second, similar to [21], the injection current is assumed independent of the output voltage swing.

This article proposes a time-variant model that offers new insights and leads to the design of broadband ILFDs. Two divider prototypes fabricated in 28-nm CMOS technology demonstrate the utility of the model and exhibit lock ranges from 26 to 63 GHz and from 24 to 73 GHz with no need for tuning [26].

Section II presents our proposed model for oscillators. Section III applies the framework to dividers, and Section IV extends it to quadrature coupling. Sections V and VI deal with the circuit implementation and experimental results, respectively.

II. Time-Variant Oscillator Model

Consider the basic cross-coupled oscillator shown in Fig. 1(a), where $I_1(t) = I_{\text{inj}} \cos(\omega_{\text{inj}} t)$ represents the injected signal. We assume that the oscillator is locked. With typical tank quality factor (Q) values, the differential output voltage can be approximated as $V_{XY}(t) = V_0 \cos(\omega_{\text{inj}} t + \phi)$. The circuit provides a negative transconductance, $G_m(t) = dI_{G_m}/dV_{\text{out}}$, which varies periodically with time and can therefore be expanded in a Fourier series [27]

$$G_m(t) = G_{m0} + 2\sum_{n=1}^{\infty} G_{m,2n} \cos\big(2n\omega_{\text{inj}} t + 2n\phi\big). \tag{1}$$

We now construct three equations with the aid of the equivalent circuit shown in Fig. 1(b). First, we have $dI_{G_m} = G_m(t) dV_{\text{out}}$, and hence,

$$\begin{aligned} I_{G_m}(t) &= \int G_m(t) \frac{dV_{\text{out}}}{dt} dt \\ &= -V_0 \omega_{\text{inj}} \int G_m(t) \sin\big(\omega_{\text{inj}} t + \phi\big) dt. \end{aligned} \tag{2}$$

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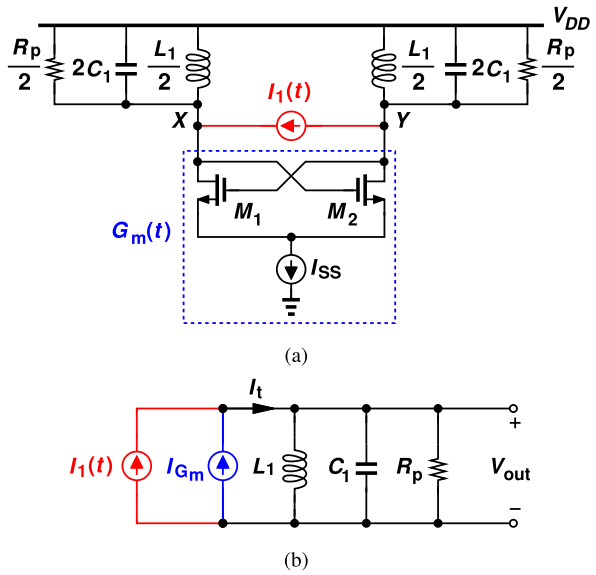


Fig. 1. (a) Cross-coupled oscillator with a current injected to its output and (b) its time-variant equivalent model.

Since we are interested in the first harmonic of $I_{G_m}(t)$ in (2), we write $G_m(t) \approx G_{m0} + 2G_{m2}\cos(2\omega_{\text{inj}}t + 2\phi)$, obtaining

$$I_{G_m}(t) \approx (G_{m0} - G_{m2})V_0 \cos\big(\omega_{\text{inj}}t + \phi\big). \tag{3}$$

Second, we express the tank current, I_t, as

$$I_t(t) = \frac{V_0}{R_p}\cos\big(\omega_{\text{inj}}t + \phi\big) + \frac{V_0}{L_1\omega_{\text{inj}}}\sin\big(\omega_{\text{inj}}t + \phi\big) - V_0C_1\omega_{\text{inj}}\sin\big(\omega_{\text{inj}}t + \phi\big). \tag{4}$$

Third, we write the injected current in the form

$$I_1(t) = I_{\text{inj}}\cos\phi\cos\big(\omega_{\text{inj}}t + \phi\big) + I_{\text{inj}}\sin\phi\sin\big(\omega_{\text{inj}}t + \phi\big). \tag{5}$$

Noting that in Fig. 1(b), $I_t(t) = I_{G_m}(t) + I_1(t)$, we have

$$\begin{aligned}&(G_{m0} - G_{m2})V_0\cos\big(\omega_{\text{inj}}t + \phi\big) + I_{\text{inj}}\cos\phi\cos\big(\omega_{\text{inj}}t + \phi\big) + I_{\text{inj}}\sin\phi\sin\big(\omega_{\text{inj}}t + \phi\big)\\ &= \frac{V_0}{L_1\omega_{\text{inj}}}\sin\big(\omega_{\text{inj}}t + \phi\big) - V_0C_1\omega_{\text{inj}}\sin\big(\omega_{\text{inj}}t + \phi\big) + \frac{V_0}{R_p}\cos\big(\omega_{\text{inj}}t + \phi\big).\end{aligned} \tag{6}$$

This equation must hold at all times, e.g., at $t = (2\pi - \phi)/\omega_{\text{inj}}$ and at $t = (\pi/2 - \phi)/\omega_{\text{inj}}$, yielding

$$G_{m0} - G_{m2} + \frac{I_{\text{inj}}}{V_0}\cos\phi = \frac{1}{R_p} \tag{7}$$

$$\frac{I_{\text{inj}}}{V_0}\sin\phi = -\Delta\omega C_1\left(\frac{\omega_{\text{inj}} + \omega_0}{\omega_{\text{inj}}}\right), \tag{8}$$

where $\Delta\omega = \omega_{\text{inj}} - \omega_0$ and $\omega_0 = 1/\sqrt{L_1C_1}$. Equations (7) and (8) are the fundamental equations governing the oscillator under injection. Interestingly, (7) can also be proved by invoking the law of conservation of energy (Appendix B).

As ω_{inj} changes, the oscillator regulates V_0 and ϕ such that both (7) and (8) remain satisfied. Note that a change in V_0 translates to one in $G_{m0} - G_{m2}$ [27]. The results expressed by (7) and (8) present refinements to those obtained in prior work. Specifically, if $\phi = 90°$, then $G_{m0} - G_{m2} = 1/R_p$, whereas Razavi [17] suggested that $G_{m0} = 1/R_p$. Also, if $\phi = 0$, then $G_{m0} - G_{m2} - 1/R_p = -I_{\text{inj}}/V_0$, whereas Razavi [17] prescribed that $G_{m0} - 1/R_p = -I_{\text{inj}}/V_0$. The large-signal transconductance, $G_{m0} - G_{m2}$, varies across the lock range. According to (8), as $\Delta\omega$ changes, so does ϕ, obligating a change in $G_{m0} - G_{m2}$ in order for (7) to be satisfied. The change in the effective transconductance is made possible by the change in the output amplitude, a result revealed by our Fourier series expansion of the cross-coupled pair's transconductance. This interdependence has also been observed in [16] and [21], by means of phasor analysis and in [23] by means of an analysis framework based on the ISF.

It is possible to further simplify (7) and (8). If M_1 and M_2 in Fig. 1(a) experience complete switching, then I_{G_m} in Fig. 1(a) is a square-wave toggling between 0 and $+I_{\text{SS}}$ in each branch, which translates to $-I_{\text{SS}}/2$ and $+I_{\text{SS}}/2$ in the equivalent differential model of Fig. 1(b). The first harmonic of this current is then given by $(2/\pi)I_{\text{SS}}\cos(\omega_{\text{inj}}t + \phi)$ and must be equal to I_{G_m} in (3). It follows that:

$$G_{m0} - G_{m2} = \frac{2I_{\text{SS}}}{\pi V_0}. \tag{9}$$

Moreover, for an input frequency range as wide as $0.5\omega_0$ to $2\omega_0$, the term $(\omega_{\text{inj}} + \omega_0)/\omega_{\text{inj}}$ in (8) changes from 1.5 to 3. It is therefore plausible that the substitution $(\omega_{\text{inj}} + \omega_0)/\omega_{\text{inj}} \approx 2$ maintains a reasonable accuracy in our derivations. We then have

$$\frac{2I_{\text{SS}}}{\pi V_0} + \frac{I_{\text{inj}}}{V_0}\cos\phi = \frac{1}{R_p} \tag{10}$$

$$\frac{I_{\text{inj}}}{V_0}\sin\phi = -2\Delta\omega C_1. \tag{11}$$

Eliminating V_0 and replacing C_1 with $Q/(R_p\omega_0)$, where Q denotes the tank quality factor, we obtain

$$|\Delta\omega| = \big|\omega_{\text{inj}} - \omega_0\big| = \frac{\omega_0}{2Q}\frac{I_{\text{inj}}\sin\phi}{2I_{\text{SS}}/\pi + I_{\text{inj}}\cos\phi}. \tag{12}$$

For a given I_{inj}, as ω_{inj} varies, so does ϕ. The maximum value of $\Delta\omega$ corresponds to the one-sided input lock range and is computed by differentiating (12) with respect to ϕ. It follows that:

$$|\Delta\omega|_{\max} = \frac{\omega_0}{2Q}\frac{1}{\sqrt{\left(\dfrac{2I_{\text{SS}}}{\pi I_{\text{inj}}}\right)^2 - 1}} \tag{13}$$

which occurs when $\phi = \cos^{-1}[-\pi I_{\text{inj}}/(2I_{\text{SS}})]$. This result agrees with those in [15], [16], [17], [21], and [23], indicating that at the edge of the lock range, $\phi \approx 90°$ if $\pi I_{\text{inj}} \ll 2I_{\text{SS}}$. Of course, our proposed equations (7) and (8) are more general and applicable even if I_{inj} is comparable to I_{SS}.

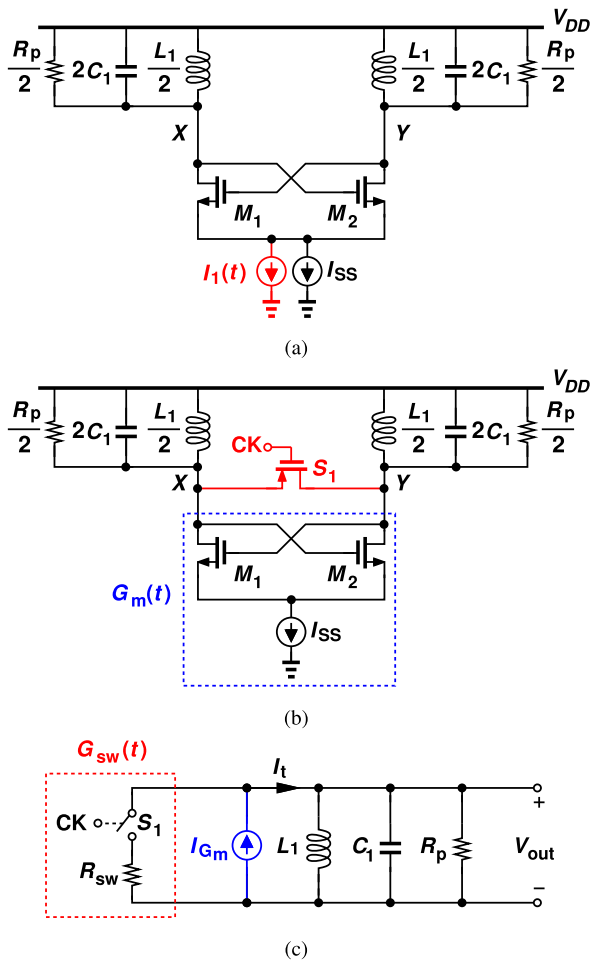


Fig. 2. (a) Indirect ILFD, (b) direct ILFD, and (c) time-variant equivalent model of the latter.

III. Injection Locking in ILFDs

The behavior of ILFDs has been analyzed extensively [17], [18], [19], [20], providing fairly accurate results for the topology shown in Fig. 2(a). We shall call this arrangement an "indirect" ILFD in this article. For the "direct" ILFD shown in Fig. 2(b) [28], on the other hand, the prior analyses are not accurate, as will be quantified in the following. Our work offers two key results: 1) a time-variant model that predicts the direct ILFD's behavior with reasonable accuracy and 2) insights that allow us to widen the circuit's lock range considerably.

A. Divider Analysis

In a manner similar to the oscillator analysis in Section II, we represent the locked divider by a time-variant circuit in which the negative transconductance varies periodically. In this case, the differential output voltage of Fig. 2(b) is written as $V_0\cos[(\omega_{inj}/2)t+\phi]$. Moreover, we also model the injection mechanism by a time-variant structure, namely, a switch [Fig. 2(c)]. The conductance of the switching branch, G_{sw}, toggles between zero and $G_{sw0}=1/R_{sw}$ at a rate of ω_{inj} if S_1 turns on and off abruptly. As explained in Section III-B, simulations with sinusoidal inputs confirm that

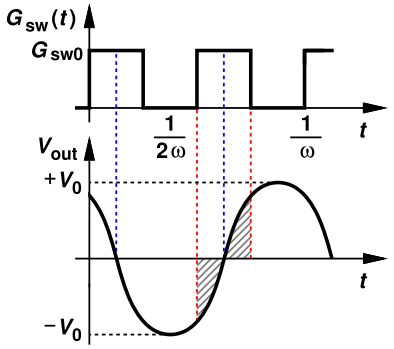


Fig. 3. Direct ILFD input and output waveforms in the middle of the lock range ($\Delta\omega=0$).

this approximation is reasonable. We then have

$$G_{sw}(t)=G_{sw0}\left[0.5+\frac{2}{\pi}\sum_{n=0}^{\infty}\frac{(-1)^n\sin[(2n+1)\omega_{inj}t]}{2n+1}\right]. \tag{14}$$

To write a Kirchhoff's current law (KCL) for the five branches, we first note that the switch current can be expressed as $I_1(t)=-G_{sw}(t)V_{out}=-G_{sw}(t)V_0\cos[(\omega_{inj}/2)t+\phi]$. Maintaining only the first two terms of (14), we have

$$I_1(t)=-G_{sw0}\left[0.5+\frac{2}{\pi}\sin(\omega_{inj}t)\right]V_0\cos\left[(\omega_{inj}t)/2+\phi\right]. \tag{15}$$

If only the fundamental component at $\omega_{inj}/2$ is retained

$$I_1(t)\approx -G_{sw0}\left[0.5-\frac{1}{\pi}\sin 2\phi\right]V_0\cos\left[(\omega_{inj}t)/2+\phi\right] - G_{sw0}\frac{1}{\pi}\cos 2\phi\ V_0\sin\left[(\omega_{inj}t)/2+\phi\right]. \tag{16}$$

We then write $I_1(t)+I_{G_m}(t)=I_t(t)$, expand the terms, and evaluate the two sides at $t=(2\pi-\phi)/(\omega_{inj}/2)$ and $t=(\pi/2-\phi)/(\omega_{inj}/2)$. It follows that:

$$G_{m0}-G_{m2}-G_{sw0}\left[0.5-\frac{1}{\pi}\sin(2\phi)\right]=\frac{1}{R_p} \tag{17}$$

$$G_{sw0}\frac{1}{\pi}\cos(2\phi)=2\Delta\omega C_1 \tag{18}$$

where $(\omega_{inj}/2+\omega_0)/(\omega_{inj}/2)$ is approximated by 2 and $\Delta\omega=\omega_{inj}/2-\omega_0$. These equations play a central role in our analysis and design of the direct ILFD.

Two points of contrast can be drawn between direct injection-locked oscillators and dividers. First, in the middle of the lock range, i.e., for $\Delta\omega=0$, (18) suggests $\phi=45°$ rather than $\phi=0°$. As shown in Fig. 3, this point means that each output zero crossing occurs halfway between two consecutive input zero crossings. We can intuitively explain this result by noting that the net charge flowing through S_1 in *half* of the input period must be zero (as indicated by the shaded parts of V_{out}), as if the switch were absent and the oscillator operated without injection. Second, at the edge of the lock range, the oscillator model with weak injection implies that $\phi\approx 90°$, whereas (17) and (18) do not suggest so. In fact, at the edge,

the value of ϕ strongly depends on G_{sw0}. This property proves useful in our optimization of the divider (Section III-B).

B. Divider Optimization

Equations (17) and (18) reveal the dependence of the lock range upon the average switch resistance, G_{sw0}. As such, they can be exploited to maximize the lock range. To this end, we eliminate ϕ from the two equations, obtaining

$$\Delta\omega = \pm\frac{G_{sw0}}{2\pi C_1}\sqrt{1-\frac{\pi^2}{G_{sw0}^2}\left(G_{m0}-G_{m2}-\frac{1}{R_p}-0.5G_{sw0}\right)^2}. \tag{19}$$

Differentiating this result with respect to G_{sw0} yields

$$G_{sw0,opt} = \frac{2\pi^2}{\pi^2-4}\left(G_{m0}-G_{m2}-\frac{1}{R_p}\right) \tag{20}$$

$$|\Delta\omega_{max}| = \frac{\omega_0}{Q\sqrt{\pi^2-4}}\left[(G_{m0}-G_{m2})R_p-1\right] \tag{21}$$

where $Q = R_pC_1\omega_0$. Note that the two-sided input-referred lock range is $4\Delta\omega_{max}$. To our knowledge, this is the first analysis prescribing an optimum condition for the injector transistor, a key benefit of the proposed time-variant model.

Let us simplify (20) and (21) to obtain some rules of thumb. Since the output amplitude reaches a minimum at the edge of the lock range, we can assume that the differential negative resistance, $-1/(G_{m0}-G_{m2})$, is approximately equal to its small-signal counterpart, $-2/g_m$. Also, $g_mR_p/2 \gg 1$, and hence,

$$G_{sw0,opt} = \frac{\pi^2}{\pi^2-4}g_m \approx 1.7g_m. \tag{22}$$

Our first optimization rule of thumb then emerges as

$$R_{sw} \approx \frac{1}{1.7g_m}. \tag{23}$$

Moreover, the total input-referred lock range is

$$\begin{aligned} 4\Delta\omega_{max} &\approx \frac{2\omega_0}{\sqrt{\pi^2-4}}\frac{g_mR_p}{Q} \\ &\approx \frac{0.83g_mR_p}{Q}\omega_0. \end{aligned} \tag{24}$$

Noting that $R_p = QL_1\omega_0$ and $\omega_0^2 = 1/(L_1C_1)$, we write our second rule of thumb as

$$4\Delta\omega_{max} \approx 0.83\frac{g_m}{C_1}. \tag{25}$$

The foregoing derivations have assumed abrupt clock transitions. For sinusoidal inputs, we can approximate the switch conductance by a half-sine waveform (Fig. 4), where the gate of the switch is biased one threshold voltage away from the source and drain common-mode level, the input amplitude is V_{inj}, and the peak switch conductance in Fig. 4 is given by $G_{sw,max} = \mu_nC_{ox}(W/L)_{sw}V_{inj}$. We then approximate this behavior by a square-wave toggling between zero and $(2/\pi)G_{sw,max}$. The right-hand side of (23) is thus multiplied by $2/\pi$, while (25) remains the same. We observe intuitively that a greater bias overdrive for the switch raises G_{sw0}, and a large input swing leads to a higher value for $G_{sw,max}$, which also increases the equivalent $G_{sw0} = (2/\pi)G_{sw,max}$. Hence, the switch width must be so selected as to satisfy the condition defined by (23). The maximum lock range prescribed by (25) remains unchanged.

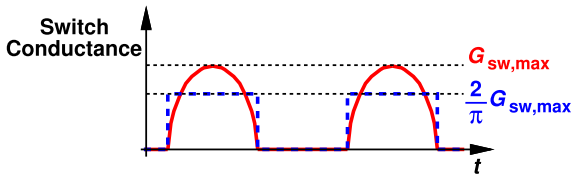


Fig. 4. Switch conductance waveform and its square-wave approximation.

We should note that our analysis assumes that the injector switch operates in the triode region. This is justified by recognizing that, at the edge of the lock range, the divider voltage swings are well below the amplitude applied to the switch's gate, while the dc level at this gate is chosen only one threshold away from its source and drain dc levels. Since the switch is biased at the edge of turn on, it is guaranteed to enter the triode region as soon as the gate departs from the dc level by about 75 mV. This point stands in contrast to the analysis in [24] where a square-wave output is assumed with voltage swings *greater* than the input amplitude, and hence, the injector resides in saturation.

If small input swings and large dc overdrives are chosen, the switch conductance does not fall to zero, thus presenting a resistance between the divider output nodes [13]. In such a case, we replace $1/R_p$ in (20) and (21) with $1/R_p + G_{sw,min}$, where $G_{sw,min}$ denotes the minimum switch conductance. We observe that this additional term reduces both the optimal G_{sw0} and the maximum lock range, an undesirable effect.

These insights are verified by circuit simulations in 28-nm CMOS technology. We target a center output frequency, ω_0, equal to 2π(24 GHz) and select the devices in Fig. 2(b) as follows: $L = 30$ nm, $W_1 = W_2 = 3.2$ μm, $L_1 = 2.4$ nH, $C_1 = 17$ fF, $I_{SS} = 1.8$ mA, and $R_p = 1.8$ kΩ. The tank Q would be around 10, but, due to the transistors' output resistance, it drops to 5 for small output swings ($\sim$150 mV_{pp}, single-ended). The effective transconductance, $G_{m0}-G_{m2} = 2.32$ mS, is close to $g_m/2 = 2.38$ mS. Equation (20) suggests that $G_{sw0,opt} = 6$ mS, which corresponds to a switch width of 5 μm. Now, we vary this width and measure the simulated lock range, observing the behavior shown in Fig. 5. The optimum G_{sw0} is around 7.2 mS, but the peak is broad. Moreover, the maximum lock range obtained in these simulations ($\approx$34 GHz) agrees well with that predicted by (25) ($\approx$35 GHz). Also plotted is the behavior as predicted by our model, except that *finite* rise and fall times are considered for the switch conductance. We elaborate on this model refinement in Appendix C. Some discrepancy is expected here as the analysis assumes a sinusoidal output voltage, whereas, near the edge of the lock range, the third harmonic becomes significant.

We should point out that the total tank capacitance varies from 15 fF for $W_{sw} = 0.5$ μm to 21 fF for $W_{sw} = 10$ μm, reducing the lock range by a small amount and causing discrepancy.

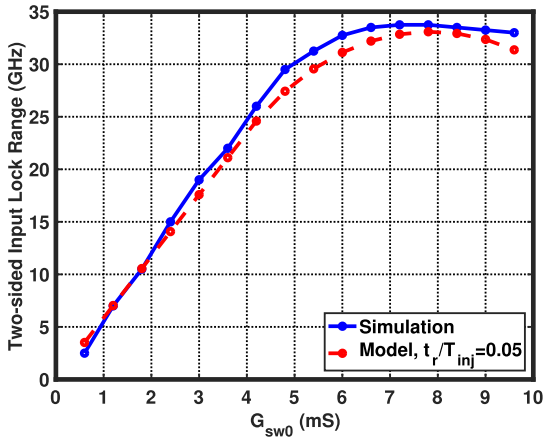


Fig. 5. Calculated and simulated two-sided input lock range versus switch conductance (G_{sw0}).

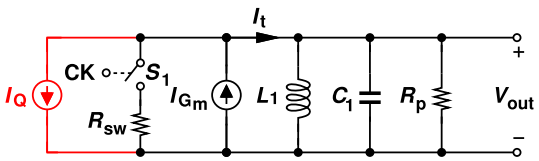


Fig. 6. Time-variant model for quadrature current injection to a DILFD.

It is worth noting that (24) predicts a wider lock range than that achievable by the Miller divider, namely [29]

$$4\Delta\omega_{\max} = \frac{2g_m R_p}{\pi Q}\omega_0. \tag{26}$$

The two differ by a factor of 1.3.

IV. Quadrature Coupling

In this section, we exploit our previous results to determine how adding quadrature injection to the direct ILFD alters its lock range. By this type of injection, we mean a current at the output frequency and 90° out of phase with respect to the output voltage. Let us assume that, in Fig. 2(b), such a current is applied to the output port. From the equivalent time-variant model shown in Fig. 6, where $I_Q = I_{\text{inj}} \sin[(\omega_{\text{inj}}/2)t + \phi]$, we recognize that only (18) changes

$$G_{m0} - G_{m2} - G_{\text{sw0}}\left[0.5 - \frac{1}{\pi}\sin(2\phi)\right] = \frac{1}{R_p} \tag{27}$$

$$G_{\text{sw0}}\frac{1}{\pi}\cos(2\phi) + \frac{I_{\text{inj}}}{V_0} = 2\Delta\omega C_1. \tag{28}$$

Notably, this reveals that $\Delta\omega$ can be *shifted* up or down by the term I_{inj}/V_0. In fact, it is possible to shift $\Delta\omega$ completely above or below the resonance frequency.

Let us investigate this point further. We begin by selecting the switch *width* according to (20) and obtaining an output lock range from $\omega_0 - \Delta\omega_{\max}$ to $\omega_0 + \Delta\omega_{\max}$. Since $\Delta\omega$ in (18) must satisfy the extreme values prescribed by (21), ϕ varies across this range so as to keep $(1/\pi)G_{\text{sw0}}\cos(2\phi)$ in (18) between two limits

$$-\frac{2}{\sqrt{\pi^2-4}}\left[(G_{m0} - G_{m2}) - 1/R_p\right]$$

$$\le \frac{1}{\pi}G_{\text{sw0}}\cos(2\phi)$$

$$\le \frac{2}{\sqrt{\pi^2-4}}\left[(G_{m0} - G_{m2}) - 1/R_p\right]. \tag{29}$$

Next, we wish to shift the lock range, $\Delta\omega = \omega_{\text{inj}}/2 - \omega_0$, completely above ω_0, i.e., $\Delta\omega$ in (28) must be positive, that is, we must ensure that I_{inj}/V_0 is greater than $-(1/\pi)G_{\text{sw0}}\cos(2\phi)$, which has a maximum given by (29). It follows that:

$$\left(\frac{I_{\text{inj}}}{V_0}\right)_{\text{opt}} = \frac{2}{\sqrt{\pi^2-4}}\left[(G_{m0} - G_{m2}) - 1/R_p\right]. \tag{30}$$

This condition guarantees that the output lock range extends from ω_0 to $\omega_0 + [2\omega_0/(Q\sqrt{\pi^2-4})][(G_{m0} - G_{m2})R_p - 1]$. Similarly, inverting the injection polarity shifts $\Delta\omega$ completely below ω_0. In summary, the optimum quadrature injection is expressed as

$$\left(\frac{I_{\text{inj}}}{V_0}\right)_{\text{opt}} = \pm\frac{2}{\sqrt{\pi^2-4}}\left[(G_{m0} - G_{m2}) - 1/R_p\right] \tag{31}$$

that is, the lock range can be doubled if quadrature current-mode injection augments the passive-switch-based mechanism.

In order to provide a current that bears a 90° phase with respect to V_{out}, we turn to a quadrature topology. Fig. 7(a) shows such an arrangement in a simplified form, where Z_T denotes the RLC tank and G_{mc} denotes the coupling coefficient. The circuit can be viewed as two direct ILFDs that are coupled to each other or a quadrature oscillator that receives direct differential injection through two switches. Both perspectives prove useful in answering the following question: how are the + and − signs in (31) satisfied as the input frequency varies from below $2\omega_0$ to above it? We know that the quadrature oscillator can operate at either $\omega > \omega_0$ or $\omega < \omega_0$ [30], but with different phase orders [Fig. 7(b)]. Thus, as the input frequency goes from less than $2\omega_0$ to greater than $2\omega_0$, V_Q automatically rotates by 180°, thereby providing the sign reversal required by (31). Fig. 7(c) summarizes the resulting shifts. In the optimum case given by (31), this figure suggests an output-referred lock range from $\omega_0 - 2\Delta\omega_{\max}$ to $\omega_0 + 2\Delta\omega_{\max}$. The input-referred range is twice as wide. It is interesting to note that a sufficiently strong coupling factor in fact leads to a dead zone in the middle of the lock range.

The dead zone can be explained intuitively as well. In the absence of an external injection, the coupled oscillators shift to a frequency equal to $\omega_0 \pm I_{\text{inj}}/(2C_1V_0)$, where I_{inj} denotes the amplitude of the current injected by one core into the other. Viewing the overall circuit as a free-running oscillating system, we recognize that locking it to an input frequency equal to $2\omega_0$ becomes more difficult as I_{inj} increases. If I_{inj} is sufficiently large, the divider's "natural" frequency is excessively far from ω_0, prohibiting lock. We remark that the lock range can be widened by replacing the LC tank with a higher order resonator, i.e., by making the tank's phase response flatter [6], [8].

We repeat the simulations of Section III-B for the quadrature topology, but now varying the coupling transconductance, G_{mc}, while the width of the injector switches has the optimum

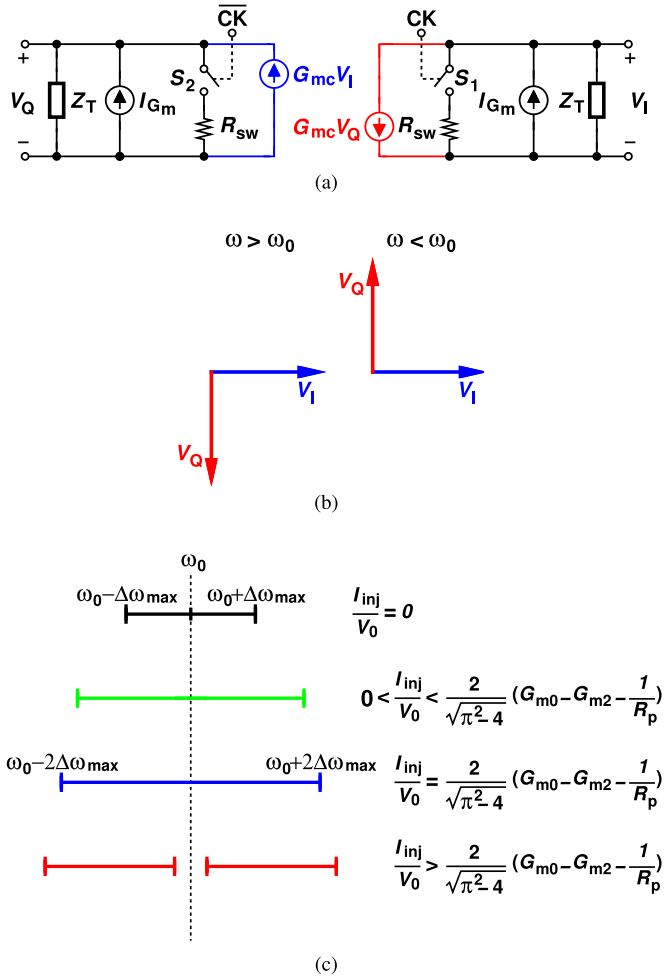


Fig. 7. (a) time-variant model of a quadrature DILFD, (b) output phasors above ω_0 and below ω_0, and (c) output-referred lock range shift with different quadrature coupling strengths.

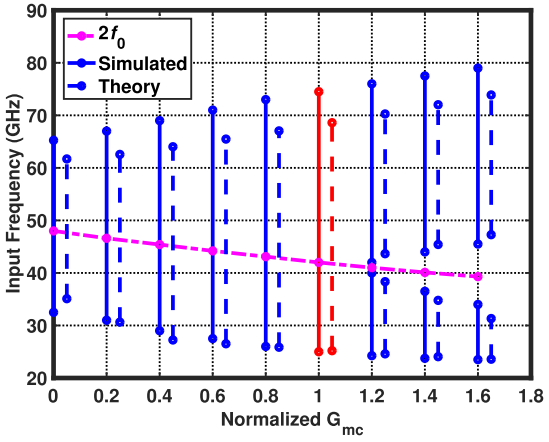


Fig. 8. Two-sided input lock range versus normalized coupling transconductance (normalized G_{mc}).

value (5 μm) found earlier. Fig. 8 plots the two-sided input lock ranges with the red plot indicating the lock range for the optimum value of G_{mc} suggested by (31), i.e., 1.45 mS.

Three aspects of the characteristics in Fig. 8 merit discussion. First, as the coupling transistors are made wider to

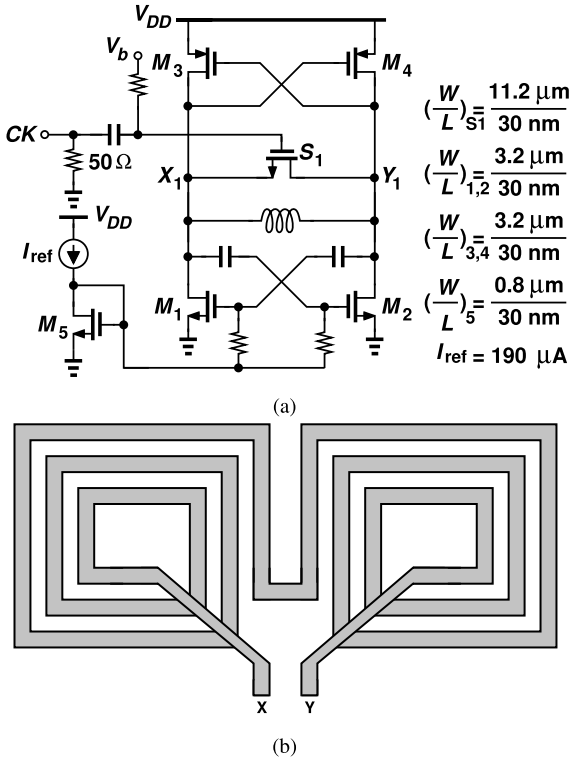


Fig. 9. (a) Implemented single-core DILFD and (b) layout of differential inductor.

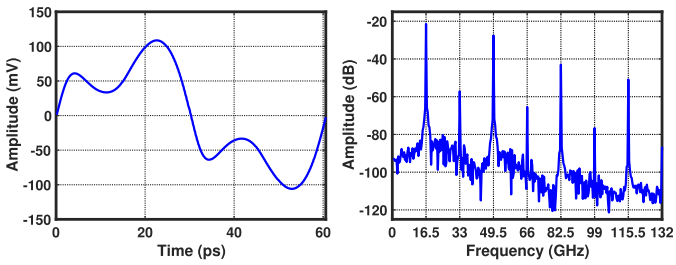


Fig. 10. Output waveform at the lower edge of the lock range (input frequency = 33 GHz) along with its spectrum.

increase the normalized G_{mc} from 0 to 1.6, $2\omega_0$ drops from 2π (48 GHz) to 2π (39.3 GHz), an effect not included in our derivations. Thus, the progression in Fig. 7(c) is affected by this decrease of ω_0; in essence, the circuit "resists" the shift of $\Delta\omega$ to higher values. We then observe that the lock range extends more above $2\omega_0$ than below. This is due to the $(\omega_{inj}/2 + \omega_0)/(\omega_{inj}/2)$ factor that we approximated by 2 in (28). In reality, this factor is less for $\omega > \omega_0$ than for $\omega < \omega_0$. Consequently, $\Delta\omega$ in (28) must change in reverse proportion.

Second, the lower end of the input lock range in Fig. 8 does not go below approximately $0.6 \times (2\omega_0)$. For example, at a normalized G_{mc} of 1.0, we have $\omega_{in,min} = 2\pi(25\ \text{GHz})$. The theoretical bound, on the other hand, is, from Fig. 7(c), equal to $2\omega_0 - 4\Delta\omega_{max} = 2\pi$ (42–33 GHz) $= 2\pi$ (9 GHz). This is because the sinusoidal output voltage waveform assumption made above does not hold if the circuit operates at lower frequencies, at which the third harmonic of the output current sees a greater tank impedance. In fact, at $\omega = \omega_0/\sqrt{3} \approx 0.58\omega_0$, the tank impedances at the first and third harmonics

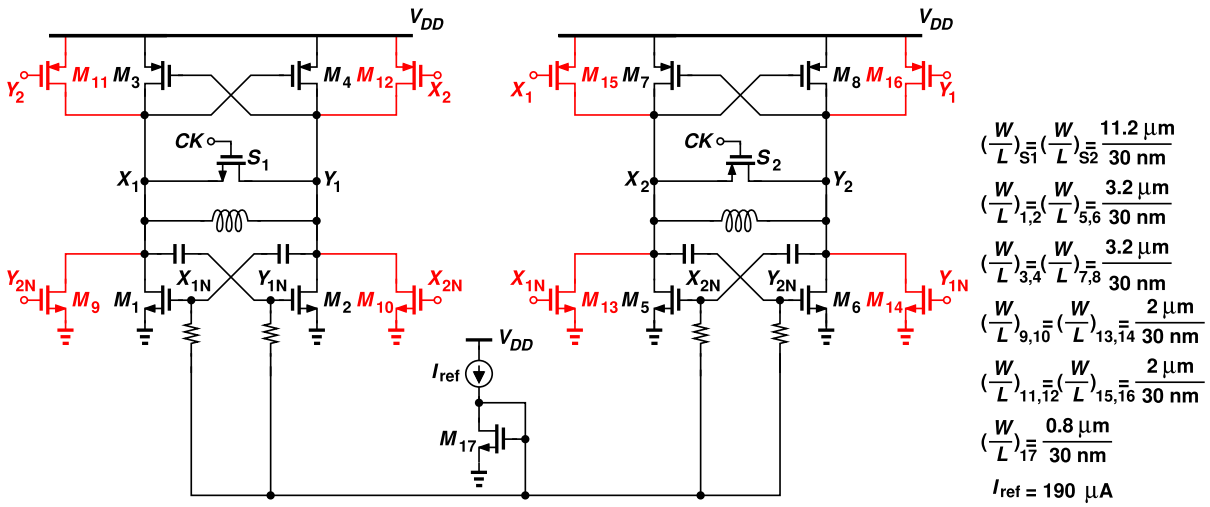


Fig. 11. Implemented quadrature DILFD.

are equal. If not attenuated sufficiently, the latter creates additional zero crossings in the output waveform, causing lock failure. This phenomenon is similar to that observed in the Miller divider [29].

Third, even though a greater coupling factor requires wider transistors and introduces a larger capacitance at the output nodes, Fig. 8 reveals that it still widens the lock range.

Finally, we have added the lock ranges predicted by the theory based on (21) and (28) for the same G_{mc} values next to the simulated plots. In these plots, we have assumed that the minimum locking frequency is $0.6 \times (2\omega_0)$, as discussed above. The predicted lock range is slightly narrower due to the limited accuracy of the assumption $(\omega_{inj} + \omega_0)/\omega_{inj} \approx 2$, made in (21) and (28).

V. Circuit Implementation

The developments in Sections II–IV lead to two realizations for direct ILFDs: a single-core differential topology or a quadrature configuration. The former provides a narrower lock range but employs one inductor, whereas the latter requires two and also consumes a higher power. Both have been investigated here.

The single-core ILFD is shown in Fig. 9(a). The use of both NMOS and PMOS cross-coupled pairs raises the transconductance and establishes a common-mode level suited to the injector switch. The input clock is terminated with an on-chip 50-Ω resistor and applied to the gate of the injector switch through an ac coupling capacitor. The gate of the injector switch is biased at the edge of turn on in order to provide the half-sine conductance behavior described in Section III. Moreover, capacitive coupling to the gates of M_1 and M_2 along with a current mirror defines the bias properly, making it much less sensitive to process, temperature, and supply variations. To our knowledge, this biasing technique has not been used in prior oscillators or dividers.

Inductor L_1 in Fig. 9(a) can be naturally realized by a standard symmetric geometry, but at the cost of substantial capacitance as the interwinding components experience a large voltage difference [31]. We instead opt for the structure shown in Fig. 9(b), reducing the equivalent capacitance by 42%. This modification drops the Q at 25 GHz from 14.9 to 11.5.

The simulation of the single-core ILFD with layout parasitics yields the waveform and spectrum shown in Fig. 10 at the lower edge of the lock range. The inductors are modeled by Ansoft's HFSS. As mentioned in Section III, the direct ILFD output departs considerably from a sinusoid near the edge of the lock range when the design targets a wide $\Delta\omega$. We note that the third harmonic is only 6 dB below the fundamental here.

One phenomenon that merits special consideration is the fall of the output swing as the output frequency departs from ω_0. It can be explained with the aid of (17) and (18). In fact, omitting ϕ from the two yields

$$\left[\frac{1}{R_p} + \frac{G_{sw0}}{2} - (G_{m0} - G_{m2})\right]^2 + 4\Delta\omega^2 C_1^2 = \frac{G_{sw0}^2}{\pi^2} \qquad (32)$$

revealing that, as $\Delta\omega^2$ increases, $G_{m0} - G_{m2}$ must climb (for a constant G_{sw0}). This is possible only if the cross-coupled pairs experience less compression, i.e., if the voltage swings become smaller. The outputs can be amplified by self-biased inverters.

The quadrature ILFD circuit is shown in Fig. 11. Two test and measurement issues govern the design. First, since it is difficult to carry a differential clock onto the chip at high frequencies, the core on the right employs a PMOS switch so that a single clock phase can drive S_1 and S_2. Second, in view of the low power levels available from millimeter-wave generators (≈0 dBm), the input is capacitively coupled to the gates of the switches and rides on a dc level of 0.75 V on the NMOS gate and 0.1 V on the PMOS gate.

For testing and characterization, the ILFDs are followed by open-drain PMOS common-source stages that directly drive off-chip instrumentation. For each PMOS device, we have $W/L = 4\ \mu m/30$ nm, approximating a typical load that the dividers would face in a transceiver environment.

VI. Experimental Results

The two divider prototypes have been fabricated in TSMC's 28-nm CMOS technology. Fig. 12 shows the die photograph

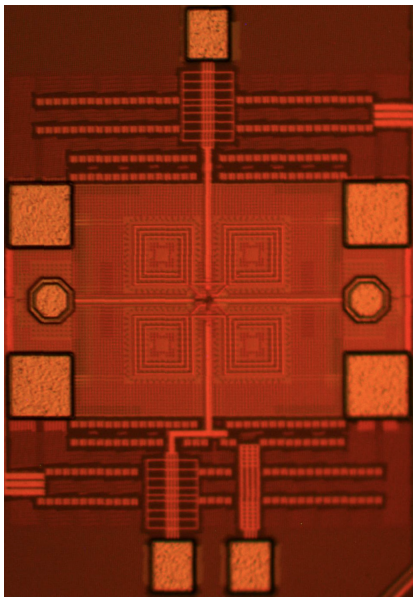


Fig. 12. Die photograph of the quadrature DILFD.

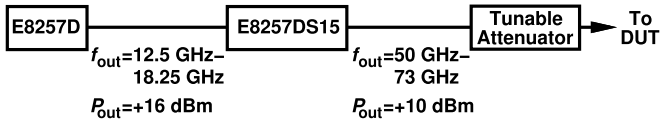


Fig. 13. Input signal generation setup for frequencies higher than 50 GHz.

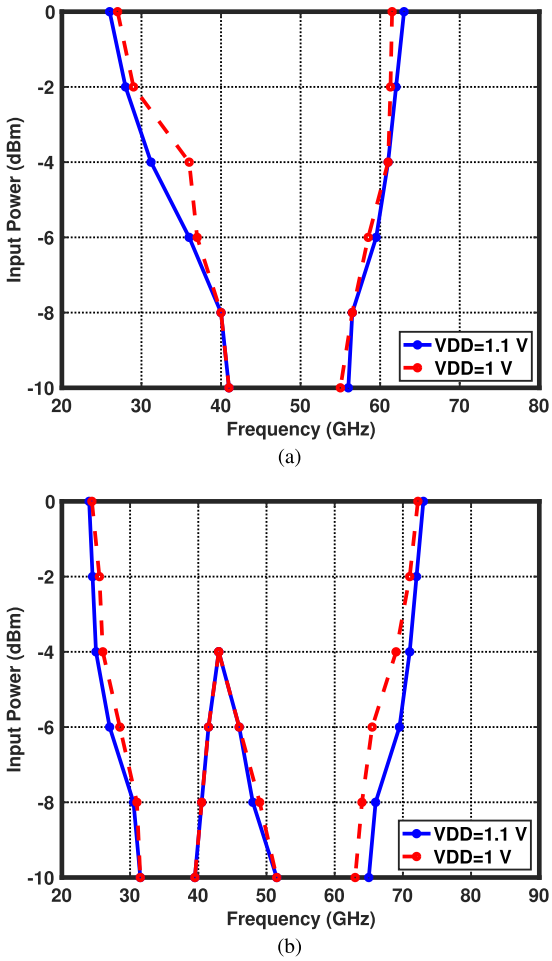


Fig. 14. Measured input sensitivity of (a) single-core DILFD and (b) quadrature DILFD.

of the quadrature ILFD. The single-core counterpart is created by simply copying this layout and removing one core and its inductor. The circuits have been tested on a high-speed probe station.

In order to measure the dividers' lock range, HP 83650B generates inputs up to 50 GHz. For higher frequencies, the setup shown in Fig. 13 is used. Keysights' E8257D generates an output in the range of 12.5–18.25 GHz, which is then quadrupled by E8257DS15.

The prototypes have been characterized with both 1- and 1.1-V supplies with a maximum input power of 0 dBm and no tuning. Even with a 1.1-V supply, none of the transistors experiences V_{GS}, V_{DS}, or V_{GD} greater than 855 mV, avoiding stress as the default supply voltage for this technology is 1 V. Fig. 14 plots their input sensitivity as a function of the input frequency. The single-core ILFD operates from 26 to 63 GHz and the quadrature counterpart operates from 24 to 73 GHz. The power consumptions are 1.88 and 4.76 mW (excluding that of the output buffers). For parts of the input range, e.g., between 42 and 56 GHz in Fig. 14(a), the necessary input power is below −10 dBm. Input power levels below −10 dBm are not investigated in view of practicality. The rise in the required input power between 40 and 52 GHz in Fig. 14(b) is to be expected. We show that, in a quadrature ILFD, the sensitivity is best at *two* input frequencies above and below $2\omega_0$, thus degrading between the two. We first rewrite (28) as

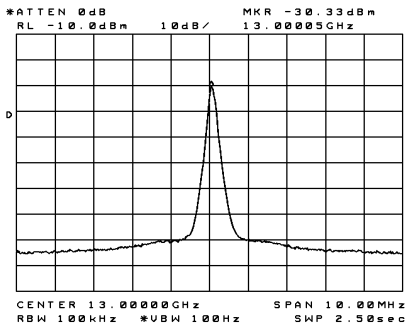
$$G_{sw0}\frac{1}{\pi}\cos(2\phi) = 2\Delta\omega C_1 - \frac{I_{inj}}{V_0} \tag{33}$$

and seek the "best" case as when G_{sw0} can be at its lowest. Bearing in mind that I_{inj}/V_0 can be either positive or negative in a quadrature design (Section IV), we recognize that the right-hand side of (33) approaches zero at $\Delta\omega \approx (+I_{inj}/V_0)/(2C_1)$ and $\Delta\omega \approx (-I_{inj}/V_0)/(2C_1)$. These two offsets are located on the two sides of $2\omega_0$ and enable operation with a minimal G_{sw0}. In between, a higher G_{sw0} and, hence, a higher input power is necessary.

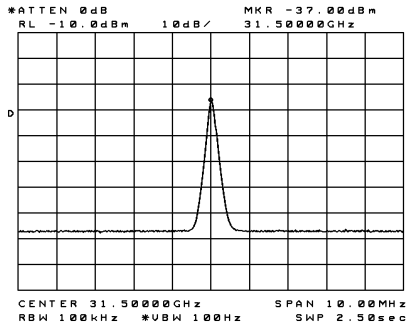
Fig. 15 shows the measured output spectra of the dividers at the lower and upper edges of their lock range, demonstrating proper operation.

Fig. 16 plots the measured phase noise profiles at the 60-GHz input frequency for offset frequencies from 100 Hz to 10 MHz. It can be seen that the output phase noise is limited by that of the signal generator. According to simulations, the intrinsic phase noise of the ILFDs is about −131.5 to −146.5 dBc/Hz at 10 MHz depending on the input frequency (lower in the middle of the lock range and higher at the edges). The HP 83650B signal generator exhibits substantial phase noise fluctuations at low offset frequencies. Since we are unable to monitor the dividers' input and output phase noise profiles simultaneously, the difference between the two departs from the nominal value of 6 dB at some offsets.

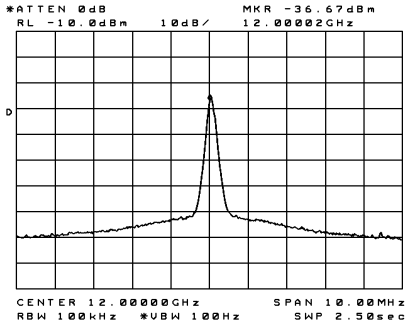
Table I summarizes the measured performance of the proposed dividers and compares it to that of the prior art. Both exhibit wide lock ranges, namely, 83% and 101%. Moreover,



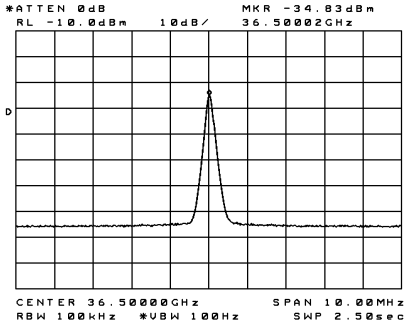
(a)



(b)



(c)



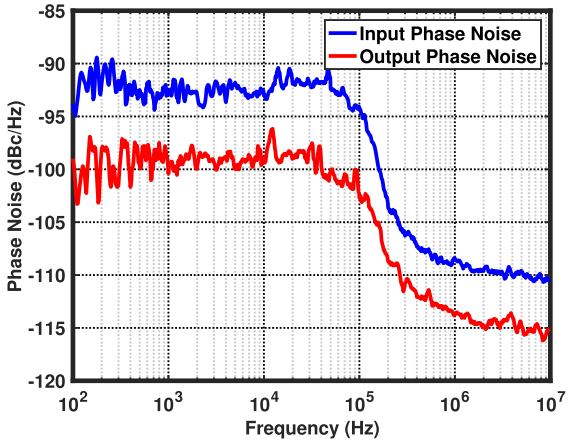
(d)

Fig. 15. Output spectrum of (a) single-core DILFD at the lower edge of the lock range, (b) single-core DILFD at the upper edge of the lock range, (c) quadrature DILFD at the lower edge of the lock range, and (d) quadrature DILFD at the upper edge of the lock range.

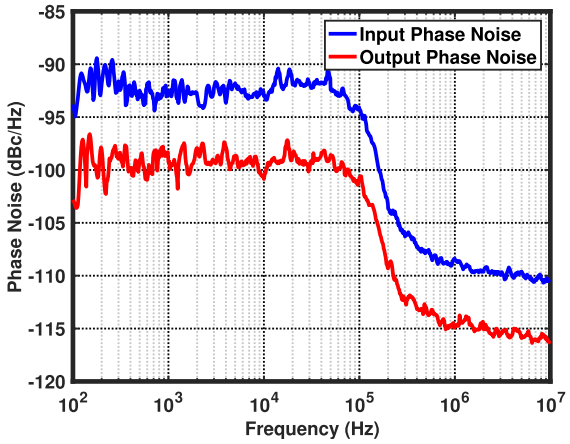
the single-core circuit provides a 9-dB advantage in the figure of merit (FOM).

VII. Conclusion

This article introduces a general time-variant model for injection locking in oscillators and frequency dividers that yields new insights and optimization criteria. The model is applied to both single-core and quadrature topologies, offering methods of maximizing the lock range without sacrificing the quality factor. The proposed concepts lead to wide lock ranges and highest FOM reported to date.



(a)



(b)

Fig. 16. Phase noise profile at 60-GHz input frequency for (a) single-core DILFD and (b) quadrature DILFD.

Appendix A

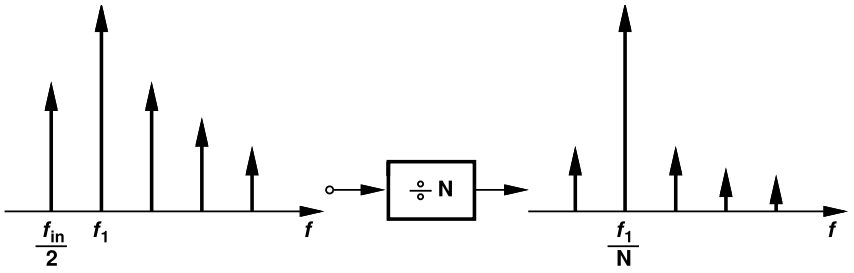
An oscillator or divider under injection at a frequency of f_{in} but operating outside its lock range produces a spectrum of discrete frequencies the strongest of which is not harmonically related to the input [15], [17] [Fig. 17(a)]. Upon traveling through a $\div N$ circuit, the weaker spurs are suppressed by a factor of N. The ILFD and $\div N$ stages thus behave as if they received an input frequency equal to $2f_1$ even though the actual value is f_{in}. This can cause a false lock in a PLL.

We study the locking behavior of a PLL exploiting a direct ILFD with a narrow lock range. As shown in Fig. 17(b), the PLL comprises a behavioral voltage-controlled oscillator (VCO), an injection-locked divide-by-2 stage, a latch-based divide-by-16 stage, and a sampling phase detector. The ILFD has an input lock range of 52–54.5 GHz. In this experiment, the reference frequency is swept to obtain the desired VCO output frequency. As shown in Fig. 17(c), when the target VCO frequency is 52.8 GHz ($f_{ref} = 1.65$ GHz), the PLL

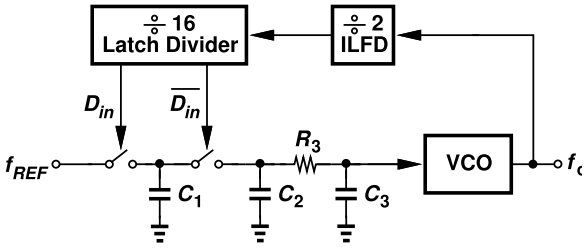
TABLE I
DIVIDERS' PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ART

	[5][1]	[6][1]	[7][1]	[8][1]	This Work[1]	
					Single DILFD	Quadrature DILFD
Frequency [GHz]	12-32	27.9-53.5	25-53.6	28.8-91.9	26-63	24-73
Lock Range [%] [2]	90.9	62.9	72.7	104.5	83.1	101
P_{DC} [mW]	2.4	5.8	6.7	5.8	1.88	4.76
FOM [GHz/mW] [3]	8.33	4.41	4.26	10.9	19.68	10.29
Active Area [mm^2]	0.45	0.18	N/A	0.02	0.019	0.037
CMOS Technology	90 nm	65 nm	65 nm	40 nm	28 nm	28 nm

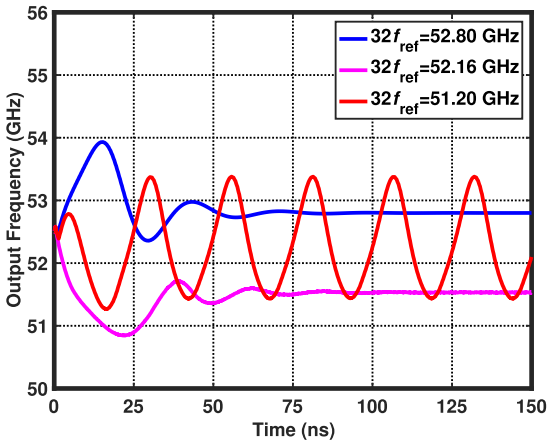
[1]All measurements with a maximum input power = 0 dBm [2]Lock Range=$2(f_{max}-f_{min})/(f_{max}+f_{min})$
[3]FOM=$(f_{max}-f_{min})/P_{DC}$



(a)



(b)



(c)

Fig. 17. (a) Output spectrum of an injection-pulled frequency divider before and after a $\div N$ stage, (b) PLL with a direct ILFD divider, and (c) its lock behavior.

properly locks. If the target frequency is 51.2 GHz ($f_{\text{ref}} = 1.6$ GHz), the PLL fails to lock, as expected. However, when the target frequency is 52.16 GHz ($f_{\text{ref}} = 1.63$ GHz), the VCO frequency reaches 51.53 GHz, representing a false lock condition. In fact, under this condition, $f_{\text{in}}/2$ in Fig. 17(a) is equal to 51.53 GHz/2, but $f_1 = 52.16$ GHz/2. After passing through the $\div 16$ circuit, only $f_1/16 = 1.63$ GHz survives and drives the phase detector.

APPENDIX B

In this appendix, we use the law of conservation of energy to obtain the first key equation governing injection locking. In the time-variant model of Fig. 1(b), the power injected into the tank by I_{inj} and I_{G_m} must be equal to that consumed by the tank. The first two power quantities are expressed as

$$P_{\text{inj}} = \frac{1}{T}\int_{-T/2}^{+T/2} I_{\text{inj}} V_0 \cos(\omega t + \phi)\cos(\omega t)dt = \frac{V_0 I_{\text{inj}}\cos(\phi)}{2} \tag{34}$$

and

$$P_{G_m} = \frac{1}{T}\int_{-T/2}^{+T/2} (G_{m0} - G_{m2}) V_0^2 \cos^2(\omega t + \phi)dt = \frac{(G_{m0} - G_{m2})V_0^2}{2}. \tag{35}$$

Equating $P_{\text{inj}} + P_{G_m}$ to $V_0^2/(2R_p)$ yields

$$G_{m0} - G_{m2} + \frac{I_{\text{inj}}}{V_0}\cos(\phi) = \frac{1}{R_p}. \tag{36}$$

APPENDIX C

In this appendix, we study a more general form of injection in direct ILFDs and compare the analytical and simulation results. Let us assume that the switch conductance toggles between zero and its maximum with finite rise and fall times, t_r, as shown in Fig. 18, rather than with abrupt transitions. From Section III, we know that only the dc and the first harmonic of the conductance play the main role in our derivations. It can be shown that the sum of these two is given by $G_{\text{sw0}}[0.5 \times (1 - 2t_r/T_{\text{inj}}) + (2/\pi)\text{sinc}(2t_r/T_{\text{inj}})\sin(\omega_{\text{inj}}t)]$, where $\text{sinc}(2t_r/T_{\text{inj}}) = \sin[\pi(2t_r/T_{\text{inj}})]/[\pi(2t_r/T_{\text{inj}})]$.

We rewrite the KCL equations of Section III and revise (17) and (18) to, respectively

$$G_{m0} - G_{m2} - G_{\text{sw0}}\left[0.5 \times \left(1 - \frac{2t_r}{T_{\text{inj}}}\right) - \frac{1}{\pi}\text{sinc}\left(\frac{2t_r}{T_{\text{inj}}}\right)\sin(2\phi)\right] = \frac{1}{R_p} \tag{37}$$

$$G_{\text{sw0}}\frac{1}{\pi}\text{sinc}\left(\frac{2t_r}{T_{\text{inj}}}\right)\cos(2\phi) = 2\Delta\omega C_1. \tag{38}$$

Eliminating ϕ yields

$$\Delta\omega = \pm\frac{G_{\text{sw0}}}{2\pi C_1} \times \sqrt{\text{sinc}^2\left(\frac{2t_r}{T_{\text{inj}}}\right) - \alpha^2\frac{\pi^2}{G_{\text{sw0}}^2}} \tag{39}$$

where $\alpha = G_{m0} - G_{m2} - 1/R_p - 0.5 \times (1 - 2t_r/T_{\text{inj}})G_{\text{sw0}}$. This in turn provides the optimal G_{sw0} and $\Delta\omega_{\max}$

$$G_{\text{sw0,opt}} = \frac{0.5\pi^2\left(1 - \frac{2t_r}{T_{\text{inj}}}\right)}{0.5^2\pi^2\left(1 - \frac{2t_r}{T_{\text{inj}}}\right)^2 - \text{sinc}^2\left(\frac{2t_r}{T_{\text{inj}}}\right)} \times \left(G_{m0} - G_{m2} - \frac{1}{R_p}\right) \tag{40}$$

$$|\Delta\omega_{\max}| = \frac{\omega_0\text{sinc}\left(\frac{2t_r}{T_{\text{inj}}}\right)}{2Q\sqrt{\pi^2\left[0.5 \times \left(1 - \frac{2t_r}{T_{\text{inj}}}\right)\right]^2 - \text{sinc}^2\left(\frac{2t_r}{T_{\text{inj}}}\right)} \times \left[(G_{m0} - G_{m2})R_p - 1\right]}. \tag{41}$$

In order to plot the lock range versus G_{sw0}, we need to optimize $\Delta\omega$ in (39) with respect to $G_{m0} - G_{m2}$ for each value of G_{sw0}. In other words, for each G_{sw0}, the direct ILFD sets its output amplitude such that the resulting $G_{m0} - G_{m2}$ maximizes $\Delta\omega$. Since $G_{m0} - G_{m2}$ cannot exceed the small-signal differential transconductance, $g_m/2$, the two-sided input lock range is conditionally expressed as

$$4|\Delta\omega_{\max}| = \frac{2\text{sinc}\left(\frac{2t_r}{T_{\text{inj}}}\right)}{\pi C_1}G_{\text{sw0}} \tag{42}$$

if $G_{\text{sw0}} \le (g_m - 2/R_p)/(1 - 2t_r/T_{\text{inj}})$ or as

$$4|\Delta\omega_{\max}| = \frac{2G_{\text{sw0}}}{\pi C_1}\sqrt{\text{sinc}^2\left(\frac{2t_r}{T_{\text{inj}}}\right) - \beta^2\frac{\pi^2}{G_{\text{sw0}}^2}} \tag{43}$$

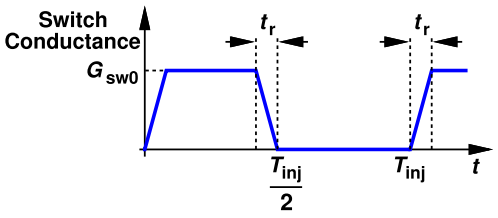


Fig. 18. Switch conductance waveform with finite rise and fall times, t_r.

if $G_{\text{sw0}} > (g_m - 2/R_p)/(1 - 2t_r/T_{\text{inj}})$. Here, $\beta = g_m/2 - 1/R_p - 0.5(1 - 2t_r/T_{\text{inj}})G_{\text{sw0}}$.

Since simulations (and measurements) are performed with a sinusoidal input, we estimate the rise and fall times of about $0.05T_{\text{inj}}$ for the switch conductance, obtaining the results shown in Fig. 5.

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