Channel Selection at RF Using Miller Bandpass Filters

Joung Won Park, *Member, IEEE*, and Behzad Razavi, *Fellow, IEEE*

***Abstract*—Channel selection at the input of RF receivers can considerably relax linearity requirements, leading to low-power, compact implementations. A GSM/WCDMA/802.11b/g receiver incorporates a Miller bandpass filter and its variants to achieve a channel bandwidth from 350 kHz to 20 MHz and a noise figure of 2.9 dB while consuming 20 mW. Fabricated in 65 nm CMOS technology, the receiver withstands a 0 dBm blocker at 20 MHz offset and exhibits a noise figure of 5.1 dB.**

***Index Terms*—High-order BPF, Miller effect, N-path filter, N-path Miller bandpass filter, RF channel selection.**

I. Introduction

CHANNEL selection at radio frequencies has remained attractive for the simplicity that it affords in receiver (RX) design. However, it has also eluded RF designers owing to the need for precise center frequency definition, the loss-selectivity trade-off of passive filters, and the noise-nonlinearity trade-off of active implementations. With the resurrection of N-path filters in recent years, these issues have been addressed vigorously, but a combination of a narrow channel bandwidth, reasonable noise performance in the presence of large blockers, and low power dissipation has not been reported. Additionally, RF channel selection for bandwidths of a few hundred kilohertz requires very large on-chip capacitors, possibly placing their parasitics in the RF signal path.

This paper describes the design of a broadband receiver that realizes channel selection at the input of the low-noise amplifier (LNA), satisfying the tough blocking requirements of GSM and WCDMA. Employing concepts such as the "Miller bandpass filter" and its variants and the "super capacitor," the receiver achieves a programmable -3 dB RF channel bandwidth from 350 kHz to 20 MHz. Designed in 65 nm CMOS technology, the prototype exhibits a noise figure (NF) of 2.9 dB without blockers and 5.1 dB with a 0 dBm blocker at 20 MHz offset.

Section II provides the background for this work and Section III deals with the receiver front-end design. Section IV describes the baseband and phase generation circuits. Section V presents the experimental results.

Manuscript received April 30, 2014; revised August 11, 2014; accepted September 21, 2014. Date of publication October 31, 2014; date of current version November 20, 2014. This paper was approved by Guest Editor Sven Mattisson. This work was supported by Lincoln Laboratory and Realtek Semiconductor.

The authors are with the Electrical Engineering Department, University of California, Los Angeles, CA 90095-1594 USA (e-mail: razavi@ee.ucla.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2014.2362843

II. Background

A. General Considerations

RF channel selection at the receiver input holds two attractions. First, by suppressing the large far-out blockers, it obviates the need for front-end SAW filters and/or high linearity in the LNA and the downconversion mixers. Second, in the absence of such blockers, it still attenuates close-in interferers, relaxing the linearity required of *all* of the stages in the signal path. It is important to distinguish between these two aspects because tolerance to large blockers (e.g., as in [1]–[4]) does not necessarily imply channel selection, and, conversely, small-signal narrow-band filtering does not necessarily entail enough linearity to handle large blockers.

The receiver blocking test required by GSM stipulates higher interferer levels at greater offset frequencies. In the extreme case, the RX must withstand a 0 dBm blocker 20 MHz away from the edge of the band while maintaining a sensitivity of -99 dBm in a 200 kHz bandwidth. The sheer strength of this blocker makes it the most demanding even though front-end filtering presumably attenuates it the most. With today's supply voltages, this blocker level must not be amplified by the LNA, allowing only two possibilities: (1) the blocker is removed by a filter before reaching the LNA, or (2) the LNA output is terminated into a virtual ground [1]–[3].[1]

B. Prior Art

The impedance translation property of N-path filters has been exploited recently to develop narrowband filters with precise center frequencies. Described by [1], [4]–[7], frequency-translated transfer functions can be traced back to the comb filters and "commutated networks" described in [8]–[10]. In fact, [9] and [10] analyze the circuit shown in Fig. 1(a) with N non-overlapping LO phases, find an analogy to a reflective transmission line, and derive a two-sided -3 dB bandwidth for each of the translated frequency responses equal to

$$f_{3\text{ dB}} = \frac{1}{\pi N R_S C_L}. \tag{1}$$

While not exact, this expression does reveal the trade-off between the total capacitance, NC_L, and the bandwidth; e.g., $NC_L = 32$ nF for $R_S = 50\ \Omega$ and a bandwidth of 200 kHz. Interestingly, [9] and [10] recognize that $R_S C_L$ must be much greater than the on-time of the switches so as to create a harmonically rich voltage and hence a significant magnitude for the translated response.

[1]In other words, the LNA is realized as a transconductance amplifier.

0018-9200 © 2014 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

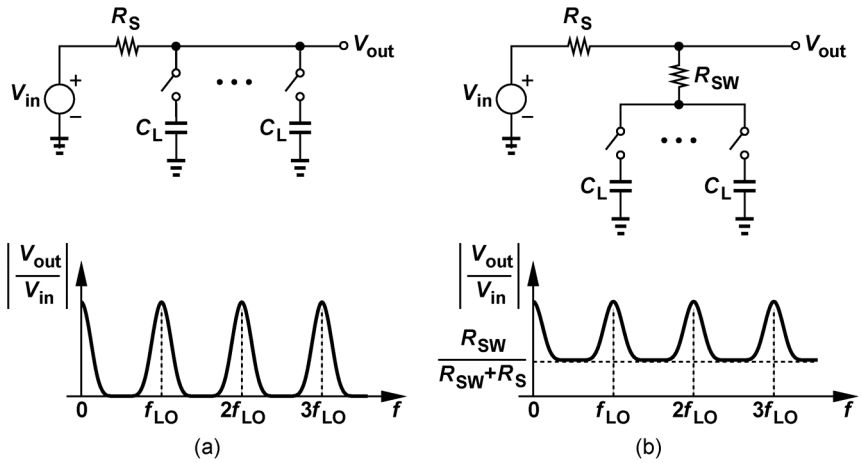


Fig. 1. N-path filter: (a) ideal, and (b) with switch on-resistance.

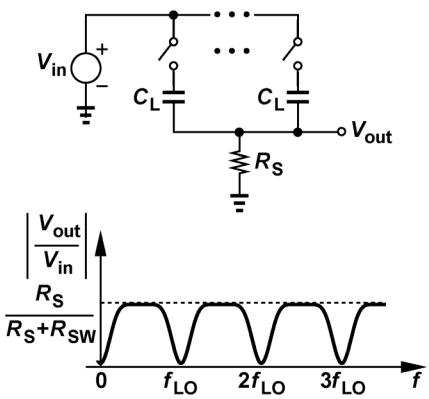


Fig. 2. N-path notch filter.

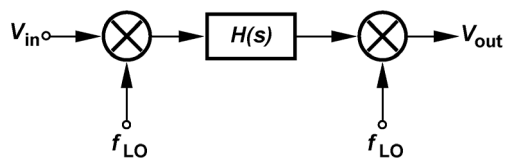


Fig. 3. Model for translational circuits.

Absent from the above expression is the on-resistance of the switches, R_{SW}. Since only one switch is on at a time, we can factor out R_{SW} as shown in Fig. 1(b). We now recognize that, as the translated impedance falls at high offset frequencies, R_{SW} eventually becomes dominant, limiting the transfer function to $R_{SW}/(R_{SW} + R_S)$. In other words, to maximize the out-of-channel rejection, R_{SW} must be minimized, demanding high power dissipation in the LO phase generation circuitry.

In analogy with low-pass to high-pass transformation of a first-order RC circuit, we can swap the commutated capacitors in Fig. 1(a) with R_S, obtaining the *notch* filter shown in Fig. 2. The notch behavior is evident by noting that the translated impedance of the commutated capacitors is infinite at the LO frequency, $f_{\rm LO}$, yielding $V_{\rm out} = 0$, and falls as the input frequency, $f_{\rm in}$, departs from $f_{\rm LO}$, yielding $V_{\rm out} \neq 0$. This topology has been described in [11] in 1953 and [12] in 2012 and also follows the selectivity limitations mentioned above due to R_{SW}. That is, while the width of the notch depends on the total capacitance, the out-of-channel transmission is limited to $R_S/(R_S + R_{SW})$.

With the aid of N-path filters, a number of recent designs have achieved blocker tolerance or channel selection. The filter in [4] offers a bandwidth of 8 MHz with a total capacitance of 1.27 nF while drawing about 65 mW at 1.2 GHz. (The circuit does not provide input matching.) The work in [13] incorporates two instances of the circuit shown in Fig. 1(a), reaching a bandwidth of 14 MHz with a total capacitance of 440 pF. The receiver's NF in the presence of a 0 dBm blocker at 80 MHz offset rises to 11.4 dB. The work in [14] employs translational circuits in four feedback paths around an amplifier, obtaining a bandwidth of 5 MHz with a total capacitance of 60 pF. However, the circuit consumes 62 mW to avoid instability due to the feedback pole resulting from the parasitics of the capacitors. Also, in the presence of a large blocker, the amplifier in the feedback path may saturate, possibly providing much less rejection than small-signal analysis indicates. Moreover, the NF in the presence of a blocker is not reported.

One might ask whether it is possible to redesign the foregoing three circuits for GSM. Rough calculations suggest that the topology in [13] would require a total capacitance of 30 nF, and that in [14] a total power of 150 mW. But, we should also remark that the N-path filters described above exhibit only a gradual roll-off. Thus, even if area and power penalties are ignored, one could not simultaneously achieve a flat response within the desired channel and significant rejection in the adjacent or alternate adjacent channel (Section III-E). Although the work in [4] exhibits a flat frequency response over the bandwidth, it would require roughly 50 nF to achieve a bandwidth of 200 kHz.

In the analysis and design of commutated networks, it is helpful to construct frequency-translated models of circuits, e.g., view a baseband low-pass function as a band-pass filter centered around $f_{\rm LO}$, or a baseband high-pass function as an RF notch. Such transformations are justified by the general model shown in Fig. 3, where $H(s)$ denotes the equivalent baseband response if $V_{\rm in}$ and $V_{\rm out}$ are in the vicinity of $f_{\rm LO}$. This model

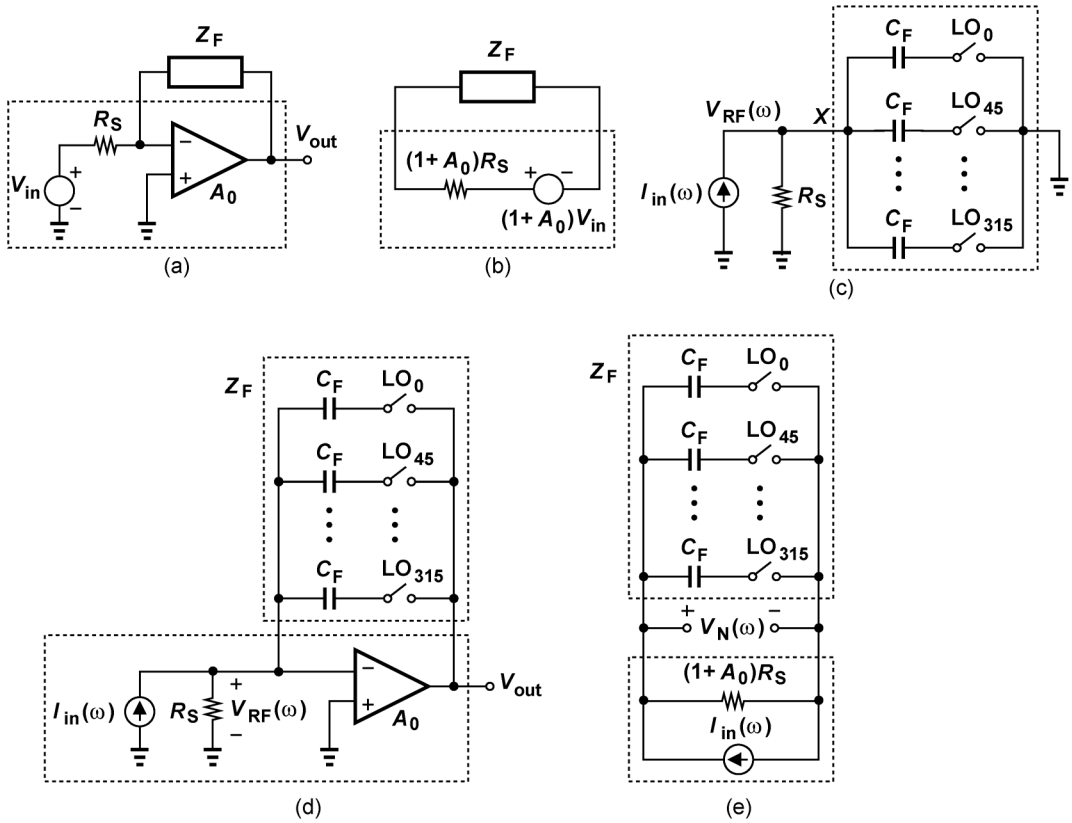


Fig. 4. (a) Miller effect with ideal amplifier, (b) Thevenin equivalent model, (c) ideal 8-path filter, (d) 8-path Miller filter, and (e) Norton equivalent model.

was originally used in [15] to study N-path filters. (A more exact model must incorporate quadrature downconversion and upconversion to avoid corruption by images as described in [6], [7].)

III. Receiver Front End Design

This section describes step-by-step the evolution of the proposed receiver architecture. We introduce various ideas, identify their issues, and present additional methods of dealing with the issues. With the aid of Cadence's pss and pnoise simulations, we quantify the behavior of the proposed circuits, but, for the sake of brevity, we do not use the term "simulated" in each case.

A. Miller Bandpass Filter

Consider the negative-feedback circuit shown in Fig. 4(a), where Z_F denotes an arbitrary impedance. With an ideal amplifier, we can say R_S sees an impedance of $Z_F/(1+A_0)$. Alternatively, we can find the Thevenin equivalent seen by Z_F, as depicted in Fig. 4(b), recognizing that R_S is *boosted* by a factor of $1+A_0$ as it is presented to Z_F. This alternative view of the Miller effect proves useful in our front end design.

Now, consider the topology shown in Fig. 4(c), where the switches are driven by eight 12.5%-duty-cycle non-overlapping LO phases. If $R_S C_F$ is large enough to allow a harmonically rich voltage waveform at node X, this network exhibits a bandpass impedance centered around $f_{\rm LO}$. Let us place the 8-path network around an amplifier as shown in Fig. 4(d). We wish to analyze the behavior of this arrangement, assuming an ideal amplifier for now. In analogy with the transformation shown in Fig. 4(b), we construct the Norton equivalent seen by Z_F [Fig. 4(e)] and obtain a topology similar to that in Fig. 4(c) except that R_S is boosted to $(1+A_0)R_S$. The impedance equation for Fig. 4(c) [7] can therefore be readily modified for Fig. 4(e):

$$\frac{V_N}{I_{\rm in}}(\omega) = \frac{(1+A_0)R_S}{(1+A_0)R_S + R_{SW}} \times \left[R_{SW} + \frac{\frac{16}{\pi^2}(2-\sqrt{2})(1+A_0)R_S}{1+j8\left[(1+A_0)R_S + R_{SW}\right] C_F(\omega-\omega_{\rm LO})} \right]. \quad (2)$$

Since V_N in Fig. 4(e) is equal to $(1+A_0)V_{RF}$ in Fig. 4(d), we have

$$\frac{V_{RF}}{I_{\rm in}}(\omega) = \frac{R_S}{R_S + \frac{R_{SW}}{1+A_0}} \times \left[\frac{R_{SW}}{1+A_0} + \frac{\frac{16}{\pi^2}(2-\sqrt{2})R_S}{1+j8\left(R_S + \frac{R_{SW}}{1+A_0}\right)(1+A_0)C_F(\omega-\omega_{\rm LO})} \right]. \quad (3)$$

Thus, the proposed topology maintains the bandpass nature of the 8-path network but offers two critical advantages. (1) The unit capacitor, C_F, is multiplied by $1+A_0$, saving considerable area. With an LNA voltage gain of 20, $8C_F$ can be as low as 1.5 nF, but a total capacitance of 2 nF is chosen for margin. (2) The on-resistance of the switches is reduced by a factor of $1+A_0$, proportionally scaling down the power dissipated by the LO path.

The circuit in Fig. 4(d) can also be viewed as one incorporating a *notch* filter (similar to that in Fig. 2) in its feedback path,

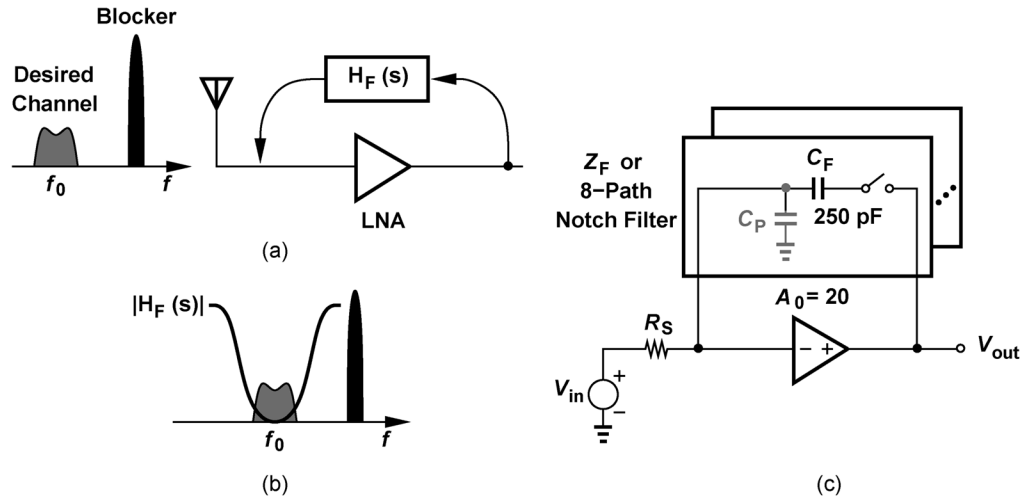


Fig. 5. (a) RX front end with frequency-selective network in feedback path, (b) desired $H_F(s)$, and (c) RX front end with N-path notch filter in feedback path.

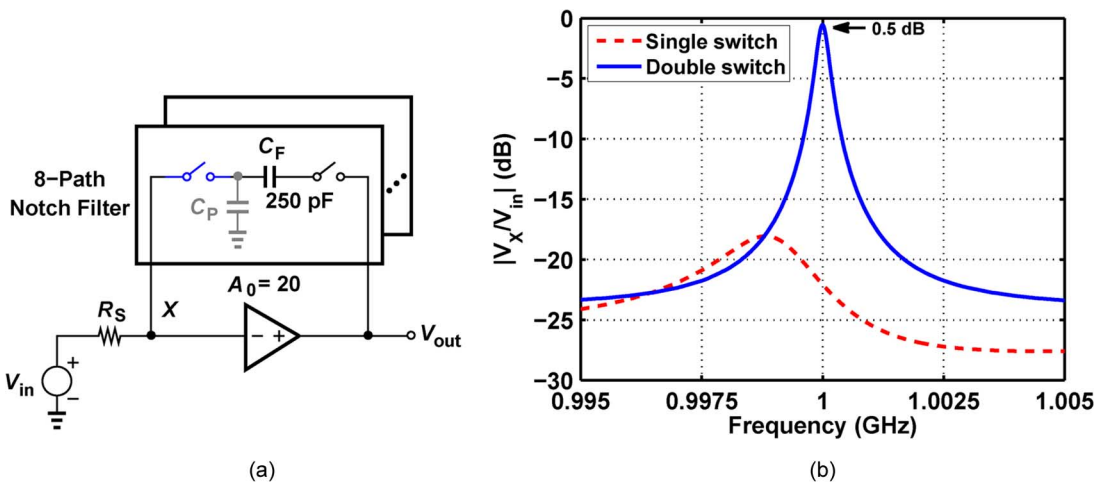


Fig. 6. (a) Double-switch N-path notch filter around LNA. (b) Frequency response of $V_X/V_{\rm in}$.

allowing stronger feedback as the input frequency departs from $f_{\rm LO}$ and attenuating out-of-channel components. Fig. 5 summarizes our findings thus far, visualizing the feedback network as either an impedance, Z_F, or a notch filter, $H_F(s)$.

Unfortunately, the parasitics of $8C_F$ in Fig. 5(c) amount to $C_p \approx 100$ pF, severely attenuating the RF signal. Fig. 6(a) depicts a modification whereby an additional series switch upconverts C_P as seen at node X. The two switches are driven by the same LO phase. Fig. 6(b) plots the response from $V_{\rm in}$ to V_X with and without the additional switch. In the absence of the switch on the left, C_P loads the input, introducing nearly 20 dB of loss and degrading the selectivity—even at 1 GHz. (For negligible impact on the performance up to 2 GHz, C_P would be limited to 0.5 pF.)

For a fair comparison in terms of LO loading, each switch size in Fig. 6(a) is half the original switch in Fig. 5(c). Thus, the overall switch on-resistance in Fig. 6(a) is four times that in Fig. 5(c) and (3). Fig. 7 plots the simulated frequency response from $V_{\rm in}$ to V_X in Fig. 6(a) along with that of the passive filter in Fig. 1(b) for $N = 8$. The close-up view in Fig. 7(a) indicates that, by virtue of Miller effect, the -3 dB bandwidth falls from 3 MHz to about 150 kHz. Additionally, the wider span in Fig. 7(b) reveals that the out-of-channel rejection rises by 13 dB. We observe that the rejection reaches a plateau of about 28 dB beyond ± 5 MHz, making the 0 dBm, 20 MHz-offset GSM blocker test more demanding that the -23 dBm, 5 MHz-offset test.

The Miller-multiplied capacitance of the feedback notch filter directly fights the blocker emerging from the antenna. Implicit in our analysis is the assumption that the LNA itself provides a gain of A_0 even in the presence of a large blocker. We return to this point in Section III-C.

B. Circuit Implementation

This work employs the LNA topology proposed in [16] and modified in [17]. Depicted in Fig. 8(a), the three-stage topology avoids the use of inductors and incorporates resistive feedback to establish input matching. The input impedance, $Z_{\rm in}$, is now equal to that in (2) in parallel with $R_F/(1 + A_0)$. Drawing a total bias current of 8.6 mA from a 1.2 V supply, the closed-loop LNA (without the notch filter) exhibits a bandwidth of 9.5 GHz, a noise figure of 1.4 dB, and an input 1 dB compression point $(P_{1\ \rm dB})$ of -25 dBm. Such a low $P_{1\ \rm dB}$ brings into question the ability of the circuit to handle a 0 dBm blocker.

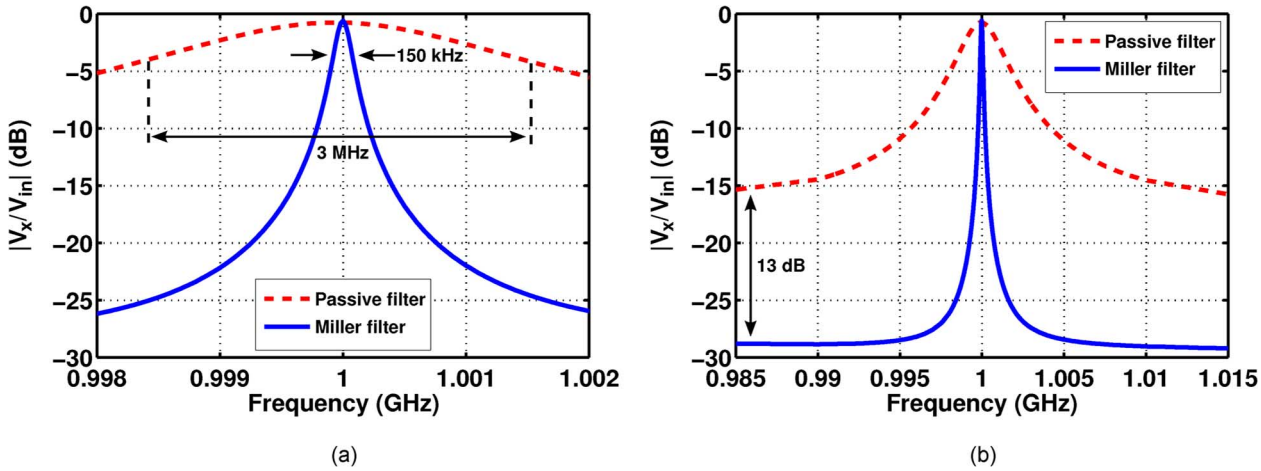


Fig. 7. (a) Close-in response of 8-path filter without and with Miller effect. (b) Stopband rejection for the two cases.

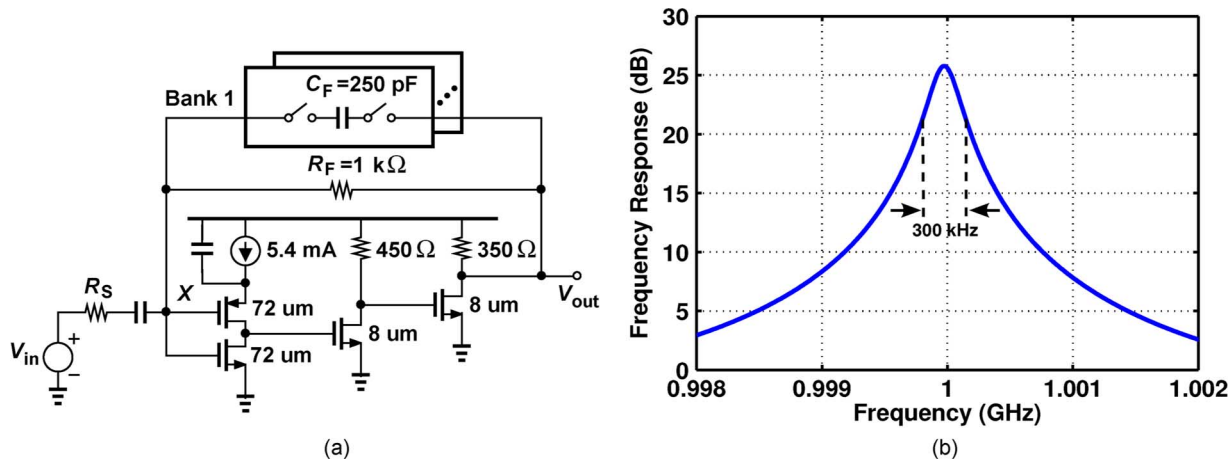


Fig. 8. (a) First attempt at front-end implementation. (b) Frequency response to LNA output.

Fig. 8(b) plots the frequency response of the overall front end, displaying a gain of 26 dB and a slight increase in the bandwidth due to the shunting effect of R_F. Also evident is a small shift in the center frequency from $f_{\rm LO} = 1$ GHz. This phenomenon is studied in Section III-F.

C. Local Miller Filter

An important question that we must answer is, does the LNA of Fig. 8(a) maintain its gain of $A_0 = 20$ when sensing a 0 dBm blocker? From a different perspective, we can ask, if the LNA input acts as a virtual ground under this condition, then through which path does the large blocker current flow? The peak current of 632 mV/50 Ω = 12.64 mA must primarily travel *forward* through the notch filter and be absorbed by the third stage of the LNA.[2] Unfortunately, this stage can neither source nor sink this much current. As a result, V_X in Fig. 8(a) experiences a swing of 726 mV_{pp}, saturating the last two stages of the LNA. The front end NF thus rises to 12 dB. This saturation mechanism can also occur in the feedback loop employed in [14].

[2]As a worst-case scenario, the peak amplitude of the antenna voltage is assumed 632 mV_p because the heavy impedance mismatch at the blocker frequency allows the Thevenin voltage of the antenna to appear at the LNA input without a 2X attenuation.

In order to resolve this issue, we add a local Miller filter around the first stage. Illustrated in Fig. 9(a), the idea is to attenuate the blocker before it reaches the last two stages. To avoid area penalty, the capacitors in Bank 1 are reduced to 50 pF and those in Bank 2 are chosen equal to 100 pF. The behavior of the modified front end can be analyzed by means of the approximate, unilateral model shown in Fig. 9(b), where A_1, A_2, and A_3 denote the gains of the three LNA stages, respectively. (In this design, $A_1 = 6.2$, $A_2 = 2.1$, and $A_3 = 1.6$.) We have

$$\frac{V_{\rm out}}{V_{\rm in}} = \frac{-A_1A_2A_3}{1 + H_2A_1 + H_1A_1A_2A_3}, \tag{4}$$

predicting a *wider* channel bandwidth because the capacitance in H_2 (which has been deducted from that in H_1) is multiplied by A_1 rather than by $A_1A_2A_3 = A_0$. The output of the first stage is expressed as

$$V_Y = \frac{-A_1}{1 + H_2A_1 + H_1A_1A_2A_3}V_{\rm in}, \tag{5}$$

exhibiting a greater blocker attenuation with H_2 present because the far-out rejection provided by H_1 and H_2 is only a function of the switch on-resistance and not of the total capacitance.

Fig. 10 plots the simulated LNA noise figure and frequency response with and without a 0 dBm blocker at 20 MHz offset.

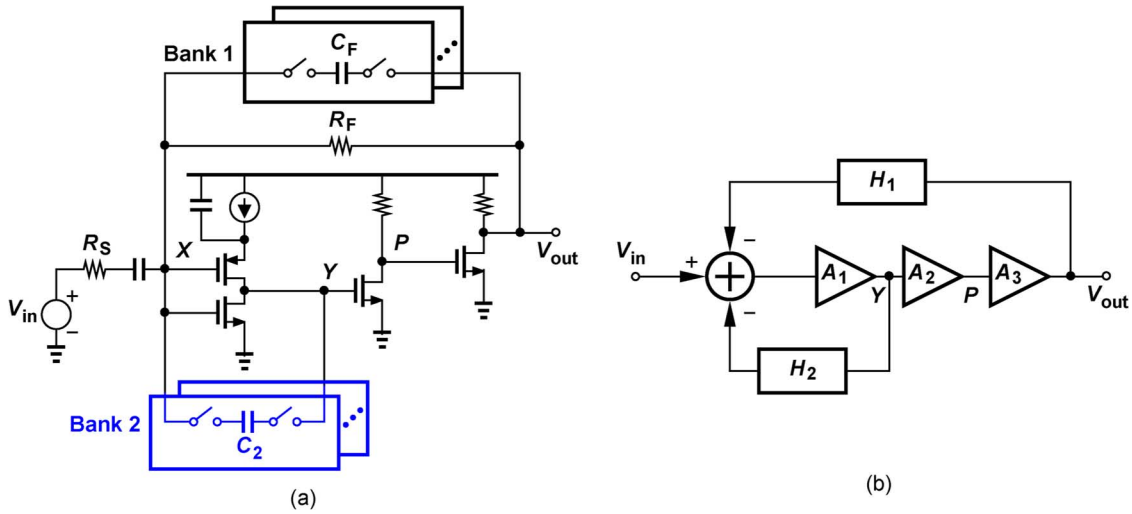


Fig. 9. (a) Local Miller filter (Bank 2). (b) Simplified model.

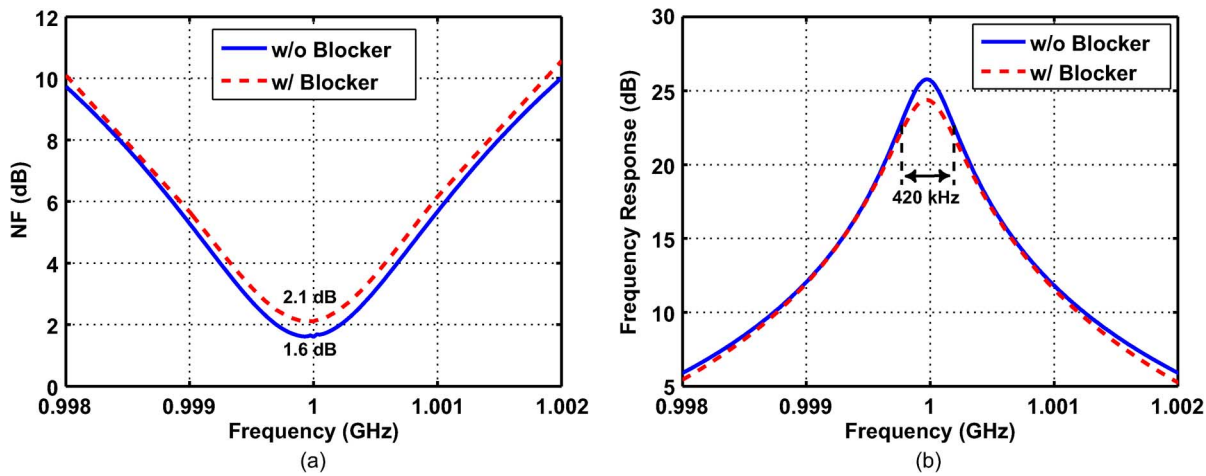


Fig. 10. Effect of local Miller filter on (a) NF with a 0 dBm blocker at 20 MHz offset, and (b) input-output frequency response.

The out-of-band input $P_{1\,\mathrm{dB}}$ has been improved to -1 dBm compared to the original $P_{1\,\mathrm{dB}}$ of -25 dBm. The NF is negligibly affected, but the bandwidth is increased to 420 kHz. This is because the total allowable capacitance of 2 nF is now partitioned between Bank 1 and Bank 2 while Bank 2 entails less Miller multiplication (due to less gain around it). Moreover, the first-order nature of the notch creates only a gradual decline in the gain.

Table I summarizes the blocker peak-to-peak voltage swings observed at different nodes in Fig. 9(a) with only the first bank or both banks present. We conclude that Bank 2 reduces the swings to a level well below the compression point of each stage. In fact, it is this criterion that dictates the partitioning of the total capacitance between Bank 1 and Bank 2. In this case, about 8.5 mA of the blocker current is absorbed by the first stage as a result of its class-AB operation and the remainder by the third.

TABLE I
PEAK-TO-PEAK VOLTAGES FOR NODES WITHIN LNA IN THE PRESENCE OF A 0 dBm BLOCKER AT 20 MHz OFFSET

(mV_{PP})	V_X	V_Y	V_P	V_{out}
with Bank 1	726	1180	1090	296
with Banks 1 and 2	210	154	330	132

D. Unilateral Miller Filter

In order to reduce the filter bandwidth in Fig. 9(a) without increasing the value of the capacitors, we seek a means of raising the loop gain. Since the LNA gain is limited by the voltage headroom and trades with the compression point, we insert a gain stage in the feedback path, thus arriving at the "unilateral Miller filter" (Bank 3) depicted in Fig. 11(a). Here, C_M is multiplied by $1+A_0A_1 = 1+20\times17.8 = 357$, saving considerable capacitor area. With $C_F = 50$ pF, $C_2 = 100$ pF, and $C_M = 12.5$ pF, we obtain the frequency response plotted in Fig. 11(b), i.e., a bandwidth of 200 kHz. Owing to the additional gain in Bank 3, the total capacitance is reduced to 1.3 nF.

The use of A_1 in the feedback path raises two issues. First, the noise–power trade-off of eight instances of the amplifier is critical. We analyze the noise contribution with the aid of the equivalent circuit shown in Fig. 12(a), where V_{n1} is the input-referred noise voltage of A_1 and the effect of Bank 1 and Bank 2

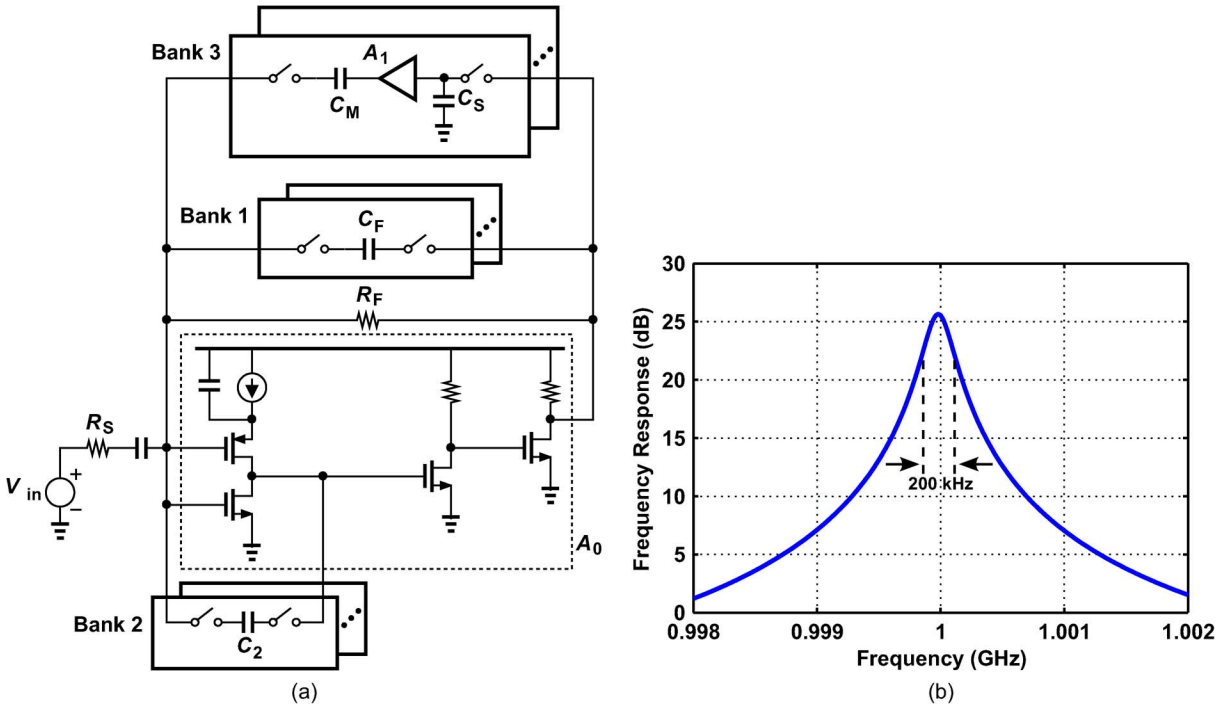


Fig. 11. (a) RX front end with unilateral Miller path. (b) Corresponding frequency response.

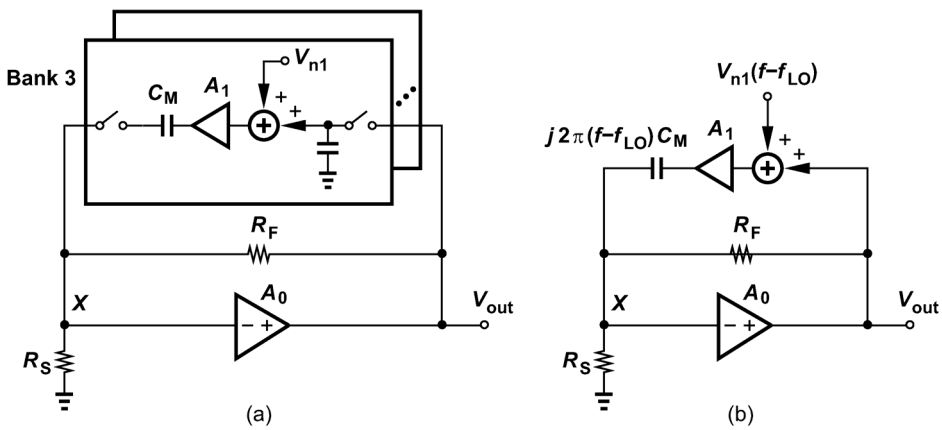


Fig. 12. (a) Noise model of A_1. (b) Noise model after frequency translation to RF.

is neglected.[3] Assuming a unity conversion gain for the mixing operations preceding and following A_1, we can translate both V_{n1} and $j2\pi f C_M$ to RF, and denote them by $V_{n1}(f - f_{\rm LO})$ and $j2\pi(f - f_{\rm LO})C_M$, respectively [Fig. 12(b)]. Summing the currents at X gives

$$-\frac{V_{\rm out}(f)}{A_0 R_S} = \frac{V_{\rm out}(f) + V_{\rm out}(f)/A_0}{R_F} + [V_{\rm out}(f) + V_{n1}(f - f_{\rm LO})]\, A_1\, [j2\pi(f - f_{\rm LO})C_M]\,. \quad (6)$$

That is,

$$\frac{V_{\rm out}(f)}{V_{n1}(f - f_{\rm LO})} = \frac{A_0 A_1 R_S R_F j2\pi(f - f_{\rm LO})C_M}{(1+A_0A_1)R_S R_F j2\pi(f - f_{\rm LO})C_M + R_F + (1 + A_0)R_S}. \quad (7)$$

[3]These two banks provide little feedback within the desired channel.

This result implies that V_{n1} experiences a notch filter as it is upconverted and travels to the output, vanishing at $f - f_{\rm LO}$. This behavior can be explained intuitively: since the left plate of C_M in Fig. 12(a) sees a *resistance* (i.e., the impedance downconverted by the switch on the left), C_M acts as a high-pass filter in the baseband, blocking the very low frequency components in V_{n1}. Upon translation to RF, the high-pass characteristic is transformed to a notch. Recognizing that input matching translates to $R_F = (1 + A_0)R_S \approx A_0 R_S$, we simplify (6) to

$$\frac{V_{\rm out}(f)}{V_{n1}(f - f_{\rm LO})} = \frac{A_1 R_F j\pi(f - f_{\rm LO})C_M}{1 + A_1 R_F j\pi(f - f_{\rm LO})C_M} \quad (8)$$

which corresponds to a baseband high-pass filter consisting of a capacitance equal to $A_1 C_M$ and a resistance equal to $R_F/2$.

Fig. 13 plots the noise transfer function of the actual circuit as predicted by Cadence's pss simulation. Although the attenuation remains greater than 70 dB for offset frequencies up to

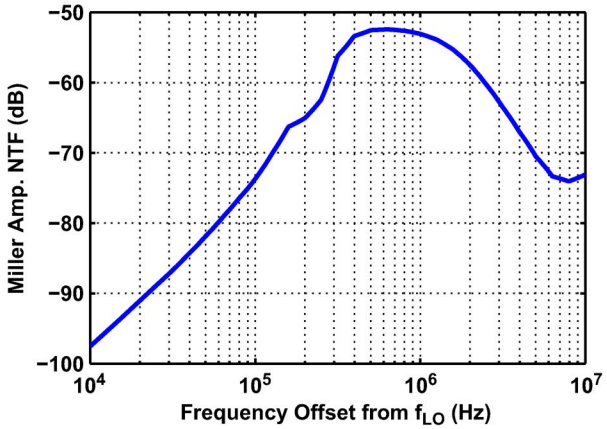


Fig. 13. Noise transfer function of A_1.

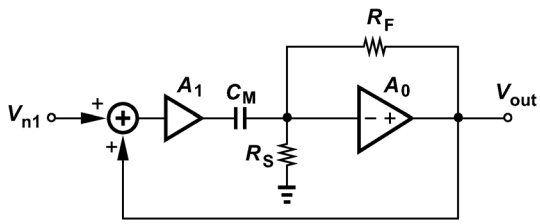


Fig. 14. Baseband model for noise analysis.

100 kHz, the flicker noise of A_1 must be confined so as to ensure negligible degradation of the RF noise figure. Nevertheless, A_1 draws only 0.46 mW for its relaxed noise requirements. From Fig. 12(a), we observe that the kT/C noise generated at the input of A_1 is indistinguishable from the noise of A_1 itself. Thus, kT/C noise sees the same notch response as it travels to the main output and is heavily attenuated. The choice of $C_S = 20$ fF ensures a safe bound on this noise but is not stringent; note that, as seen by the LNA output, C_S is upconverted and does not load the LNA. Interestingly, intermodulation components generated by these amplifiers also experience this transfer function. The linearity is therefore relaxed up to the compression point, at which the Miller multiplication factor begins to roll off.

Rather than upconvert V_{n1} and C_M to RF, the above analysis could downconvert the remainder of the circuit to baseband, leading to the model shown in Fig. 14, where the poles and zeros of A_0 are shifted by an amount equal to $f_{\rm LO}$. This model yields (7) if $A_1 \gg 1$, but it also facilitates the stability analysis as explained below.

The second issue related to the unilateral notch filter is potential loop instability due to the poles contributed by A_1. We study this issue by examining the loop transmission in Fig. 12(a), noting that A_1 exhibits three poles at 350 MHz, 290 MHz, and 16 MHz, the last one arising from the output resistance of A_1 and the parasitic component of C_M. Along with those of A_0, these poles may cause significant unwanted peaking in the closed-loop response.

Fortunately, the strong feedback provided by Bank 1 overwhelms the phase shift through Bank 3, guaranteeing stability. This can be seen from the baseband model shown in Fig. 15,

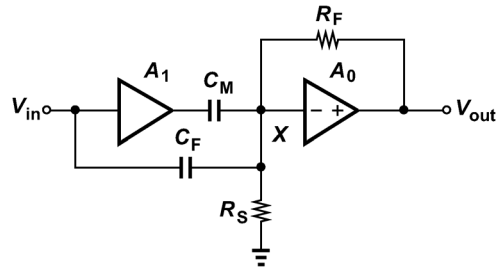


Fig. 15. Baseband model for stability analysis.

where C_F and resistance seen at X form a high-pass filter representing the RF notch action. With a corner frequency of a few hundred kilohertz, this path exhibits a low impedance at the pole frequency of A_1, minimizing the excess phase shift.

Plotted in Fig. 16(a) and (b) are the magnitude and phase of the loop transmission of the actual circuit before and after Bank 1 is added. The phase margin increases from 6° to 104°.

E. Higher Order Response

As mentioned in Section II-B, the first-order response obtained by commutated capacitors provides only moderate rejection of close-in blockers if the droop within the desired channel must be small. It is therefore desirable to seek a circuit that offers a higher order roll-off. Recall from Fig. 11(a) that C_M is multiplied by $1 + A_0A_1$, creating an admittance equal to $(1+A_0A_1)C_Mj2\pi(f-f_{\rm LO})$ at the input. We note that A_1 need not be constant with frequency and can play a role in shaping the response. Intuitively, we prefer that A_1 *increase* with frequency so as to elevate the Miller multiplication of C_M at greater frequency offsets. For example, if $A_1(s) = ks$, then the RF equivalent of the Miller effect is given by $[1 + A_0kj2\pi(f - f_{\rm LO})]C_Mj2\pi(f - f_{\rm LO}) \approx -kA_0C_M4\pi^2(f - f_{\rm LO})^2$. We say "super Miller effect" has created a "super capacitor" in this case because the admittance is proportional to $(f - f_{\rm LO})^2$ rather than $(f - f_{\rm LO})$.

Depicted in Fig. 17(a), A_1 contains two zeros to sharpen the selectivity. The large transistor dimensions in the first stage yield an input-referred noise of 454 nV/$\sqrt{\rm Hz}$ at 10 kHz. The frequency response (with the parasitics of C_M included) is shown in Fig. 17(b), displaying the effect of the zeros in the range of 10 kHz to 1 MHz. Fig. 17(c) plots the front-end frequency response, revealing about 20 dB of rejection at 400 kHz offset but also 4 dB of peaking at the lower edge.

F. Polyphase Notch Filter

Despite the dominance of Bank 1 over Bank 3 in Fig. 11(a), the frequency response of the front end suffers from 4 dB of peaking near the lower edge of the passband. This phenomenon is caused by the total phase shift that the signal experiences as it travels through the LNA and the unilateral path. While not so much as to create instability, this phase shift alters the nature of the Miller bandpass filter by introducing a *real* feedback current flowing through the feedback capacitors and an *imaginary* feedback current flowing through the feedback resistor. To see this point, we recognize that the Miller effect of C_M is now expressed as

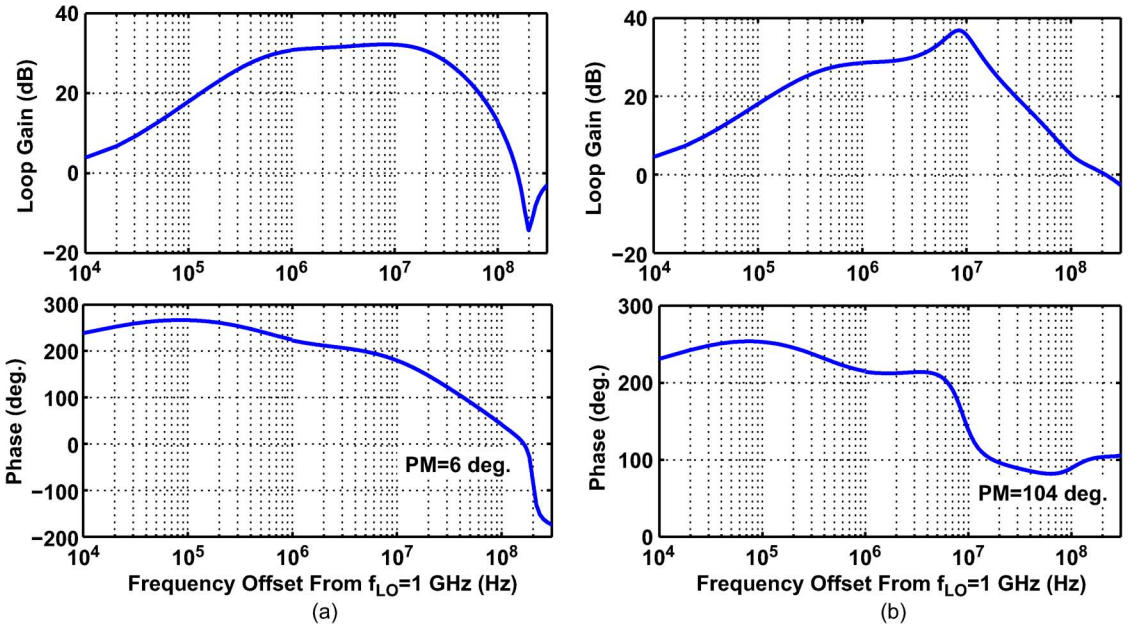


Fig. 16. Front end (a) loop gain and phase without Bank 1, and (b) with Bank 1.

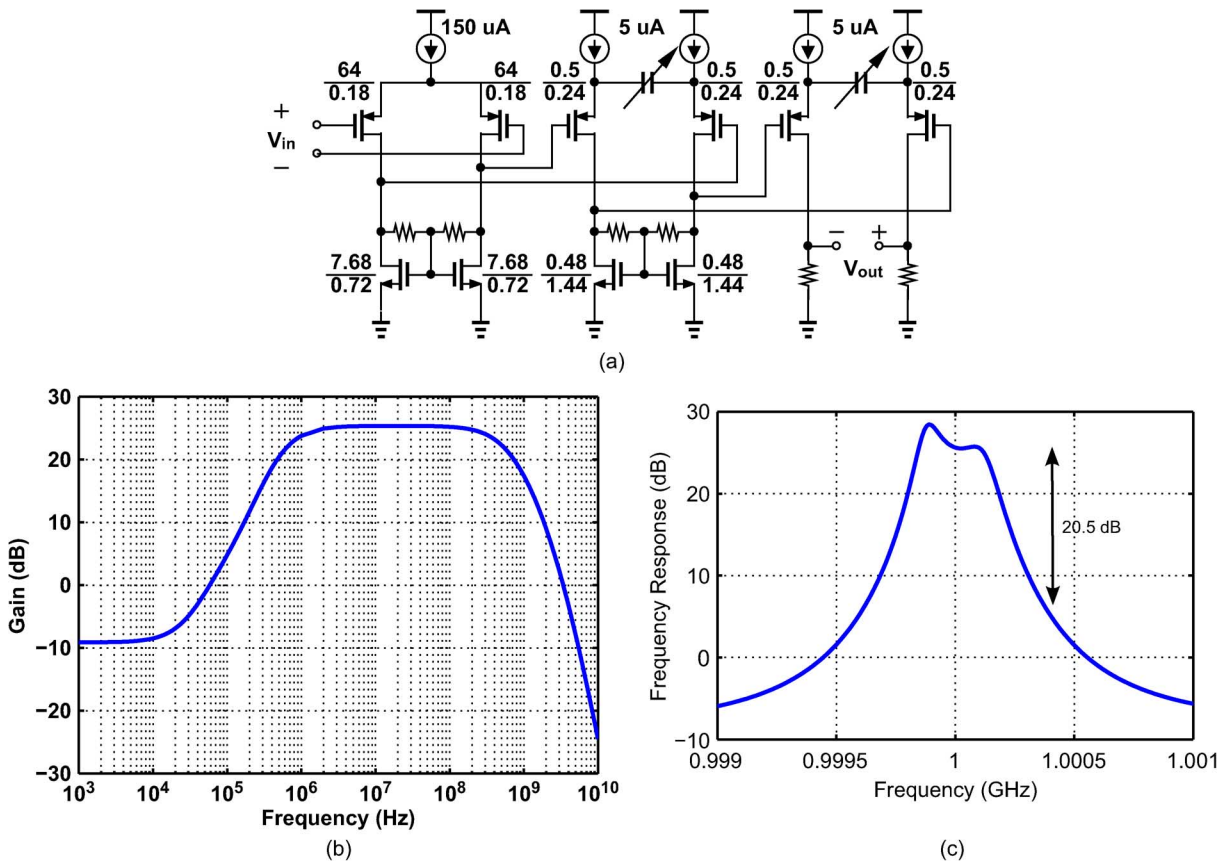


Fig. 17. (a) Three-stage Miller amplifier, (b) Miller amplifier frequency response, and (c) front end response.

$A_0(\omega)A_1(\omega - \omega_{\rm LO})\exp(-jt_d\omega)C_M j2\pi(f - f_{\rm LO})$, where t_d denotes the equivalent delay around the loop. Multiplied by $\cos\omega t_d - j\sin\omega t_d$, the capacitor returns a real current and no longer appears as a pure capacitance at the input. The slight shift of the peak in Fig. 11(b) also stems from this effect because now the maximum feedback impedance occurs at $f \neq f_{\rm LO}$ (Appendix II).

In order to reduce the peaking, the current flowing through C_M can be so modified as to become completely imaginary. In other words, the current must be *rotated* in the opposite direction by ωt_d radians. This should be possible with the aid of the eight phased currents present in Bank 3 in a manner similar to [4], [20], and [21]. As shown in Fig. 18(a), we decompose each A_1 into two amplifiers and each C_M into two capacitors, injecting

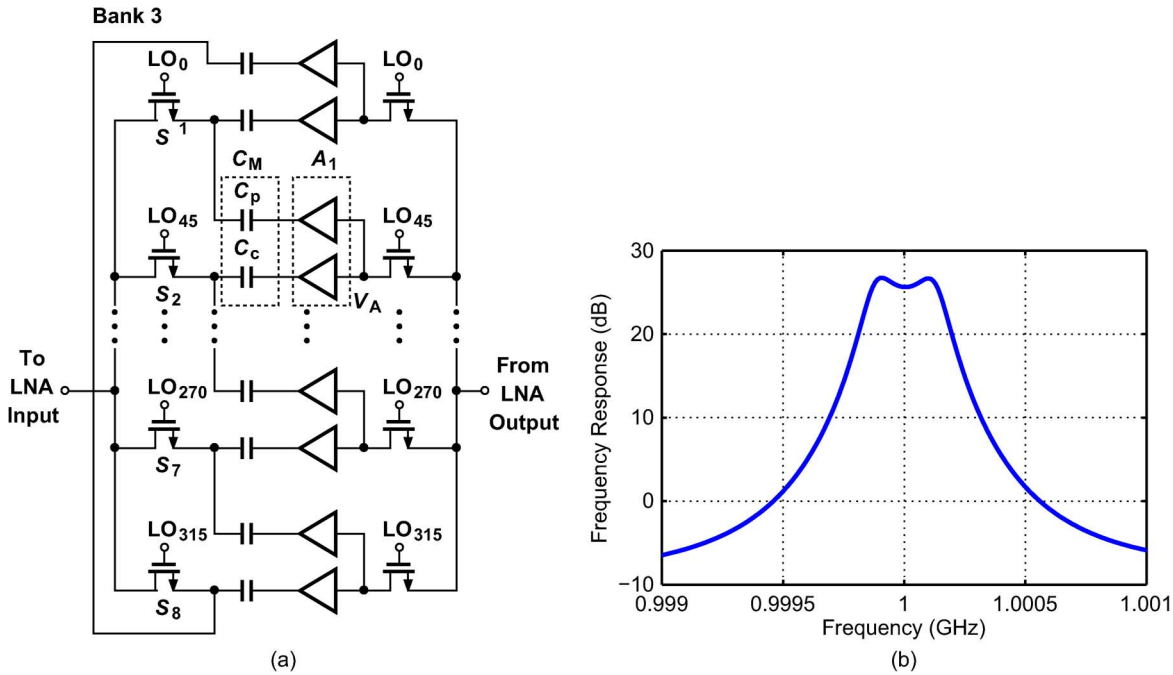


Fig. 18. (a) Polyphase Miller notch filter, and (b) its effect on peaking.

a fraction of the feedback signal from one branch into its adjacent branch. The current flowing through the main capacitor, C_c, is approximately equal to $A_1 V_A j C_c(\omega - \omega_{\rm LO}) \exp(-j\omega t_d)$, where $A_1 V_A \exp(-j\omega t_d)$ denotes the output voltage of A_1, and that injected from the adjacent branch is given by $A_1 V_A j C_p(\omega - \omega_{\rm LO}) \exp(-j\omega t_d) \exp(j2\pi/8)$. The sum of these two currents returns to the LNA input and must be purely imaginary. Expanding the sum and setting the real part to zero, we have, for ω in the vicinity of $\omega_{\rm LO}$,

$$\frac{C_p}{C_c} = \frac{\sqrt{2}\sin\omega_{\rm LO} t_d}{\sin\omega_{\rm LO} t_d - \cos\omega_{\rm LO} t_d} = \frac{2\sin\omega_{\rm LO} t_d}{\sin(\omega_{\rm LO} t_d - \pi/4)}. \quad (9)$$

Thus, according to the frequency band of interest, C_p and C_c can be programmed to satisfy this equation while their sum is close to the nominal value of C_M. Fig. 18(b) demonstrates the result for $C_p/C_c = 4/10$ at 1 GHz, indicating that, due to polyphase action, the peaking on the lower edge decreases and that on the upper edge increases. Simulations suggest that, with this setting, the peaking increases by 0.8 dB and 1.3 dB at the slow-slow, 75°C and fast-fast, 0°C corners of the process, respectively.

IV. Complete Receiver

A. Harmonic-Rejection Mixing

The receiver front end developed in the previous sections performs channel selection and blocker suppression at the input of the LNA, but it also produces the baseband signals in eight phases within each of the banks. In particular, the baseband components generated in Bank 1 contain the least amount of noise[4] and can serve as outputs. Simple amplifiers with relaxed linearity can follow these outputs, enlarging the signal level to reach the full scale of the baseband ADCs. Unfortunately, the broadband noise of the LNA is mixed with the higher LO harmonics, raising the receiver NF from about 2.5 dB to 4 dB at 50 kHz offset. As shown in Appendix I, the NF of a broadband receiver is approximately equal to

$$NF_{tot} = \frac{\pi^2}{8} NF_{LNA} + \frac{NF_{mix} - \pi^2/8}{A_V^2} \cdot \frac{R_{\rm out1}}{R_S} \quad (10)$$

when NF_{mix} is calculated with respect to the LNA output resistance, $R_{\rm out}$, and A_V is the voltage gain from the signal source to the LNA output.

In order to avoid broadband noise downconversion, the baseband amplifiers can be decomposed and reconfigured so as to create harmonic-rejection mixing. As shown in Fig. 19(a), the eight baseband outputs produced by Bank 1 are converted to current by properly ratioed G_m stages and combined. The weighting factor of $1 + \sqrt{2}$ is different from that in prior work [18] owing to our use of 12.5%-duty-cycle mixing. Depicted in Fig. 19(b), the equivalent LO waveforms are nominally free from $(8n - 4 \pm 1)$th harmonics. To minimize the flicker noise of the G_m stages, a W/L of 48 μm/1.2 μm is chosen for the weighting factor of 1. Realized as simple differential pairs with no degeneration, the G_m stages consume a total power of 1.1 mW and pose a receiver NF penalty of 0.4 dB at 50 kHz offset. If rejection of large blockers at the LO harmonics is desired, other techniques [17], [19] can be applied as well.

B. Low-Power 12.5% Duty Cycle Generation

The generation of eight LO phases with 12.5% duty cycle can consume substantial power, e.g., 30 mW at 2 GHz in 40 nm technology [3]. We propose an approach that reduces the power to 7.1 mW at the same rate in 65 nm technology. Of course, some of these savings accrue due to the smaller switches afforded by the Miller notch filter and its variants.

[4]Because the widest switches are used in this bank for negligible $1/f$ noise generation in the presence of a large blocker.

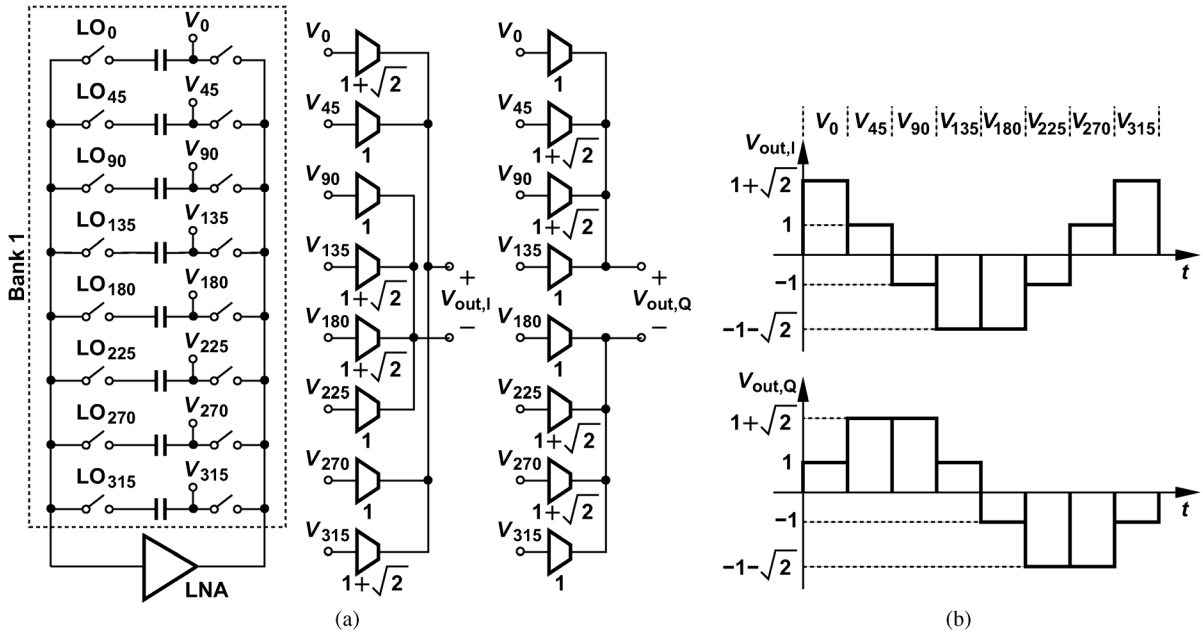


Fig. 19. (a) Harmonic-rejection mixing by properly ratioed G_m stages, and (b) equivalent waveforms for quadrature outputs.

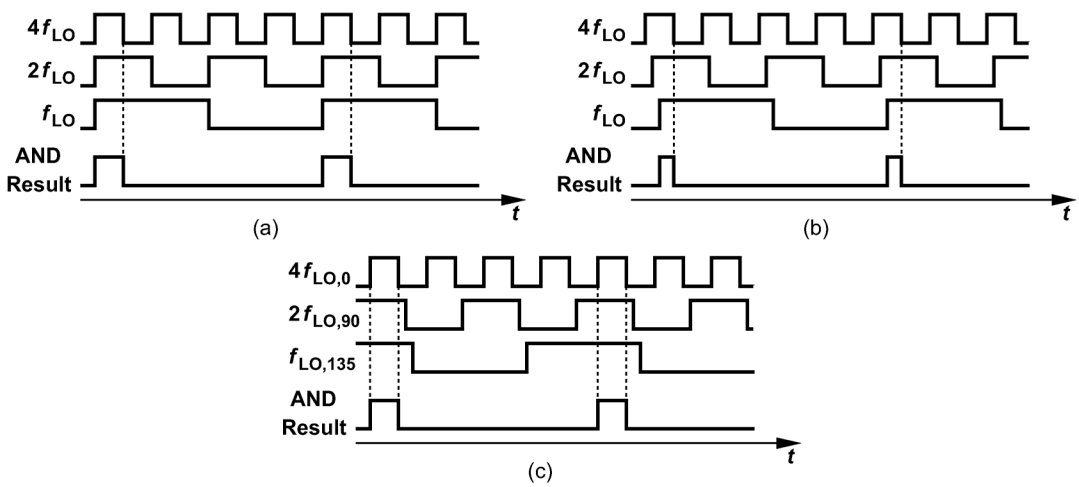


Fig. 20. (a) 12.5% duty cycle clock generation by ANDing $f_{\rm LO}$, $2f_{\rm LO}$, and $4f_{\rm LO}$, (b) reduced duty cycle due to delay of dividers, and (c) proper choice of phases to avoid duty cycle error.

A 12.5% duty cycle at $f_{\rm LO}$ can be created by ANDing three 50% duty cycle waveforms at $4f_{\rm LO}$, $2f_{\rm LO}$, and $f_{\rm LO}$ [Fig. 20(a)]. However, the divider-induced delays between $4f_{\rm LO}$ and $2f_{\rm LO}$ and between $2f_{\rm LO}$ and $f_{\rm LO}$ reduce the duty cycle [Fig. 20(b)]. We must therefore seek an arrangement whereby the pulses at $f_{\rm LO}$ and $2f_{\rm LO}$ *enclose* those at $2f_{\rm LO}$ and $f_{\rm LO}$, respectively, allowing sufficient margin for the delays. Fig. 20(c) shows an example employing $2f_{\rm LO,90}$ and $f_{\rm LO,135}$, suggesting a robust solution if these phases are available.

Depicted in Fig. 21, the phase generation module consists of two sections: (1) a divider circuit producing eight phases with 50% duty cycle, and (2) a combining circuit converting these signals to phases with 12.5% duty cycle. As shown in Fig. 21(a), the former employs a flipflop-based $\div 2$ stage to generate quadrature phases at $2f_{\rm LO}$ and a ring divider comprising four latches to create eight phases at $f_{\rm LO}$. This section draws 4.3 mW at 2 GHz.

Shown in Fig. 21(b), each instance of the combining circuit performs an AND function on three signals as described in Fig. 21(c). We recognize that four of the NAND gates are driven by $4f_{\rm LO,0}$, and hence can share their corresponding transistors in the stack [Fig. 21(c)]. Similarly, another gate driven by $2f_{\rm LO,90}$ shares its internal node with the first gate. Since only one gate performs complete pull down in a given phase, this sharing augments the pull-down strength and sharpens the edge. The combining circuit consumes a total of 2.76 mW at 2 GHz.

According to simulations, the overall phase generation circuit exhibits a phase noise of -163.5 dBc/Hz at 3 MHz offset and -165.7 dBc/Hz at 20 MHz offset. The latter negligibly affects the performance because the mixer switches process only heavily attenuated blockers. Note that the frequency divider output noise is removed by the gating effect of the $4f_{\rm LO}$ inputs in Fig. 21(b).

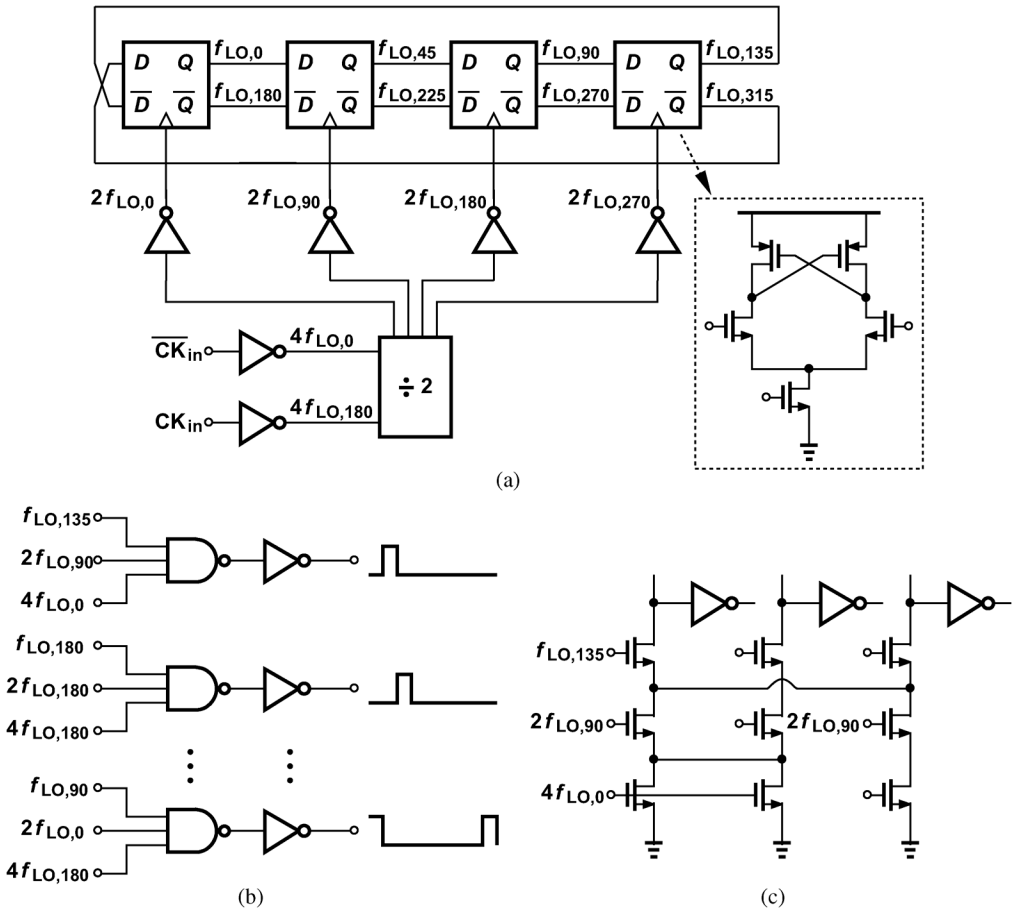


Fig. 21. (a) 50% duty cycle phase generation, (b) phase combination for 12.5% duty cycle, and (c) drain node sharing for the same clock.

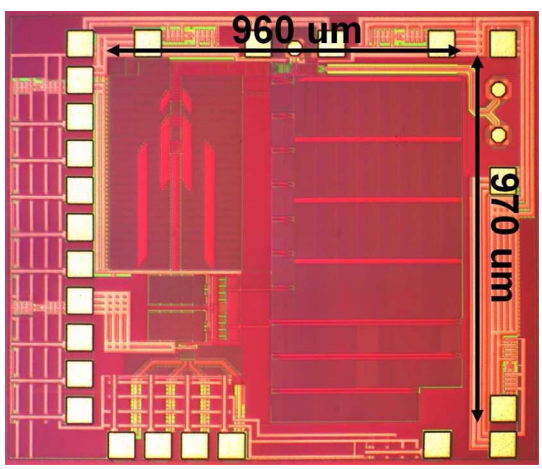


Fig. 22. Receiver die photograph.

V. Experimental Results

The proposed GSM/WCDMA receiver with RF channel selection has been fabricated in TSMC's 65 nm CMOS technology. Shown in Fig. 22, the die occupies an active area of about 0.82 mm^2. With a 1.2 V supply, the LNA draws 10.1 mW, the Miller amplifiers 1.7 mW, the baseband amplifiers 1.1 mW, and the LO phase generation circuit 7.1 mW. The capacitors in all three banks are programmable through an on-chip serial bus so as to support GSM, WCDMA, and IEEE 802.11b/g.

In this design, the following switch dimensions have been used: 28 μm/60 nm in Bank 1, 7 μm/60 nm in Bank 2, and 0.96 μm/60 nm in Bank 3. The respective on-resistances are 15 Ω, 60 Ω, and 440 Ω. All capacitors are realized as metal fringe structures (with ample linearity).

Fig. 23(a) plots the measured RF-to-baseband gain as a function of baseband frequency for the three standards. The responses are measured with f_{LO} set to 1 GHz, 2 GHz, and 2.5 GHz. The one-sided -3 dB bandwidth is set to 175 kHz,[5] 2 MHz, and 10 MHz, respectively. The rejection in the alternate adjacent channel reaches at least 16 dB for all three standards. The roll-off behavior of the GSM response is explained as follows: from 175 kHz, the unilateral Miller notch filter drops the gain, providing around 24 dB of rejection. At 3 MHz, Bank 1 and Bank 2 take over, creating the second roll-off and a rejection of 50 dB at 20 MHz. For WCDMA and 802.11b/g, on the other hand, only Bank 1 and Bank 2 are necessary.

Fig. 23(b) presents the measured noise figure as a function of baseband frequency for GSM and WCDMA. The NF is about 2.9 dB beyond 100 kHz. Determined by the noise of the external

[5]In the prototype, the minimum one-sided bandwidth does not reach the desired value of 100 kHz. This is attributed to lower-than-expected capacitance density.

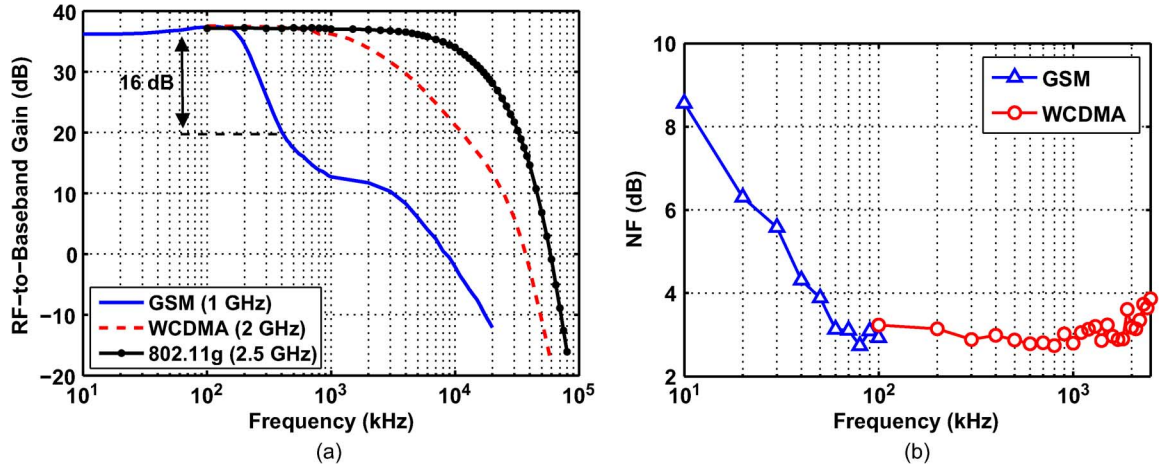


Fig. 23. (a) Measured RF-to-baseband gain for GSM, WCDMA, and 802.11g, and (b) measured NF vs. baseband frequency for GSM and WCDMA.

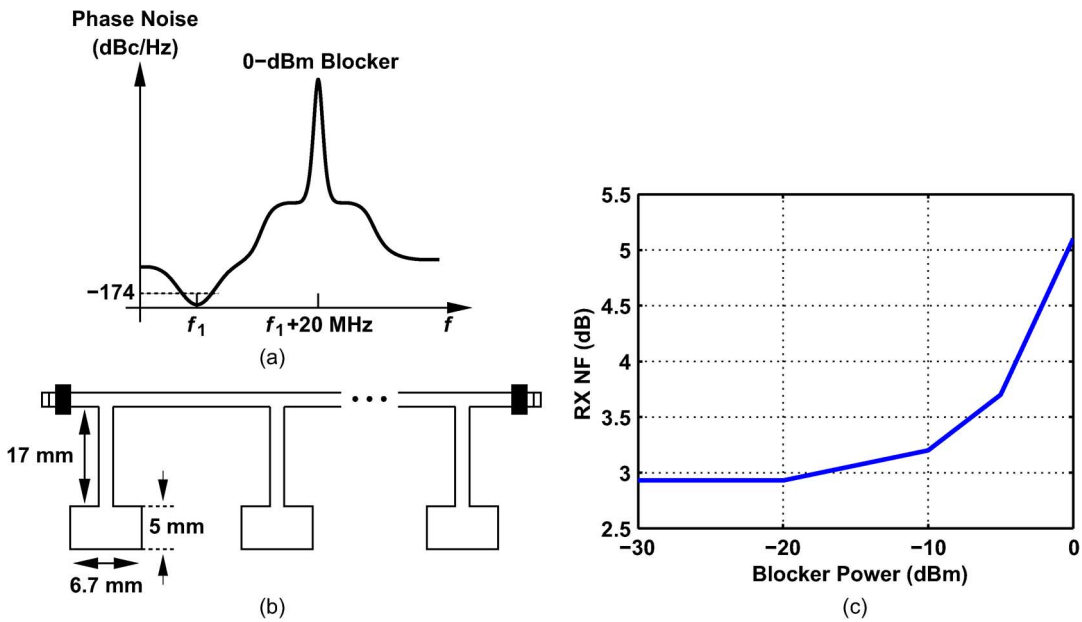


Fig. 24. (a) RF generator phase noise profile with microstrip-line LC filter, (b) microstrip-line filter implementation, and (c) measured NF as a function of blocker power level.

LO, the average NF for GSM is 4.8 dB, calculated by adding the numerical (linear) values of NF at 10 kHz, 20 kHz, . . ., 100 kHz and dividing the result by 10. (The simulated value with a noiseless LO is 2.62 dB.) The NF is measured with harmonic rejection turned on. The measured harmonic rejection for the third and the fifth harmonics is -37 dB and -45 dB, respectively, when $f_{\rm LO} = 2.5$ GHz.

Measurement of the NF with a 0 dBm blocker proves challenging as typical RF generators exhibit a noise floor of around -167 dBc/Hz at 20 MHz offset, contributing substantial noise to the receiver. As shown in Fig. 24(a), the generator's noise at the desired carrier frequency, f_1, must be reduced by means of a highly selective filter. To this end, we have designed a printed-circuit notch filter based on a microstrip loaded by six LC traps that are separated by $\lambda/4$ [Fig. 24(b)]. The LC traps consist of a 160-mm-long microstrip and six 6.7 mm $\times$ 5 mm capacitive pads. This filter rejects the noise at f_1 by 13 dB. Fig. 24(c) shows the measured NF as a function of the blocker power level at 20 MHz offset. The NF is relatively constant up to -20 dBm and rises to 5.1 dB at 0 dBm.

Fig. 25 plots the magnitude of the input return loss for GSM and WCDMA, indicating moderate input matching in both cases. Fig. 26 shows the measured $\rm IIP_3$ and $\rm IIP_2$ for GSM and WCDMA versus the offset frequency, $f_{\rm OS}$. The two input tones are located at $f_{\rm LO} + mf_{\rm OS} + \Delta f$ and $f_{\rm LO} + nf_{\rm OS} + \Delta f$, where $m = 1$, $n = 2$, $\Delta f = 100$ kHz for GSM $\rm IIP_3$, and $m = 1$, $n = 2$, $\Delta f = 1$ MHz for WCDMA $\rm IIP_3$. For $\rm IIP_2$ measurement, the two input tones are located at $f_{\rm LO} + f_{\rm OS}$ and $f_{\rm LO} + f_{\rm OS} + \Delta f$, $\Delta f = 100$ kHz for GSM $\rm IIP_2$, and $\Delta f = 1$ MHz for WCDMA $\rm IIP_2$.

Table II summarizes the performance of our receiver and several other recent designs. The LO leakage to the antenna depends on the mismatches between the paths and is measured to

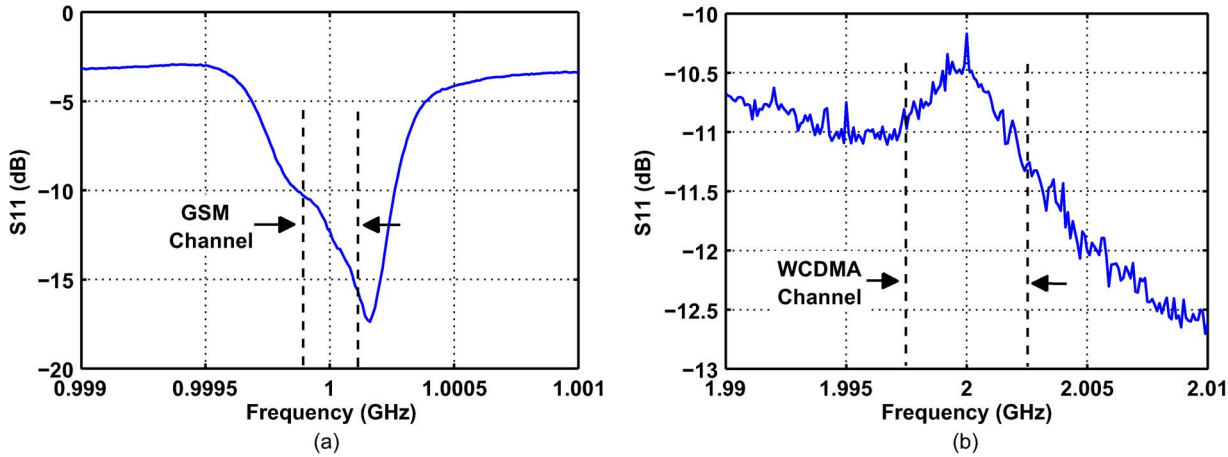


Fig. 25. (a) Measured S_{11} for GSM. (b) Measured S_{11} for WCDMA.

TABLE II
RECEIVER PERFORMANCE SUMMARY AND COMPARISON

	Murphy ISSCC 2012	Youssef ISSCC 2012	Fabiano ISSCC 2013	This work
Input Frequency [MHz]	80 ~ 2700	1000 ~ 2500	1800 ~ 2400	50 ~ 2500
Channel Bandwidth [MHz]	N/A	5	N/A	0.35 ~ 20
Gain [dB]	72	30	45.5	38
NF [dB]	1.9	7.6	3.8	2.9
NF with 0-dBm Blocker [dB] (at Given Offset)	4.1 (80 MHz)	N/A	7.9 (20 MHz)	5.1 (20 MHz)
Out-of-Band-IIP3 [dBm]	13.5	12	18	10
LO Leakage to Antenna [dBm] @ 2 GHz	−65	N/A	N/A	−67
Active Area [mm^2]	1.2	< 0.06	0.84	0.82
Supply Voltage [V]	1.3	1.2	1.2/1.8	1.2
Power Consumption [mW]	65 (2 GHz)	62[1]	35[2] (2 GHz)	20 (2 GHz)
CMOS Technology	40 nm	65 nm	40 nm	65 nm

[1] Excluding clock circuitry [2] with a 1.8 V supply for LO divider.

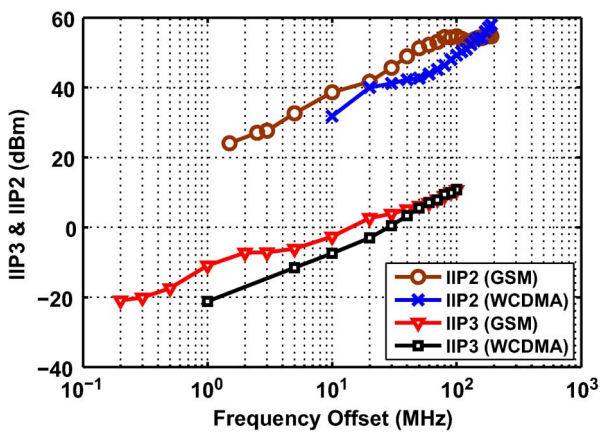


Fig. 26. Measured IIP_3 and IIP_2 for GSM and WCDMA.

be −67 dBm when $f_{\mathrm{LO}} = 2$ GHz without any mismatch correction. With a two-sided filter bandwidth programmable from 350 kHz to 20 MHz, our receiver exhibits a noise figure of 5.1 dB in the presence of a 0 dBm blocker while dissipating 20 mW.

VI. CONCLUSION

RF channel selection can greatly relax the linearity and phase noise requirements of receivers if it sufficiently suppresses large blockers. This paper has introduced the Miller bandpass filter and its variants along with a polyphase compensation technique that select the desired channel at the LNA input. A low-power 12.5% duty cycle phase generator is also described. With the wide bandwidth available in the LNA, the receiver can be readily extended to the 5 GHz range as well. Harmonic-rejection mixing is utilized to reduce the downconverted noise, but the receiver can also exploit prior techniques to achieve high rejection of blockers at the LO harmonics.

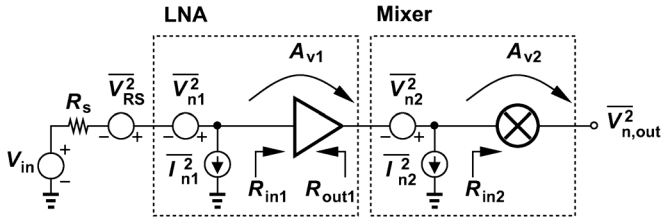


Fig. 27. Noise model for broadband RF receiver.

APPENDIX I

In this Appendix, we derive an expression for the NF of a receiver that downconverts broadband white noise. For simplicity, we consider a single mixer driven by a 50%-duty-cycle LO. It can be proved [18] that the combined 12.5%-duty-cycle LOs (in the harmonic-rejection circuitry) are equivalent to a 50%-duty-cycle waveform for this analysis. Downconverting uncorrelated noise at all odd LO harmonics, such a mixer exhibits a double-sided NF of $\pi^2/8$ (rather than 1). We now refer to the RX cascade shown in Fig. 27, where the LNA and the mixer noise is modeled by input-referred sources and A_{v1} and A_{v2} denote unloaded voltage gains. We write the total noise power at the LNA input as

$$\overline{V_{n,in1}^2} = \overline{\left[I_{n1}(R_S \parallel R_{\rm in1}) + V_{n1}\frac{R_{\rm in1}}{R_{\rm in1}+R_S}\right]^2} + \overline{V_{RS}^2}\left(\frac{R_{\rm in1}}{R_{\rm in1}+R_S}\right)^2. \quad (11)$$

The total noise power at the mixer input is thus given by

$$\overline{V_{n,in2}^2} = \overline{\left[I_{n2}(R_{\rm out1} \parallel R_{\rm in2}) + V_{n2}\frac{R_{\rm in2}}{R_{\rm in2}+R_{\rm out1}}\right]^2} + \overline{V_{n,in1}^2}A_{v1}^2\left(\frac{R_{\rm in2}}{R_{\rm in2}+R_{\rm out1}}\right)^2. \quad (12)$$

Note that the mixer's input noise sources already include folding effects within the mixer. Upon downconversion, the LNA noise experiences a factor of $\pi^2/8$ due to folding:

$$\overline{V_{n,out}^2} = A_{v2}^2\overline{\left[I_{n2}(R_{\rm out1} \parallel R_{\rm in2}) + V_{n2}\frac{R_{\rm in2}}{R_{\rm in2}+R_{\rm out1}}\right]^2} + \frac{\pi^2}{8}\overline{V_{n,in1}^2}A_{v1}^2A_{v2}^2\left(\frac{R_{\rm in2}}{R_{\rm in2}+R_{\rm out1}}\right)^2. \quad (13)$$

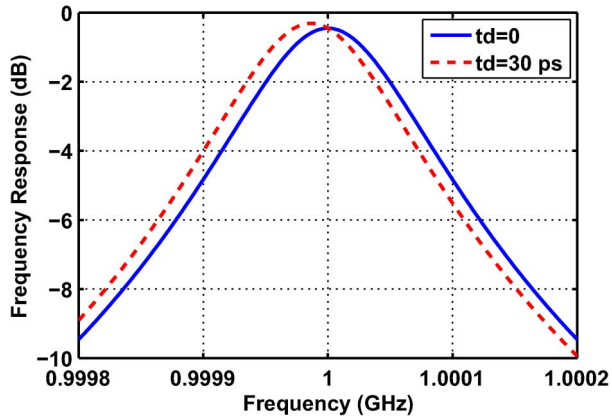


Fig. 28. f_c shift with and without 30 ps delay.

It follows that

$$NF_{tot} = \frac{\pi^2}{8}\frac{4kTR_S + \overline{(I_{n1}R_S + V_{n1})^2}}{4kTR_S} + \frac{\overline{(I_{n2}R_{\rm out1} + V_{n2})^2}}{A_{v1}^2\left(\frac{R_{\rm in1}}{R_{\rm in1}+R_S}\right)4kTR_S}. \quad (14)$$

If driven by a source impedance of $R_{\rm out1}$, the mixer exhibits a noise figure equal to

$$NF_{2,Rout1} = \frac{\frac{\pi^2}{8}4kTR_{\rm out1} + \overline{(I_{n2}R_{\rm out1} + V_{n2})^2}}{4kTR_{\rm out1}}. \quad (15)$$

Substitution in (13) thus yields

$$NF_{tot} = \frac{\pi^2}{8}\cdot NF_1 + \frac{\left(NF_{2,Rout1} - \frac{\pi^2}{8}\right)}{A_v^2}\cdot\frac{R_{\rm out1}}{R_S}, \quad (16)$$

where $A_v^2 = A_{v1}^2(R_{\rm in1}/(R_S+R_{\rm in1}))^2$.

APPENDIX II

In this Appendix, we analyze the effect of the amplifier delay, t_d, on the Miller bandpass filter, neglecting the switch on-resistances for simplicity. Returning to Fig. 4(e), we simply replace A_0 with $A_0e^{-jt_d\omega}$. Equation (3) thus reduces to (17), shown at the bottom of the page.

We examine the magnitude of the denominator, $|D|$, as ω departs from $\omega_{\rm LO}$. We have $|D|^2 = 1+\tau^2(1+A_0^2)(\omega-\omega_{\rm LO})^2+2\tau A_0(\omega-\omega_{\rm LO})\sin\omega t_d + 2\tau^2A_0(\omega-\omega_{\rm LO})\cos\omega t_d$, where $\tau = 8R_SC_F$. Since $A_0^2 \gg 1$ and $1+A_0^2 \gg 2A_0\cos\omega t_d$, we have $|D|^2 \approx 1+\tau^2A_0^2(\omega-\omega_{\rm LO})^2+2\tau A_0(\omega-\omega_{\rm LO})\sin\omega t_d$.

$$\frac{V_{RF}}{I_{\rm in}}(\omega) = \frac{\frac{16}{\pi^2}(2-\sqrt{2})R_S}{1+j8R_S(1+A_0e^{-jt_d\omega})C_F(\omega-\omega_{\rm LO})} = \frac{\frac{16}{\pi^2}(2-\sqrt{2})R_S}{1+8A_0R_SC_F(\omega-\omega_{\rm LO})\sin\omega t_d + j8R_SC_F(\omega-\omega_{\rm LO})(1+A_0\cos\omega t_d)}. \quad (17)$$

Setting $d|D|^2/d\omega$ to zero, we obtain $\tau A_0(\omega-\omega_{\rm LO})+\sin\omega t_d+t_d(\omega-\omega_{\rm LO})\cos\omega t_d=0$. The third term is negligible with respect to the first, yielding $\omega-\omega_{\rm LO}\cong-\sin\omega t_d/(\tau A_0)$. Since the offset from LO is small, $\sin\omega t_d\approx\sin\omega_{\rm LO}t_d$ and

$$\omega-\omega_{\rm LO}\approx\frac{-\sin\omega_{\rm LO}t_d}{\tau A_0}. \tag{18}$$

The peak thus shifts by this amount. For example, if $f_{\rm LO}=1$ GHz, $t_d=30$ ps, $\tau=8R_SC_F=8\times50\ \Omega\times250$ pF $=100$ ns, and $A_0=20$, then $|\omega-\omega_{\rm LO}|=2\pi$ (15 kHz). Fig. 28 plots the magnitude of (17) with these values, confirming the above result.

ACKNOWLEDGMENT

The authors would like to thank the TSMC University Shuttle Program for chip fabrication.

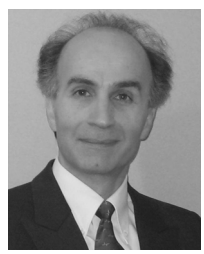
REFERENCES

[1] A. Mirzaei *et al.*, "A frequency translation technique for SAW-less 3G receivers," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2009, pp. 280–281.
[2] J. Borremans *et al.*, "A 40 nm CMOS highly linear 0.4-to-6 GHz receiver resilient to 0 dBm out-of-band blockers," in *IEEE ISSCC Dig. Tech. Papers*, 2011, pp. 62–63.
[3] D. Murphy *et al.*, "A blocker-tolerant, noise-canceling receiver suitable for wideband wireless applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, Dec. 2012.
[4] M. Darvishi *et al.*, "A 0.1-to-1.2 GHz tunable 6th-order N-path channel-select filter with 0.6 dB passband ripple and +7 dBm blocker tolerance," in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 172–173.
[5] B. Cook *et al.*, "Low-power 2.4 GHz transceiver with passive RX front-end and 400-mV supply," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2757–2766, Dec. 2006.
[6] A. Ghaffari *et al.*, "Tunable high-Q N-path band-pass filters: Modeling and verification," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, May 2011.
[7] A. Mirzaei *et al.*, "Architectural evolution of integrated M-phase high-Q bandpass filters," *IEEE Trans. Circuits Syst. I*, vol. 59, no. 1, pp. 52–65, Jan. 2012.
[8] H. Busignies and M. Dishal, "Some relations between speed of indication, bandwidth, and signal-to-random-noise ratio in radio navigation and direction finding," *Proc. IRE*, pp. 478–488, May 1949.
[9] W. R. LePage *et al.*, "Analysis of a comb filter using synchronously commutated capacitors," *Amer. Inst. Electr. Eng., Part I: Trans. Commun. Electron.*, pp. 63–68, Mar. 1953.
[10] B. D. Smith, "Analysis of commutated Networks," *IRE Trans., Professional Group on Aeronautical and Navigational Electronics*, pp. 21–26, Dec. 1953.
[11] M. A. Poole, "High Q notch filter," U.S. Patent 3,795,877, Mar. 5, 1974.
[12] A. Ghaffari *et al.*, "Tunable N-path notch filters for blocker suppression: Modeling and verification," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1370–1382, Jun. 2013.
[13] A. Mirzaei *et al.*, "A 65 nm CMOS quad-band SAW-less receiver SoC for GSM/GPRS/EDGE," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 950–964, Apr. 2011.
[14] S. Youssef *et al.*, "Active feedback technique for RF channel selection in front-end receivers," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3130–3144, Dec. 2012.
[15] L. E. Franks and L. W. Sandburg, "An alternative approach to the realization of network transfer functions: The N-path filter," *Bell Syst. Tech. J.*, vol. 39, pp. 1321–1350, Sep. 1960.
[16] B. Razavi, "Cognitive radio design challenges and techniques," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1542–1553, Aug. 2010.
[17] J. W. Park and B. Razavi, "A harmonic-rejecting CMOS LNA for broadband radios," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1072–1084, Apr. 2013.
[18] J. A. Weldon *et al.*, "A 1.75 GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2003–2015, Dec. 2001.
[19] Z. Ru *et al.*, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3359–3375, Dec. 2009.
[20] A. Mirzaei *et al.*, "A low-power process-scalable super-heterodyne receiver with integrated high-Q filters," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2920–2932, Dec. 2011.
[21] C. Andrews and A. C. Molnar, "A passive-mixer-first receiver with baseband-controlled RF impedance matching, $\ll$ 6 dB NF, and $\gg$ 27 dBm wideband IIP3," in *IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 46–47.
[22] I. Fabiano *et al.*, "SAW-less analog front-end receivers for TDD and FDD," in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 82–83.

Joung Won Park (S'10–M'13) received the B.S.E.E. degree from Seoul National University, Seoul, Korea, in 2002 and the M.S.E.E. degree from Texas A&M University, College Station, TX, USA, in 2009 and the Ph.D.E.E. degree from the University of California, Los Angeles, CA, USA, in 2013.

Since 2014, he has been Senior Engineer of Corporate R&D at Qualcomm, San Diego, CA, USA. His current research interest is in RF/analog circuit design for wireless communication systems. In fall 2008, he interned at Qualcomm, San Diego, where he was involved in RF front-end design for W/CDMA and LTE cellular systems.

Dr. Park received the Outstanding Student Design Award from Analog Devices Inc. in 2010.



Behzad Razavi (M'90–SM'00–F'03) received the B.S.E.E. degree from Sharif University of Technology, Tehran, Iran, in 1985 and the MS.E.E. and Ph.D.E.E. degrees from Stanford University, Stanford, CA, USA, in 1988 and 1992, respectively.

He was with AT&T Bell Laboratories and Hewlett-Packard Laboratories until 1996. Since 1996, he has been Associate Professor and subsequently Professor of electrical engineering at the University of California, Los Angeles, CA, USA. His current research includes wireless transceivers, frequency synthesizers, phase-locking and clock recovery for high-speed data communications, and data converters.

Prof. Razavi was an Adjunct Professor at Princeton University from 1992 to 1994, and at Stanford University in 1995. He served on the Technical Program Committees of the International Solid-State Circuits Conference (ISSCC) from 1993 to 2002 and VLSI Circuits Symposium from 1998 to 2002. He has also served as Guest Editor and Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, and the *International Journal of High Speed Electronics*.

Prof. Razavi received the Beatrice Winner Award for Editorial Excellence at the 1994 ISSCC, the Best Paper Award at the 1994 European Solid-State Circuits Conference, the Best Panel Award at the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, the best paper award at the IEEE Custom Integrated Circuits Conference in 1998, and the McGraw-Hill First Edition of the Year Award in 2001. He was the co-recipient of both the Jack Kilby Outstanding Student Paper Award and the Beatrice Winner Award for Editorial Excellence at the 2001 ISSCC. He received the Lockheed Martin Excellence in Teaching Award in 2006, the UCLA Faculty Senate Teaching Award in 2007, and the CICC Best Invited Paper Award in 2009 and in 2012. He was the co-recipient of the 2012 VLSI Circuits Symposium Best Student Paper Award and the 2013 CICC Best Paper Award. He was also recognized as one of the top 10 authors in the 50-year history of ISSCC. He received the 2012 Donald Pederson Award in Solid-State Circuits. He was also the recipient of the American Society for Engineering Education PSW Teaching Award in 2014.

Prof. Razavi has served as an IEEE Distinguished Lecturer and is a Fellow of IEEE. He is the author of *Principles of Data Conversion System Design* (IEEE Press, 1995), *RF Microelectronics* (Prentice Hall, 1998, 2012) (translated to Chinese, Japanese, and Korean), *Design of Analog CMOS Integrated Circuits* (McGraw-Hill, 2001) (translated to Chinese, Japanese, and Korean), *Design of Integrated Circuits for Optical Communications* (McGraw-Hill, 2003, Wiley, 2012), and *Fundamentals of Microelectronics* (Wiley, 2006) (translated to Korean and Portuguese), and the editor of *Monolithic Phase-Locked Loops and Clock Recovery Circuits* (IEEE Press, 1996), and *Phase-Locking in High-Performance Systems* (IEEE Press, 2003).