A 40-GHz Frequency Divider in 0.18-μm CMOS Technology

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***Abstract*—An analysis of regenerative dividers predicts the required phase shift or selectivity for proper operation. A divider topology is introduced that employs resonance techniques by means of on-chip spiral inductors to tune out the device capacitances. Configured as two cascaded ÷2 stages, the circuit achieves a frequency range of 2.3 GHz at 40 GHz while consuming 31 mW from a 2.5-V supply.**

***Index Terms*—Frequency dividers, Gilbert cell, inductive peaking, Miller divider, regenerative dividers, RF mixers.**

I. Introduction

HIGH-SPEED frequency dividers play a critical role in various broadband and wireless applications. Static CMOS frequency dividers operating at 27 GHz [1] and 33 GHz [2] have been realized in 0.12-μm technology, but future 40-Gb/s broadband transceivers and 60-GHz RF systems demand frequency division at higher rates.

This paper offers new perspectives on the operation of dynamic (Miller) dividers, providing startup conditions and exploiting the results to arrive at a high-speed topology. Configured as two cascaded ÷2 stages, the circuit operates at an input frequency of 40 GHz with an input range of 2.3 GHz while consuming 31 mW from a 2.5-V supply.

Section II of this paper presents an analysis of the Miller divider and develops the foundation for the proposed topology. Section III introduces the divider circuit and quantifies its performance limitations. Section IV describes the design of the building blocks and Section V gives the experimental results.

II. Analysis of Miller Divider

Originally proposed by Miller in 1939 [3], the dynamic divider is based on mixing the output with the input and applying the result to a low-pass filter (LPF), as shown in Fig. 1(a). Under proper phase and gain conditions, the component at $\omega_{\rm in}/2$ survives and circulates around the loop. Since the device capacitances are absorbed in the low-pass filter, this topology achieves a high speed and is widely adopted in the design of bipolar and GaAs dividers.

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A. Phase Shift and Selectivity Requirements

While providing an intuitive understanding of the circuit's operation, Fig. 1(a) fails to stipulate the conditions for proper division. For example, the low-pass filter may be realized as a first-order *RC* network [Fig. 1(b)], a reasonable model of the load seen at the output node of typical mixers. Neglecting nonlinearities in the mixer, we have

$$R_1C_1\frac{dy}{dt}+y=\beta yA\cos\omega_{\rm in}t \tag{1}$$

where β denotes the mixer conversion factor. Thus

$$R_1C_1\frac{dy}{dt}=y(\beta A\cos\omega_{\rm in}t-1) \tag{2}$$

and hence

$$y(t)=y(0)\exp\left(-\frac{t}{R_1C_1}+\frac{\beta A}{R_1C_1\omega_{\rm in}}\sin\omega_{\rm in}t\right). \tag{3}$$

Interestingly, $y(t)$ decays to zero with a time constant of R_1C_1, i.e., the circuit fails to divide regardless of the value of $\omega_{\rm in}$ with respect to the LPF corner frequency, $(R_1C_1)^{-1}$. In other words, $\omega_{\rm in}/2$ is not regenerated even though R_1C_1 is chosen to attenuate the third harmonic, $3\omega_{\rm in}/2$ (and even if a noise current at $\omega_{\rm in}/2$ is injected into the loop).

Let us now consider an extreme case where all time constants in the loop are negligible, all waveforms are rectangular, and the circuit operates correctly. As illustrated in Fig. 2(a), the mixer output resembles $y(t)$ but shifted by a quarter period, suggesting that inserting a broadband delay $\Delta T=\pi/\omega_{\rm in}$ in the loop permits correct division [Fig. 2(b)].

It is important to note that the *RC* network of Fig. 1(b) does not satisfy the conditions required in Fig. 2(b). For example, the network cannot provide a phase shift of 90° at $\omega_{\rm in}/2$ and 270° at $3\omega_{\rm in}/2$. Furthermore, it attenuates the third harmonic considerably, failing to generate the idealized waveforms shown in Fig. 2(a).

We now study another extreme case where the loop exhibits no delay at $\omega_{\rm in}/2$ but enough selectivity to attenuate the third harmonic. Fig. 3(a) exemplifies this case, with the mixer injecting a current into the parallel tank and $\sqrt{LC}=2/\omega_{\rm in}$. We assume that the peaks of $x_1(t)$ and $x_2(t)$ are aligned and examine $x_1(t)x_2(t)$ and $y(t)$. As depicted in Fig. 3(b), the product waveform displays multiple zero crossings in each period due to the third harmonic, revealing that such a loop fails to divide if this harmonic is not suppressed sufficiently, i.e., if $y(t)$ does not monotonically rise and fall. Fig. 3(c) illustrates the resulting waveforms for different values of the attenuation factor, α, experienced by the third harmonic with respect to the fundamental. To eliminate the extraneous zero crossings, we require that the

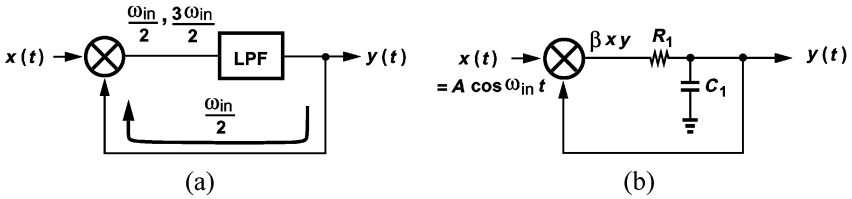

Fig. 1. Dynamic (Miller) divider. (a) Generic topology. (b) Realized with an *RC* filter.

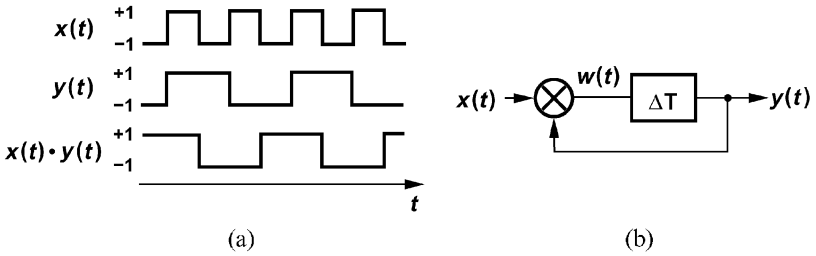

Fig. 2. 90° phase shift operation. (a) Waveforms. (b) Model.

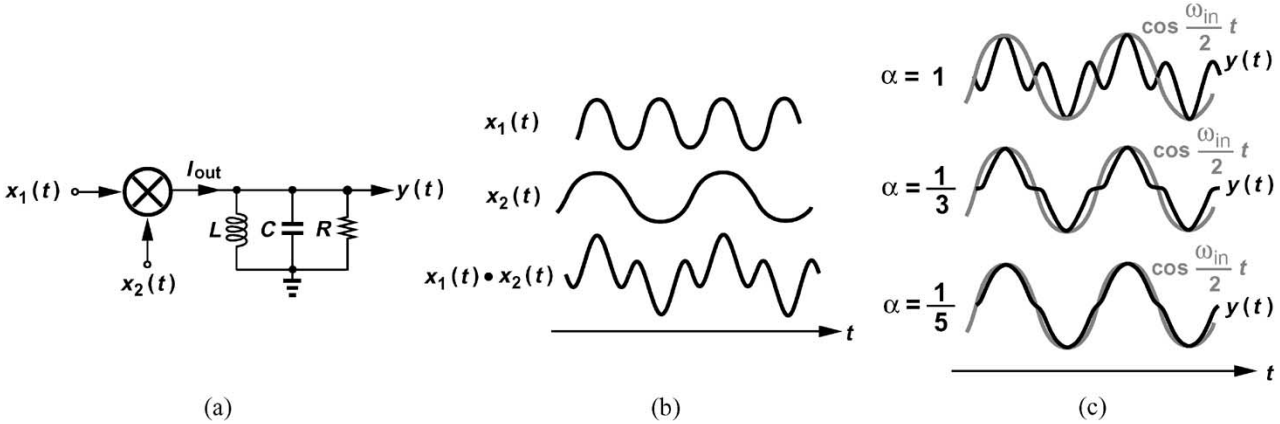

Fig. 3. (a) Mixer with selective network. (b) Input waveforms and (c) output waveforms for different values of α.

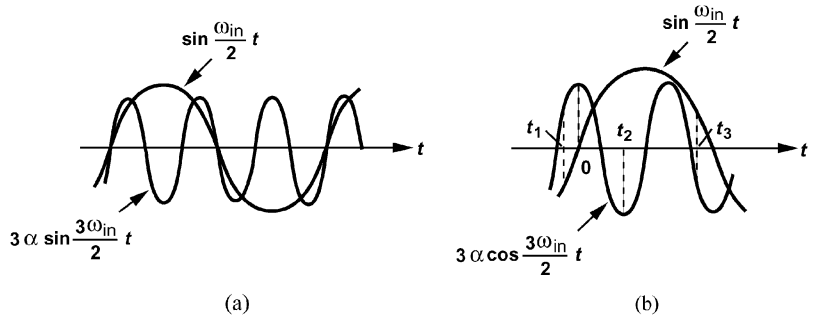

Fig. 4. Components of the slopes of output waveforms. (a) Simplified case. (b) Actual case.

slope of $y(t)$ not change sign between a positive peak and the next negative peak. Since

$$y(t) \propto \cos\frac{\omega_{\rm in}t}{2} + \alpha\cos\frac{3\omega_{\rm in}t}{2} \tag{4}$$

we have

$$\frac{dy}{dt} \propto -\sin\frac{\omega_{\rm in}t}{2} - 3\alpha\sin\frac{3\omega_{\rm in}t}{2} < 0 \quad \text{for } 0 < t < \frac{2\pi}{\omega_{\rm in}}. \tag{5}$$

Illustrated in Fig. 4(a), the terms $\sin(\omega_{\rm in}t/2)$ and $3\alpha\sin(3\omega_{\rm in}t/2)$ yield a positive sum if $0 < 3\alpha < 1$. Thus, the attenuation factor must satisfy

$$0 < \alpha < \frac{1}{3}. \tag{6}$$

The foregoing derivation assumes the third harmonic experiences no phase shift, contradicting the actual behavior of the

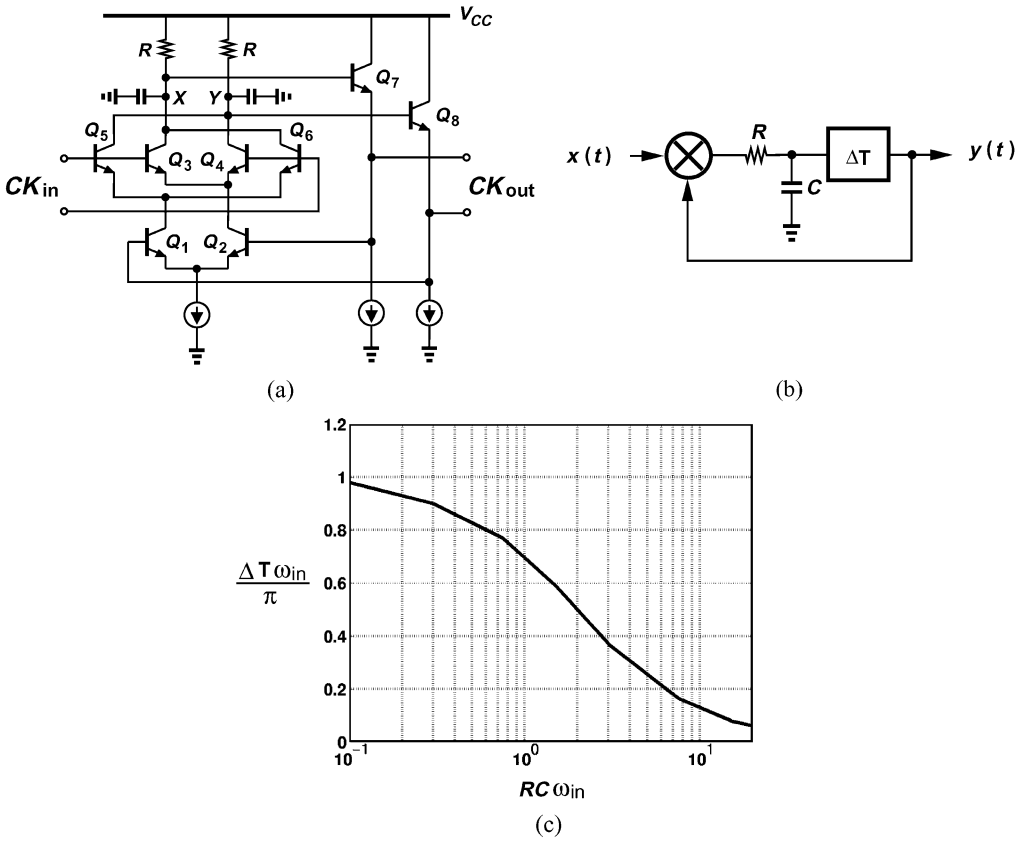

Fig. 5. (a) Bipolar Miller divider. (b) Simplified model. (c) Requisite delay as a function of *RC*.

RLC tank. Since the tank impresses a phase shift of approximately 90° upon this harmonic, (4) must be rewritten as

$$y(t) \approx \cos\frac{\omega_{\text{in}}t}{2} + \alpha \sin\frac{3\omega_{\text{in}}t}{2} \tag{7}$$

and dy/dt must remain negative in a proper interval. Plotting the two components of dy/dt in Fig. 4(b), we note that a positive sum results between t_1 and t_3 if $\sin(\omega_{\text{in}}t_2/2) - 3\alpha\cos(3\omega_{\text{in}}t_2/2) > 0$. Since the phase $\omega_{\text{in}}t/2$ reaches 60° at t_2, we have

$$0 < \alpha < \frac{1}{2\sqrt{3}} \tag{8}$$

which is a slightly more stringent condition than that in (6).

We now determine the selectivity required of the tank to guarantee (8):

$$\frac{L^2\omega^2}{R^2(1-LC\omega^2)^2 + L^2\omega^2} = \left(\frac{1}{2\sqrt{3}}\right)^2 \tag{9}$$

where $LC = (\omega_{\text{in}}/2)^{-2}$ and $\omega = 3\omega_{\text{in}}/2$. It follows that

$$\frac{R}{L\dfrac{\omega_{\text{in}}}{2}} = \frac{3\sqrt{11}}{8} \approx 1.24. \tag{10}$$

In other words, a tank Q of 1.24 at $\omega_{\text{in}}/2$ ensures enough attenuation of the third harmonic. Of course, it is assumed that the loop gain at $\omega_{\text{in}}/2$ is sufficient to sustain this component. As explained in Section III, the loop gain requirement may translate to a Q higher than the above value.

In summary, proper operation of the Miller divider requires either sufficient broadband phase shift around the loop or enough suppression of the third harmonic (or a combination of both). Typical bipolar implementations fall in the former category and the divider proposed here falls in the latter. Specifically, the commonly used bipolar realization shown in Fig. 5(a) introduces delay at nodes X and Y, through the emitter followers, and at the collectors of Q_1 and Q_2[1] while attenuating the third harmonic to some extent. Simplifying the circuit to the idealized model in Fig. 5(b), we use simulations to plot the requisite delay as a function of RC [Fig. 5(c)], arriving at the solution space (on or above the line) for the choice of these two parameters.

III. Divider With Bandpass Load

The topology of Fig. 5(b) is difficult to realize in CMOS for the following reasons: 1) with the low transconductance of MOS devices, the voltage drop across the load resistors must be large so as to provide enough loop gain; 2) source followers consume substantial voltage headroom and attenuate the signal; and 3) the limited bandwidth of the source followers prevents the divider from high-speed operation. Fortunately, these issues can be resolved by employing an *LC* tank as the load in the Miller divider, as shown in Fig. 6. For this circuit to divide properly, the loop gain at $\omega_{\text{in}}/2$ must be at least unity. Modeling the mixer as

[1]The base resistance of $Q_7 - Q_8$ and $Q_1 - Q_2$ along with their base–collector and base–emitter capacitances also contribute some phase shift.

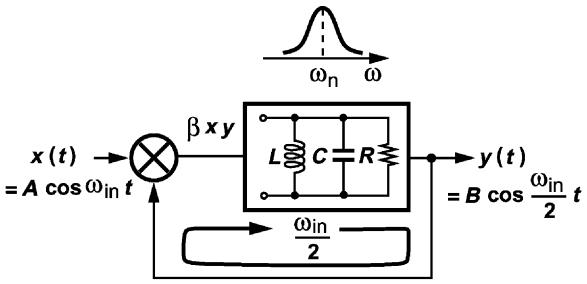

Fig. 6. Miller divider with bandpass filter.

an ideal multiplier and assuming the following transfer function for the *RLC* tank:

$$H(s) = \frac{2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{11}$$

where $2\zeta\omega_n = (RC)^{-1}$ and $\omega_n^2 = (LC)^{-1}$, we require that

$$\frac{\beta A}{2}\left|H\left(j\frac{\omega_{\text{in}}}{2}\right)\right| \geq 1. \tag{12}$$

(The factor 1/2 arises from the product-to-sum conversion of sinusoids after multiplication.) That is,

$$\frac{\beta A}{2}\left|\frac{2\zeta\omega_n\frac{\omega_{\text{in}}}{2}}{\sqrt{\left(\omega_n^2 - \frac{\omega_{\text{in}}^2}{4}\right)^2 + 4\zeta^2\omega_n^2\frac{\omega_{\text{in}}^2}{4}}}\right| \geq 1. \tag{13}$$

Thus, the minimum input amplitude necessary for correct division is given by

$$A \geq \frac{2}{\beta}\sqrt{1 + \frac{\left(1 - \frac{\omega_{\text{in}}^2}{4\omega_n^2}\right)^2}{\zeta^2\frac{\omega_{\text{in}}^2}{\omega_n^2}}}. \tag{14}$$

As expected, the right-hand side falls to a minimum of $2/\beta$ for $\omega_{\text{in}} = 2\omega_n = 2/\sqrt{LC}$. For $\Delta\omega = |\omega_{\text{in}} - 2\omega_n| \ll 2\omega_n$, we have

$$1 - \frac{\omega_{\text{in}}^2}{4\omega_n^2} = \frac{(2\omega_n + \omega_{\text{in}})(2\omega_n - \omega_{\text{in}})}{4\omega_n^2} \tag{15}$$

$$\approx \frac{4\omega_n(2\omega_n - \omega_{\text{in}})}{4\omega_n^2} \tag{16}$$

$$\approx \frac{\Delta\omega}{\omega_n}. \tag{17}$$

Consequently, since $\zeta = (2Q)^{-1}$, the fraction under the square root in (14) can be reduced to $(Q\Delta\omega/\omega_n)^2$, yielding

$$A \geq \frac{2}{\beta}\sqrt{1 + \left(\frac{Q\Delta\omega}{\omega_n}\right)^2}. \tag{18}$$

Fig. 7 plots the input sensitivity as a function of ω_{in}. For example, if we restrict the maximum input amplitude to $4/\beta$, then

$$\Delta\omega = \frac{\sqrt{3}}{Q}\omega_n. \tag{19}$$

As the input amplitude increases, the switching quad of the mixer eventually experiences complete switching, yielding a

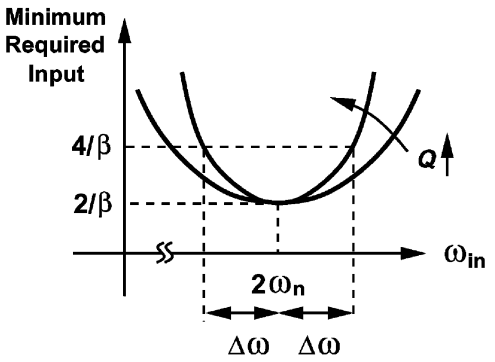

Fig. 7. Minimum input amplitude for correct division versus input frequency.

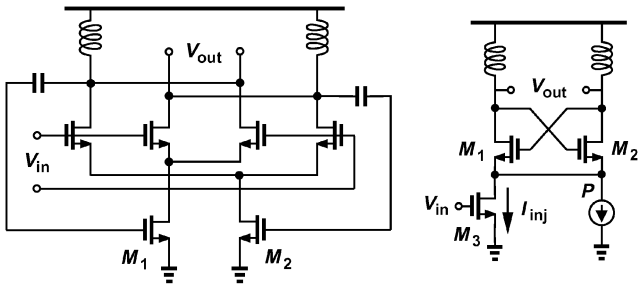

Fig. 8. (a) Simple realization of bandpass divider (bias network for M_1 and M_2 not shown). (b) Injection-locked divider.

conversion factor of $2/\pi$ in the ideal case. The loop gain is then equal to $(2/\pi)g_m$ times the magnitude of the tank impedance, where g_m denotes the transconductance of the bottom differential pair of the mixer. Consequently, (13) is modified to

$$\frac{2}{\pi}g_m\left|\frac{2\zeta\omega_n sR}{s^2 + 2\zeta\omega_n s + \omega_n^2}\right| \geq 1 \tag{20}$$

and (18) to

$$\frac{2}{\pi}g_m R \geq \sqrt{1 + \left(\frac{Q\Delta\omega}{\omega_n}\right)^2}. \tag{21}$$

That is,

$$\Delta\omega = \frac{\omega_n}{Q}\left[\left(\frac{2}{\pi}g_m R\right)^2 - 1\right] \tag{22}$$

$$\approx \frac{\omega_n}{Q}\left(\frac{2}{\pi}g_m R\right)^2. \tag{23}$$

IV. Comparison With Injection-Locked Divider

In this section, we compare a simple realization of the bandpass divider with an injection-locked counterpart (Fig. 8) [4].

With (23) predicting the maximum frequency range of Fig. 8(a), we must seek a similar expression for Fig. 8(b). If the latter divides correctly, transistors M_1 and M_2 switch at a rate of $f_{\text{in}}/2$ while M_3 injects a current at f_{in}. Thus, in a manner similar to a single-balanced mixer, M_1 and M_2 translate the input to $f_{\text{in}} \pm f_{\text{in}}/2$, injecting the result into the tanks. This translation is accompanied by a conversion factor of $2/\pi$ if the

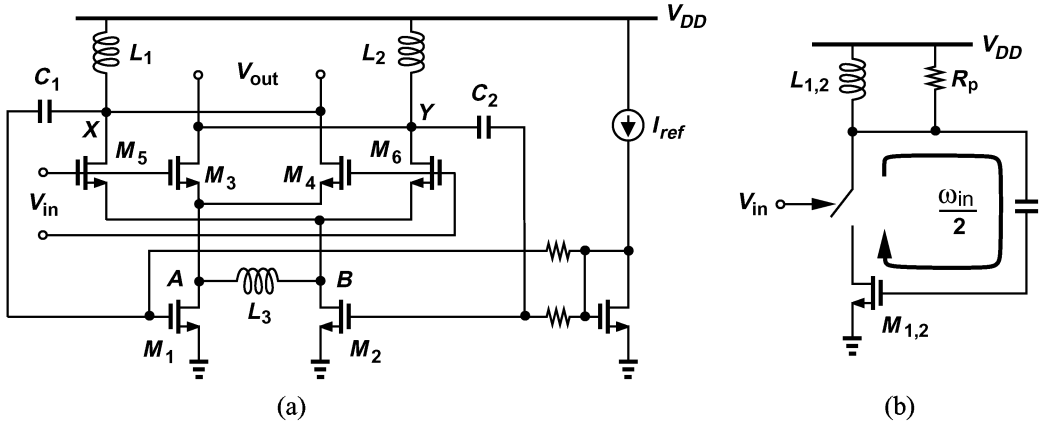

Fig. 9. (a) First ÷2 stage. (b) Simplification of (a).

cross-coupled pair switches abruptly and the capacitance at node P is neglected. As a result, the current injected into the tank at $f_{\rm in}/2$ has a peak value of $(2/\pi)I_{\rm inj}$, allowing a simple modification of Adler's lock range equation [5]:

$$\Delta\omega|_{\frac{f_{\rm in}}{2}} = \frac{\omega_n}{2Q}\frac{I_{\rm inj}}{I_{\rm osc}}\frac{2}{\pi}. \tag{24}$$

Here, the subscript $f_{\rm in}/2$ emphasizes that the lock range is measured at the output, ω_n is the resonance frequency of the tank and equal to $2\pi(f_{\rm in}/2)$, and $I_{\rm osc}$ denotes the peak value of the oscillation current (approximately equal to the tail current). It follows that the lock range at the input is equal to

$$\Delta\omega|_{f_{\rm in}} = \frac{\omega_n}{2Q}\frac{I_{\rm inj}}{I_{\rm osc}}\frac{4}{\pi}. \tag{25}$$

Circuit simulations indicate that this is a good approximation for the upper bound on the lock range.

For the two circuits to divide correctly across the same input frequency range, (23) and (25) must be equal, yielding

$$\frac{1}{\pi}g_m^2R^2 = \frac{I_{\rm inj}}{I_{\rm osc}}. \tag{26}$$

This result implies that even if the injection level in Fig. 8(b) were to approach the oscillation level, $I_{\rm inj} \approx I_{\rm osc}$, the circuit of Fig. 8(a) would need a g_mR of only $\sqrt{\pi} \approx 1.8$ to provide the same frequency range. In other words, the bandpass divider using feedback to the RF port generally achieves a wider range.[2]

Exhibiting no tendency to oscillate with $V_{\rm in} = 0$, the scheme of Fig. 8(a) is expected to produce less phase noise. Indeed, SpectreRF simulations indicate that, for a given power dissipation and output frequency, this circuit achieves 4 dB less phase noise (for offset frequencies up to 10 MHz) than the injection-locked divider with $I_{\rm inj} \approx I_{\rm osc}$.

Another difference between the topologies in Fig. 8 relates to their outputs under incorrect operation: Fig. 8(a) produces zero whereas Fig. 8(b) generates an injection-pulled waveform. It is, therefore, simpler at the system level to detect failure in the former and perhaps tune it by means of varactors.

[2]Simulations indicate that the output amplitude varies by only a few percent across this range.

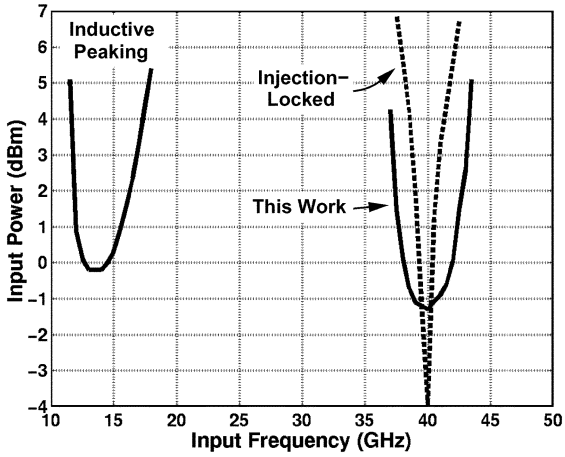

Fig. 10. Simulated operation behavior of CMOS dividers.

V. Circuit Implementation

A. First Divider Stage

Fig. 9(a) shows the first ÷2 stage. Here, load inductors $L_1 = L_2 = 0.85$ nH resonate with the parasitic capacitances at nodes X and Y and the input capacitance of M_1 and M_2, thus providing a 600-Ω equivalent resistance at 20 GHz with negligible voltage headroom consumption.

The device dimensions and component values in this circuit must be chosen so as to provide both sufficient loop gain—to guarantee correct division—and large enough output swings necessary for the subsequent stage. Assuming abrupt, complete switching of $M_3 - M_6$, neglecting the effect of L_3 and parasitic capacitances, and simplifying the circuit to that shown in Fig. 9(b), we express the voltage conversion gain of the mixer (= loop gain) as $(2/\pi)g_{m1,2}R_p$, where $R_p = QL_{1,2}\omega$ denotes the equivalent parallel resistance of each tank. Since $g_m \approx 2\pi f_T C_{GS}$ and since the loop gain must exceed unity

$$\frac{2}{\pi}2\pi f_T C_{GS} Q L_{1,2}\frac{\omega_{\rm in}}{2} \geq 1. \tag{27}$$

With all of the parasitics neglected, $\omega_{\rm in}/2 \approx 1/\sqrt{C_{GS}L_{1,2}}$ and hence

$$Q \geq \frac{\pi}{4}\frac{f_{\rm in}}{f_T} \tag{28}$$

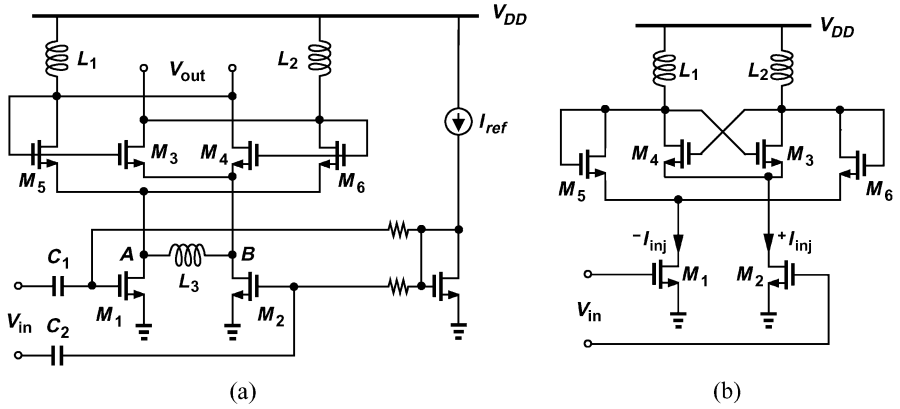

Fig. 11. (a) Second ÷2 stage. (b) Redrawn to show injection locking.

where $f_{\rm in}$ is the input frequency.[3] This result implies that, even for input frequencies as high as f_T, a Q of about unity suffices. However, the following effects necessitate a much higher Q.

1) The total capacitance at nodes A and B; even if the source/drain junction capacitances are neglected, $M_3 - M_6$ create a pole around f_T at these nodes, "wasting" about half of the small-signal drain currents of M_1 and M_2.
2) The gradual switching of $M_3 - M_6$ with a nearly sinusoidal drive converts part of the differential currents produced by M_1 and M_2 to a common-mode component.
3) The parasitic capacitances of the load inductors and the coupling capacitors lead to $\omega_n < 1/\sqrt{C_{GS}L_{1,2}}$. Simulations reveal that the Q must exceed 4.5 for correct division.

In summary, the required Q of the tank is determined by the following requirements: attenuation of the third harmonic, sufficient loop gain in the ideal case, and sufficient loop gain in the presence of parasitics—with the last dominating in this design.

Since all of the six transistors in this circuit are relatively wide $[(W/L)_{1,2} = 16/0.18, (W/L)_{3\sim6} = 10/0.18]$, the total capacitance at the drains of M_1 and M_2 shunts a considerable portion of their small-signal drain current to ground. Inductor L_3 is, therefore, added to resonate with this capacitance. Realized as a symmetric structure, $L_3 = 1.6$ nH exhibits a higher Q with differential signals (estimated to be around 10 at 20 GHz), introducing a resistance of 2 kΩ between A and B. This impedance is much greater than that seen looking into the sources of M_3–M_6, thereby wasting little current. Since the feedback signal is applied to the RF port, the circuit produces a zero output when the LO input is zero. In contrast to the injection-locked oscillator of Fig. 8(b), this topology is not prone to oscillation.

Fig. 10 plots the simulated sensitivity of three CMOS dividers topologies: Miller divider with inductive peaking,[4] the proposed circuit, and an injection-locked configuration.

B. Second Divider Stage

The second ÷2 stage is depicted in Fig. 11(a). In this case, the output is returned to the switching quad rather than to the bottom pair so as to present less capacitance to the first divider. This circuit in fact operates as an injection-locked oscillator if $(W/L)_{3,4} \neq (W/L)_{5,6}$: M_3 and M_4 form a cross-coupled pair, and M_5 and M_6 appear as diode-connected transistors, lowering the Q of the tank and, hence, increasing the lock range.[5] Inductor L_3 resonates with the capacitances at nodes A and B, widening the lock range to some extent [7]. In contrast to injection-locked dividers with a single-ended input [4], [7], this topology injects the differential phases of the 20-GHz signal into the tail nodes and the output nodes. Simulations indicate that differential injection in this manner increases the lock range by 20%.

The bottom-plate parasitic capacitance of C_1 and C_2 in Fig. 9(a) and Fig. 11(a) lowers the loop gain of the first stage. These capacitors are, therefore, realized as "fringe" structures [8] to obtain both small parasitics and a high density. A differential pair buffers this stage and drives the external load.

Since the operation frequency range of the overall ÷4 circuit is given by the intersection of those of the two stages, accurate device modeling proves critical here. In particular, the inductors and their parasitics must be modeled carefully to achieve the necessary resonance frequencies.

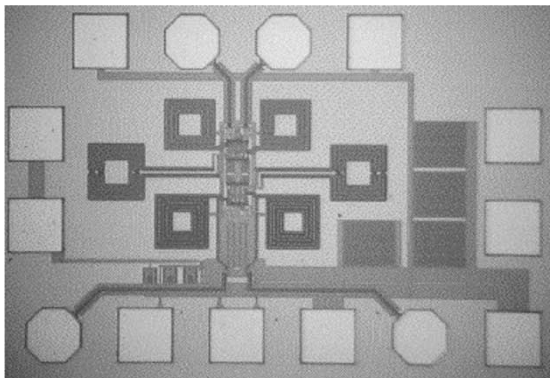

Fig. 12. Die photo.

VI. Experimental Results

The frequency divider has been designed and fabricated in a 0.18-μm CMOS technology. Shown in Fig. 12 is a photograph

[3]Equation (28) holds for the center of the input frequency range, i.e., if the tank can be reduced to a single resistor R_p.

[4]Similar to that in [6].

[5]In this design $(W/L)_{3,4} = (W/L)_{5,6}$ so that the circuit has no tendency to oscillate.

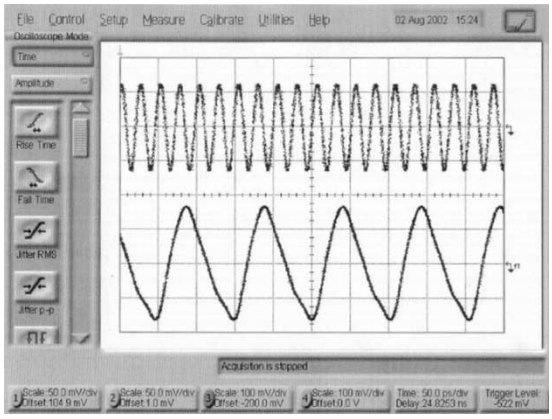

Fig. 13. Single-ended input and output waveforms of the divider. (Horizontal scale: 50 ps/div, vertical scale: 100 mV/div. Input waveform attenuated by 10 dB in this display.).

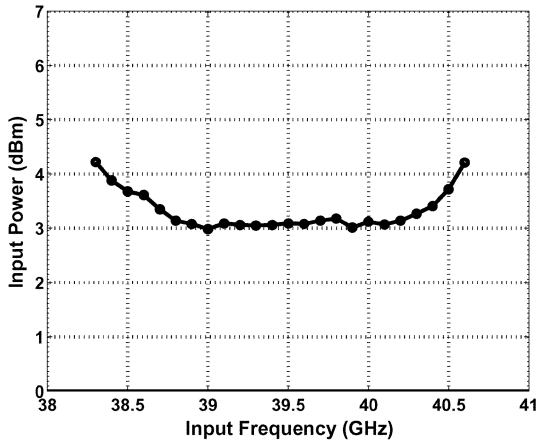

Fig. 14. Measured input sensitivity of the divider.

of the die, which measures 0.5 mm $\times$ 0.7 mm. The circuit has been tested on a high-speed probe station while running from a 2.5-V power supply. Note that none of the devices experiences more than 1.8 V across it in steady-state operation.

Fig. 13 shows the measured input and output waveforms of the divider, and Fig. 14 plots the minimum required input level for correct operation. This measurement is constrained by the limited output power of the 40-GHz RF generator, loss in the probes, and lack of a 40-GHz single-ended-to-differential converter. Nonetheless, the frequency range of ± 1.25 GHz around 39.5 GHz for 1.3-dB increase in input level agrees reasonably well with that predicted by (23) if a Q of 8 is assumed at 20 GHz.

The spectrum of the 10-GHz output is shown in Fig. 15, exhibiting a phase noise of approximately -115 dBc/Hz at 1-MHz offset.[6] The circuit draws 16.8 mW in the first stage and 14 mW in the second.

VII. Conclusion

This paper has presented an analysis of the Miller divider that reveals the conditions for correct division. A divider topology

[6]The loss in the output buffer degrades the phase noise to some extent.

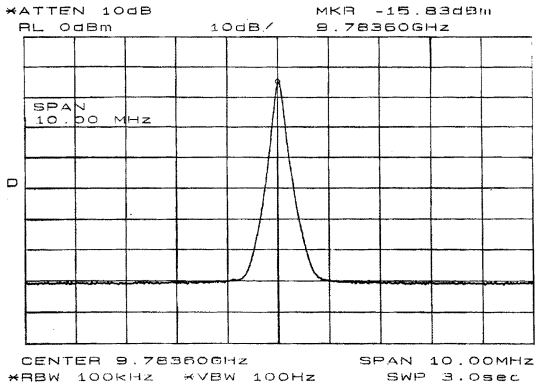

Fig. 15. Spectrum of the 10-GHz output. (Horizontal scale: 1 MHz/div., vertical scale: 10 dB/div.).

is proposed that incorporates resonant tanks at both the output and the internal nodes of a Gilbert cell, increasing the operation frequency considerably. The proposed circuit is also compared with injection-locked dividers. A divide-by-4 circuit employing these techniques operates at 40 GHz.

References

[1] H.-D. Wohlmuth *et al.*, "A high sensitivity static 2:1 frequency divider up to 27 GHz in 120 nm CMOS," in *Proc. Eur. Solid State Circuits Conf. (ESSCIRC)*, 2002, pp. 823–826.

[2] J.-O. Plouchart *et al.*, "A power-efficient 33 GHz 2:1 static frequency divider in 0.12-μm SOI CMOS," in *RFIC Symp. Dig. Papers*, 2003, pp. 329–332.

[3] R. L. Miller, "Fractional-frequency generators utilizing regenerative modulation," *Proc. Inst. Radio Eng.*, vol. 27, pp. 446–456, July 1939.

[4] H. R. Rategh and T. H. Lee, "Superharmonic injection-locked frequency dividers," *IEEE J. Solid-State Circuits*, vol. 34, pp. 813–821, June 1999.

[5] R. Adler, "A study of locking phenomena in oscillators," *Proc. Inst. Radio Eng.*, vol. 34, pp. 351–357, June 1946.

[6] M. Kuriso *et al.*, "A Si bipolar 28 GHz dynamic frequency divider," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 1992, pp. 92–93.

[7] H. Wu and A. Hajimiri, "A 19-GHz 0.5-mW 0.35-μmm CMOS frequency divider with shunt-peaking locking range enhancement," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2001, pp. 412–413.

[8] O. E. Akcasu, " High capacitance structure in a semiconductor device," U.S. Patent 5,208,725, May 4, 1993.

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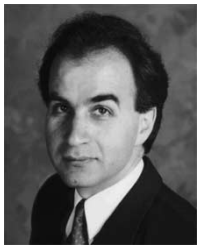

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