A 40-Gb/s Clock and Data Recovery Circuit in 0.18-μm CMOS Technology

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***Abstract*—A phase-locked clock and data recovery circuit incorporates a multiphase *LC* oscillator and a quarter-rate bang-bang phase detector. The oscillator is based on differential excitation of a closed-loop transmission line at evenly spaced points, providing half-quadrature phases. The phase detector employs eight flip-flops to sample the input every 12.5 ps, detecting data transitions while retiming and demultiplexing the data into four 10-Gb/s outputs. Fabricated in 0.18-μm CMOS technology, the circuit produces a clock jitter of 0.9 ps_{rms} and 9.67 ps_{pp} with a PRBS of $2^{31}-1$ while consuming 144 mW from a 2-V supply.**

***Index Terms*—CDR circuits, demultiplexers, injection locking, oscillators, phase detectors, phase-locked loops.**

I. Introduction

CLOCK and data recovery (CDR) circuits operating at tens of gigabits per second pose difficult challenges with respect to speed, jitter, signal distribution, and power consumption. Half-rate 40-Gb/s CDR circuits have been implemented in bipolar technology [1], [2], but they require 5-V supplies and draw 1.6–5 W of power. (The work in [1] uses an external oscillator and 90° phase shifter.) On the other hand, the recent integration of 10-Gb/s receivers in CMOS technology [3] encourages further research on CMOS solutions for higher speeds, especially if it leads to low-voltage low-power realizations.

This paper presents the design and experimental verification of a 40-Gb/s phase-locked CDR circuit fabricated in 0.18-μm CMOS technology. Realized as a quarter-rate architecture, the circuit incorporates a multiphase oscillator and a phase detector (PD) with inherent data retiming and 1-to-4 demultiplexing. Section II describes the design implications of the technology limitations, arriving at the CDR architecture. Section III deals with the design of each building block, and Section IV examines the effect of nonidealities. Section V summarizes the experimental results.

II. CDR Architecture

A. General Considerations

We consider the technology limitations in the context of the full-rate deserializer shown in Fig. 1(a). The f_T of an nMOS transistor with $L = 0.18$ μm and $V_{GS} - V_{TH} = 500$ mV is approximately equal to 50 GHz. If used in a differential pair, such a device bias requires a single-ended peak-to-peak input swing of about 700 mV to ensure relatively complete switching of the tail current, which is a value five times that necessary in bipolar counterparts. That is, a bipolar transistor having the same f_T allows much faster operation. In practice, current-steering flip-flops (FFs) in 0.18-μm CMOS technology with a fanout of one fail at approximately 12 Gb/s even if large clock swings are used. Since broadband data is much more difficult to amplify than are narrowband clocks, this observation suggests relaxing the data path design in exchange for more stringent clock generation.

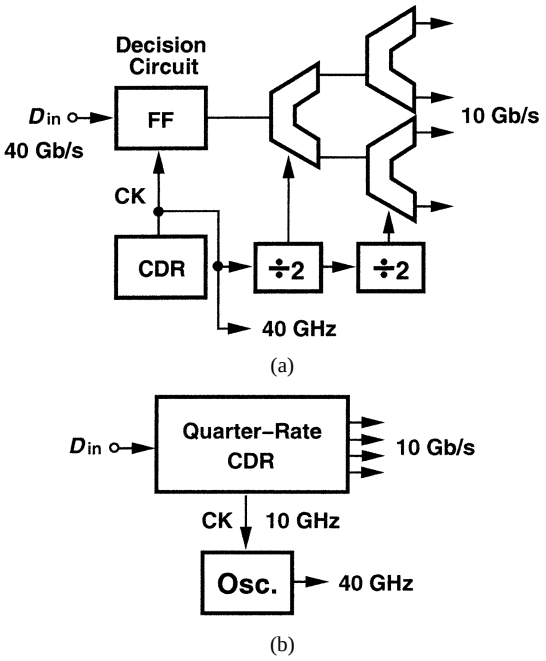

Fig. 1. (a) Full-rate and (b) quarter-rate deserializer.

The speed of FFs can be improved by inductive peaking [4], but inductor parasitics in CMOS technology limit such an improvement to less than 40%, prohibiting even a half-rate CDR approach. More importantly, the large area consumed by inductors in at least four latches required for a half-rate phase detector [5] would make it difficult to route the 40-Gb/s data and the 20-GHz clock with reasonable skews (Section IV). Similarly, the first and second ranks of demultiplexing in Fig. 1(a) face severe speed limitations.

Another critical issue in Fig. 1(a) relates to the design of high-speed frequency dividers. Due to the limited capture range of CDR circuits, the oscillator must initially be locked to an external reference [3], requiring a feedback divider. Moreover, dividers are necessary for generating clock frequencies used in demultiplexing of the data. Typical divide-by-two circuits fail

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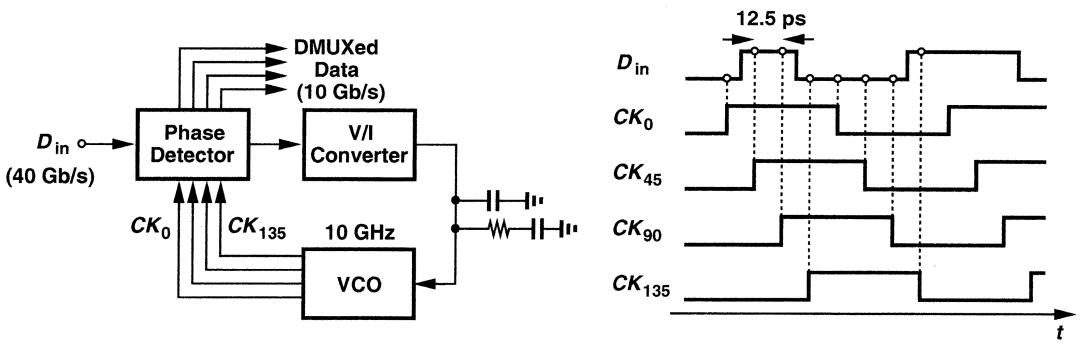


Fig. 2. CDR architecture.

at frequencies above 20 GHz in 0.18-μm CMOS technology. Also, *LC* oscillators having a reasonable tuning range at 40 GHz present another challenge.

Let us now consider the deserializer shown in Fig. 1(b). Here, a quarter-rate CDR circuit inherently retimes and demultiplexes the data, obviating full-rate FFs and frequency dividers.[1] The sensitivity of the clock phase margin (jitter tolerance) to oscillator phase mismatches can be alleviated through the use of large devices and careful layout.

Design of a 40-Gb/s system in 0.18-μm CMOS technology is motivated by two factors: 1) the mask and fabrication cost of the next generation (e.g., 0.13 μm) is substantially higher; and 2) many new techniques that relax the speed requirements here can be used in future generations to lower the power dissipation and complexity.

B. CDR Architecture

The CDR circuit employs a quarter-rate architecture to relax the issues described above. Shown in Fig. 2, the circuit incorporates a multiphase voltage-controlled oscillator (VCO), a quarter-rate phase detector (PD), a voltage-to-current (V/I) converter, and a simple loop filter. The PD uses the half-quadrature phases provided by the VCO to sample the input data every 12.5 ps, thereby detecting data edges and determining whether the clock is early or late. Four of these samples fall in the center of the data eye, retiming and demultiplexing the 40-Gb/s input into four 10-Gb/s outputs. In the absence of data transitions, the V/I converter generates no output current, leaving the oscillator control line undisturbed. The circuit is fully differential, except for the oscillator control line.

With quarter-rate sampling, the FFs' hold time can be four times that required in full-rate operation, but their acquisition speed must still guarantee correct sampling of the input bits in less than 50 ps. The FF design described in Section III accomplishes this goal.

It is interesting to compare the quarter-rate architecture of Fig. 2 with a full-rate system in terms of power dissipation, hardware, and clock load capacitance. The PD of Fig. 2 employs 16 latches to perform phase detection, data retiming, and 1-to-4 demultiplexing, with each clock phase driving two latches. Depicted in Fig. 3, the full-rate counterpart incorporates seven latches in an Alexander PD [6], four latches in two

[1]In applications requiring a full-rate recovered clock, a 40-GHz oscillator can be injection-locked to the 10-GHz VCO.

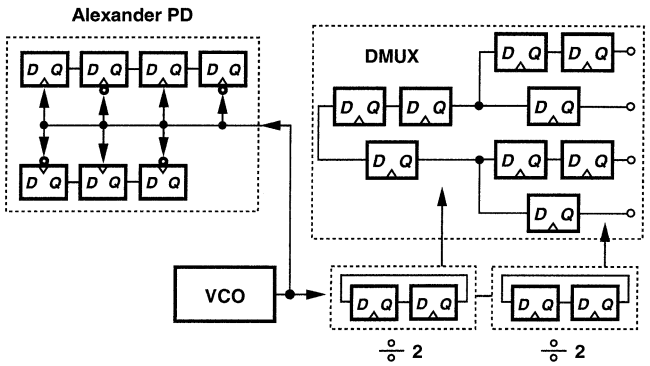


Fig. 3. Full-rate CDR and DMUX architecture.

cascaded divide-by-two circuits, and a minimum of nine latches in the demultiplexer, i.e., nine latches operating at full rate and eleven at half rate. Note that the full-rate clock drives the input capacitance of nine latches. Thus, the two architectures consume comparable power levels in their digital sections, but the latter presents a substantially larger capacitance to the full-rate clock.

III. Building Blocks

A. VCO

The speed, jitter, and driving capability required of the oscillator point to the use of an *LC* realization. A number of multiphase *LC* oscillators have been reported. Coupled oscillators [8]–[10] operate away from the resonance frequency of the tanks so as to create the required phase shift, thus bearing a tradeoff between reliability of oscillation and the phase noise [10]. The multiphase oscillator in [11] drives transmission lines by a resistively-loaded gain stage, incurring energy loss in each cycle.

The multiphase oscillator introduced here is based on the concept of differential stimulus of a closed-loop transmission line at evenly-spaced points, as illustrated conceptually in Fig. 4(a) with two differential negative-G_m cells. Approximated in Fig. 4(b) by lumped inductors and capacitors, the circuit consists of eight inductors forming a loop and four differential negative-G_m cells driving diagonally opposite nodes. In the steady state, every two such nodes sustain a phase separation of 180°, thus providing 45° phase steps in between. Unlike the topologies in [9] and [10], this oscillator does not operate away from the resonance frequency. Also, in contrast to

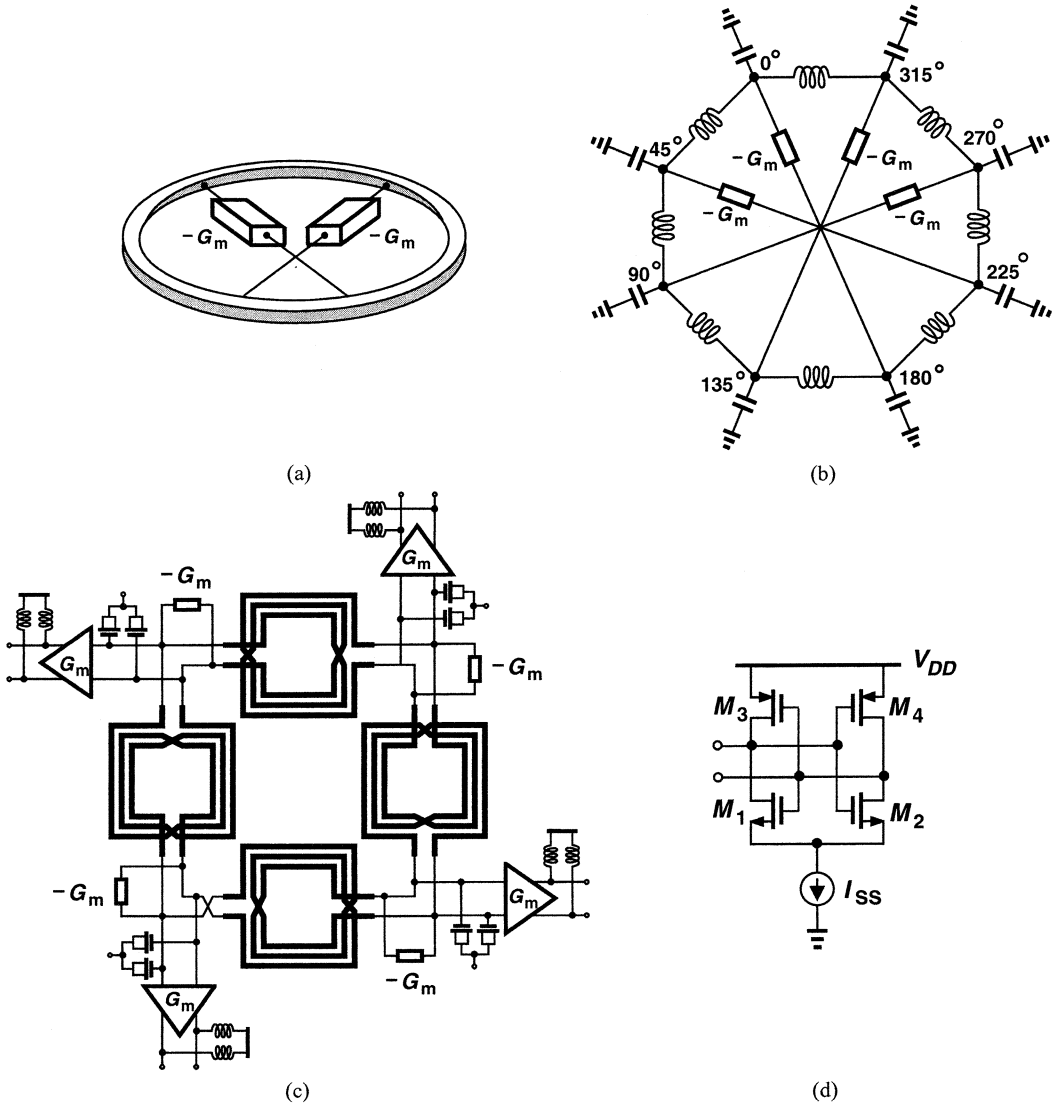


Fig. 4. (a) Proposed oscillator. (b) Half-quadrature implementation. (c) Modification of (b). (d) Realization of $-G_m$ cell.

the design in [11], the transmission line requires no termination resistors, thereby displaying lower phase noise and larger voltage swings for a given power dissipation and inductor Q. Fig. 5 plots the phase noise of three 10-GHz half-quadrature oscillator topologies simulated in Spectre RF and designed with the same power dissipation and inductor Q. The proposed oscillator achieves at least 7-dB lower phase noise and twice the voltage swing.

The oscillation frequency of the circuit is uniquely given by the travel time of the wave around the loop. Noting that the phase velocity in a transmission line is equal to $v = 1/\sqrt{L_o C_o}$, where L_o and C_o represent the inductance and capacitance per unit length, respectively, we write the oscillation frequency of this topology as

$$f = \frac{1}{8\sqrt{LC}} \tag{1}$$

where L and C, respectively, denote the lumped inductance and capacitance of each of the eight sections.

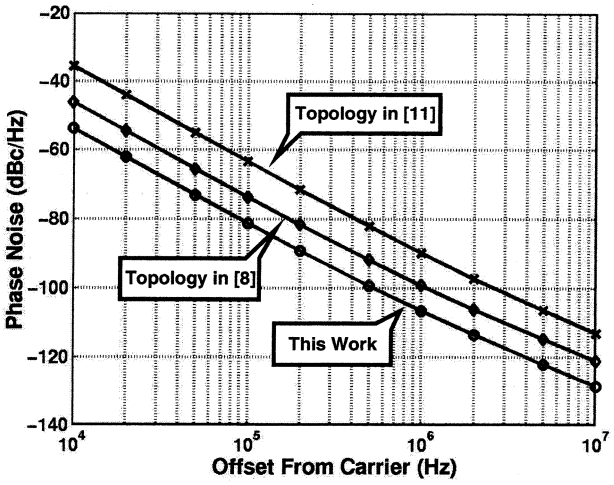


Fig. 5. Simulated phase noise.

The topology of Fig. 4(b) necessitates long interconnects between the nodes and their corresponding $-G_m$ cells. However, recognizing that diagonally opposite inductors carry currents

that are 180° out of phase, we modify the circuit as shown in Fig. 4(c), grouping inductor elements into differential structures and placing the $-G_m$ cells in close proximity of the oscillator nodes. Exploiting the higher Q of differential inductors [12], the VCO incorporates the $-G_m$ cell shown in Fig. 4(d), shaping the rising and falling edges by the pMOS transistors and hence lowering the upconversion of $1/f$ noise [13]. The value of each differential inductor is 0.9 nH.

Each node in the oscillator in loaded by a MOS varactor. With the oscillation common-mode level set by the $-G_m$ cells to around $V_{\rm DD}/2$, the MOS varactors can go from the accumulation mode to the depletion mode, maximizing the tuning range. Unlike the design in [11], the VCO avoids external control and, hence, exhibits a high gain, approximately 1 GHz/V, thus necessitating a smaller ripple on the control line to obtain low jitter.

Each differential port of the VCO in Fig. 4(b) is buffered by an inductively-loaded differential pair. These buffers serve to: 1) isolate the VCO from the long interconnects going to the PD that would otherwise introduce greater uncertainty in the oscillation frequency; 2) generate voltage swings above the supply voltage, thus driving the FFs in the PD efficiently (Section III); and 3) isolate the VCO from the data edges coupled through the phase detector.

Device mismatches in the circuit of Fig. 4(c) yield nonuniform separations between adjacent VCO phases and, hence, static phase error in the CDR. Circuit simulations predict a phase mismatch of 0.22 ps for a 5% mismatch between the *LC* products in two adjacent tanks. Such a mismatch also shifts the oscillation frequency by 0.3%, which is an error well within the tuning range.

An interesting issue in the proposed VCO is that, due to symmetry, the wave may propagate clockwise rather than counterclockwise. In the present prototype, this effect is not observed, perhaps because the Q of the inductors is slightly higher when the current flows from the outer turns toward the inner turns. Nonetheless, to achieve a more robust design, a means of detecting the wave direction is necessary. Since nodes that are 90° apart in one case exhibit a phase difference of −90° in the other case, an FF sensing such nodes at its data and clock inputs generates a constant high or low level, thereby providing a dc quantity indicating the wave direction.[2] As described in the next section, this result can be used to avoid corruption of data.

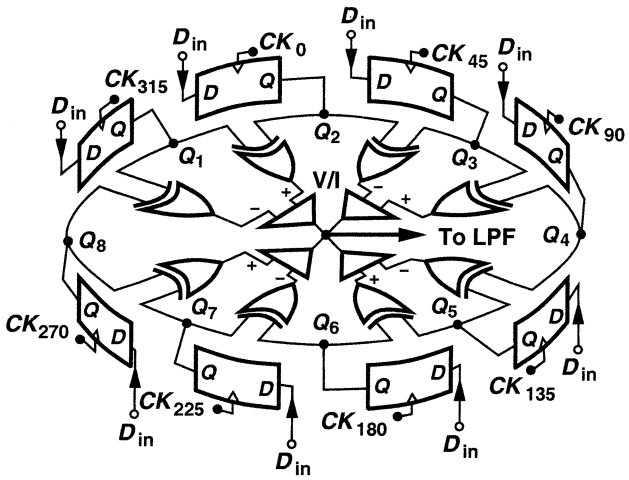
B. Phase Detector

1) Architecture: The PD employs eight FFs to strobe the data at 12.5-ps intervals (Fig. 6). In a manner similar to an Alexander topology, the PD compares every two consecutive samples by means of an XOR gate, generating a high level if an edge has occurred. To determine the polarity of the phase error from three consecutive samples, the outputs of two XORs are applied to a V/I converter, which produces a net current if its inputs are unequal. In lock, every other sample serves as a retimed and demultiplexed output.

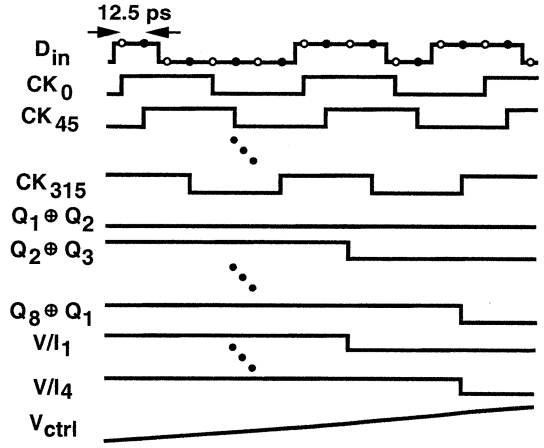
It is important to note that, in the absense of data transitions, the FFs generate equal outputs, and each V/I converter produces a zero current, in essence presenting a tristate (high) impedance to the oscillator control. This is in contrast to other bang-bang topologies [7], [5] that continue to apply a high or low level to the VCO during long runs, creating a potentially high jitter.

The early-late phase detection method used here exhibits a bang-bang characteristic, forcing the CDR circuit to align every other edge of the clock with the zero crossings of data after the

[2]In practice, four FFs could be connected to the buffered outputs to equalize the loading, but they would consume a small power and present a small capacitance.



(a)



(b)

Fig. 6. (a) Quarter-rate phase detector. (b) Its waveforms.

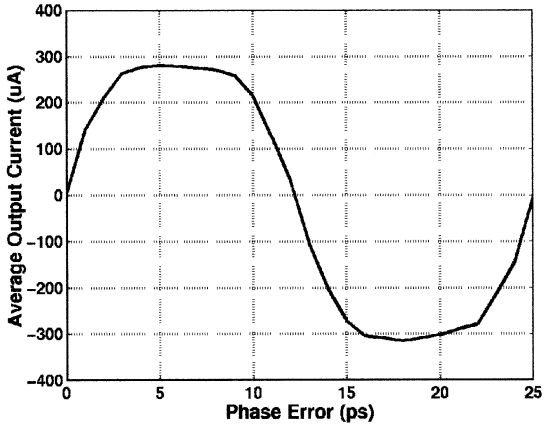
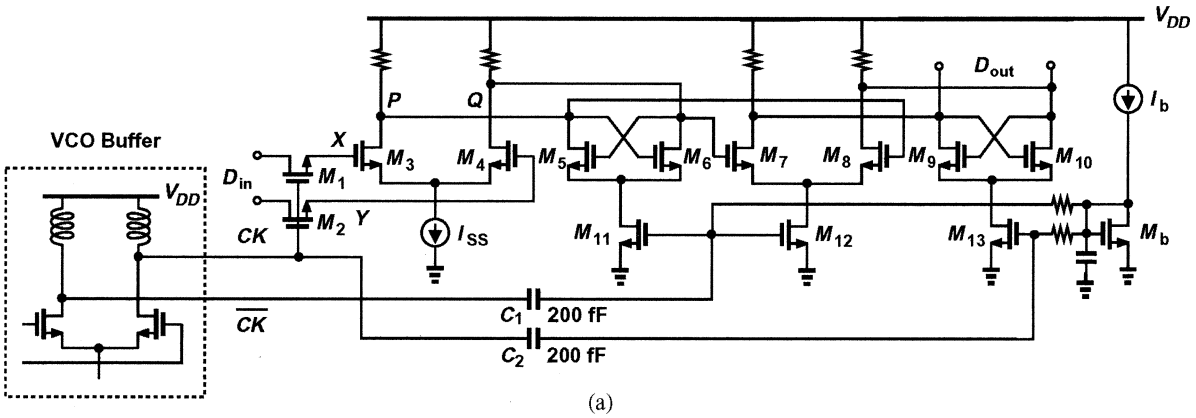
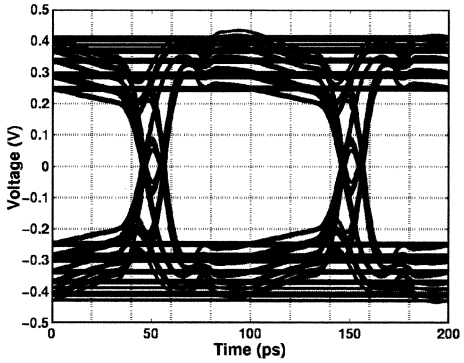


Fig. 7. Simulated input/output characteristic of the PD together with the V/I converter.



(a)



(b)

Fig. 8. (a) Flip-flop. (b) Differential eye diagram at X and Y.

loop is locked.[3] In reality, the metastable behavior of the FFs leads to a finite PD gain, allowing the clock edges to sustain some offset with respect to the data zero crossings. Shown in Fig. 7 is the input/output characteristic of the PD together with the V/I converter, obtained by transistor-level simulations while the circuit senses a 40-Gb/s random data stream and eight phases of the 10-GHz clock. For a phase error $\Delta\phi$ of less than $\pm$2.5 ps, the PD displays a relatively constant gain of 100 μA/ps. With an ideal V/I converter, a finite phase difference would still lead to injection of a finite current into the loop filter (similar to an ideal integrator), forcing the loop to lock with a zero static phase error. The output resistance of the V/I converter, on the other hand, results in lossy integration, necessitating a small change in $\Delta\phi$ as the control voltage varies from minimum to maximum. Nevertheless, simulations indicate that, with the present PD and V/I converter design, the static phase offset reaches 0.8 ps as the V/I output varies from near zero to near $V_{\rm DD}$.

As mentioned in the previous section, the arbitrary wave direction in the oscillator yields two possible sets of phases, but a FF can detect the direction. Analysis of the PD and loop operation for the two possibilities reveals that in one case, the even-numbered PD outputs are metastable whereas in the other case, the odd-numbered outputs are. Thus, the dc level generated by direction detector FF can simply select and reroute the nonmetastable outputs to the next rank of demultiplexing.

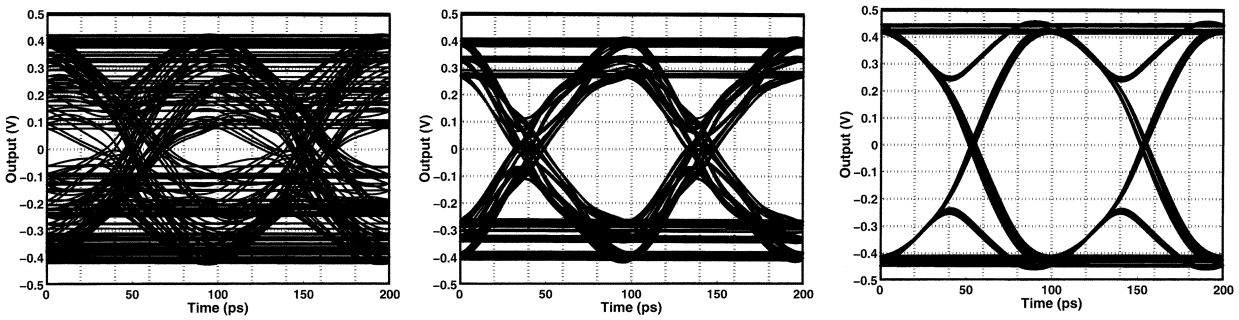
2) FF Design: Even though the PD FFs operate with a 10-GHz clock, proper sampling of 40-Gb/s data still requires fast recovery from the previous state and rapid acquisition of the present input. To this end, both a wide sampling bandwidth and a short clock transition time are necessary. Fig. 8(a) depicts the master–slave FF used in the phase detector. Here, nMOS switches M_1 and M_2 sample $D_{\rm in}$ on the parasitic capacitances at nodes X and Y when CK is high and isolate these nodes from $D_{\rm in}$ when CK is low. Since the minimum input common-mode (CM) level is dictated by the gate–source voltage of M_3-M_4 and the headroom required by $I_{\rm SS}$, the sampling switches experience an overdrive voltage of only 0.5 V even if CK reaches $V_{\rm DD}$, failing to provide fast sampling. This issue is remedied by setting the CM level of CK and $\overline{\rm CK}$ equal to $V_{\rm DD}$, a choice afforded by inductively-loaded stages following the VCO core. The peak value of CK thus exceeds $V_{\rm DD}$ by 0.8 V, more than doubling the sampling speed of M_1 and M_2.[4] The large clock swings also minimize the transition times.[5] As M_1 and M_2 turn off, their channel charge injection and clock feedthrough introduce a CM pedestal of 200 mV at the gates of M_1 and M_2. Fig. 8(b) shows the simulated eye diagram at nodes X and Y.

With large clock swings available, the current switching in pairs M_5-M_6, M_7-M_8, and M_9-M_{10} is accomplished by gate control rather than conventional source-coupled steering. The proposed topology offers two advantages: 1) since the tail current source is removed, M_{11}-M_{13} can be much narrower, presenting a smaller capacitance to the VCO buffer; and 2) since the drain currents of M_{11}-M_{13} are not limited by a tail current source, these transistors experience class-AB switching,

[3]Whether the odd-numbered or even-numbered samples are metastable depends on the polarity of the feedback around the CDR loop.

[4]The small-signal bandwidth at the gates of M_1 and M_2 exceeds 55 GHz.

[5]The buffer transistors experience a peak drain–gate voltage of 2 V, slightly degrading the reliability.



(a) (b) (c)

Fig. 9. Output data for (a) conventional current-steering FF, (b) conventional current-steering FF with inductive peaking, and (c) proposed FF.

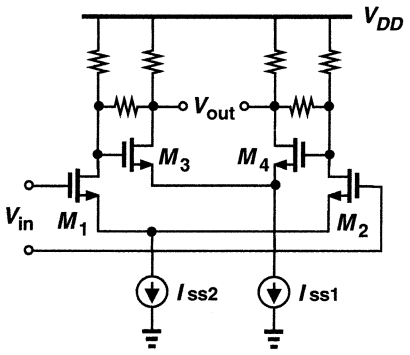


Fig. 10. Cherry–Hooper amplifier.

drawing a large current at the peak of the clock swing and providing greater voltage swings and a higher gain in the data path.

The coupling capacitors C_1 and C_2 in Fig. 8 can potentially occupy a large area and/or present a great bottomplate capacitance to the clock lines. To resolve this issue, these capacitors are realized as fringe structures [14] using metal-2 through metal-5 layers.

Fig. 9 compares the performance of the above FF with a standard current-steering topology consuming the same power and driven by the same clock swings with and without inductive peaking. Derived from simulations, the waveforms in Fig. 9(a)–(c) represent the 10-Gb/s output resulting from quarter-rate sampling of 40-Gb/s data. It can be seen that the proposed FF introduces much less intersymbol interference (ISI). The circuit can benefit from inductive peaking, but skew issues in the layout (Section IV) prohibit the use of inductors here.

The connection of the sources of M_{11}-M_{13} to ground rather than to tail current sources can potentially corrupt the data in the presence of noise on the supply voltage of the VCO buffer. Simulations reveal that a 10-$\mathrm{mV_{pp}}$ 1-GHz sinusoid on the supply increases the jitter at the output of the FF by 0.03 ps.

Each FF in the PD must drive an XOR gate. Furthermore, four of the FFs must also drive output buffers or subsequent stages of demultiplexing. To avoid systematic delay mismatches resulting from loading disparity, all FFs are immediately followed by a Cherry–Hooper amplifier (Fig. 10) [15], tapered up in driving capability by a factor of 1.5 from M_1–M_2 to M_3–M_4.

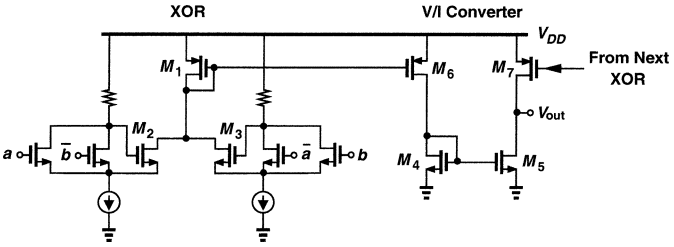


Fig. 11. XOR gate and V/I converter.

3) XOR Gate and V/I Converter: The XOR gates used in the PD must exhibit symmetry with respect to their two inputs and operate with a low supply voltage. Shown in Fig. 11 along with the V/I converter, the XOR gate is a modified version of that in [16], with transistors M_2 and M_3 forming local positive feedback loops and avoiding the reference voltage necessary in the earlier realization [16].

The V/I converter copies the output current of the XOR, providing nearly rail-to-rail swings for the oscillator control line. Unlike charge pumps, V/I converters need not switch after every phase comparison and are, therefore, free from the dead-zone issue.

IV. Effect of Nonidealities

A. Staggered Outputs

In order to save power and minimize the clock load capacitance, the PD uses only one FF in each data sampling path. As a result, the outputs of consecutive FFs in Fig. 6(a) are staggered by 12.5 ps, failing to provide the instantaneous phase-error information simultaneously. Since the low-pass filter extracts the average value of the V/I output, the CDR loop still locks properly, but the misalignment creates ripple on the oscillator control line.

To estimate the jitter resulting from this effect, we consider the worst case, illustrated in Fig. 12, where only half of the PD is shown for the sake of clarity. Assuming a run of at least seven zeros before sample 1, we observe that sample 2 drives both X_1 and X_2 high, still generating $I_1 = 0$. At sample 3, X_2 goes low, X_3 goes high, and both I_1 and I_2 assume their maximum value. This condition holds for 87.5 ps, leading to a peak jitter of

$$\Delta T = \frac{T}{2\pi} K_{\mathrm{VCO}} \int_0^{87.5\ \mathrm{ps}} (I_1 + I_2) R_p \, dt \qquad (2)$$

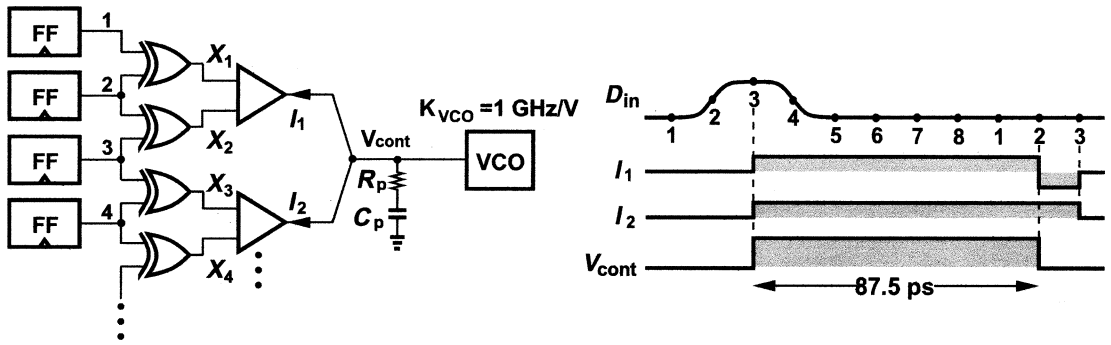


Fig. 12. Effect of staggered outputs.

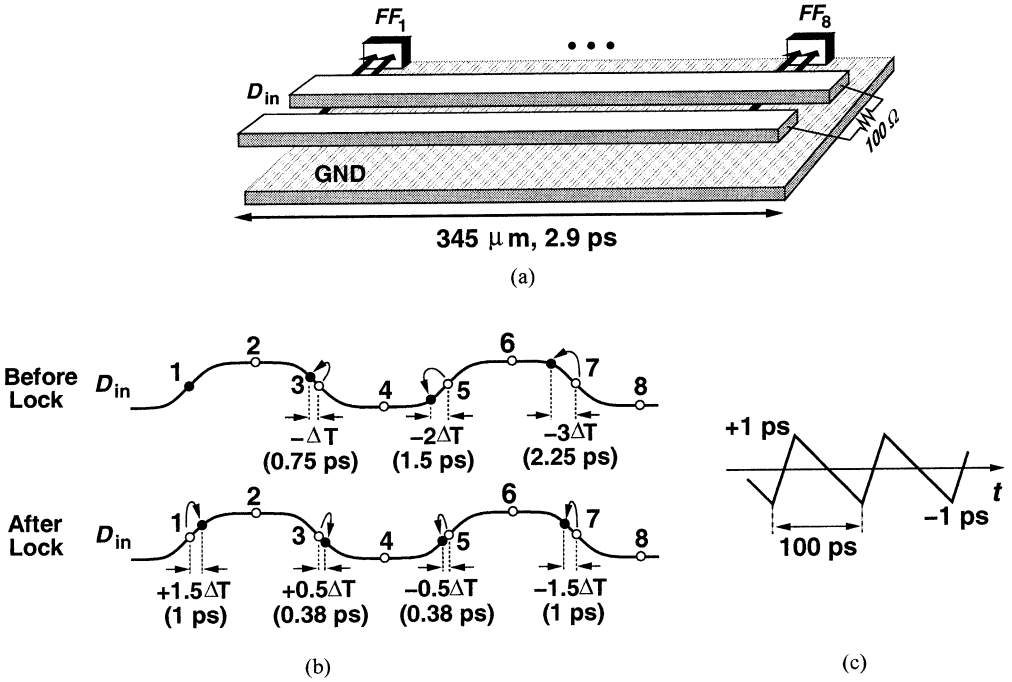


Fig. 13. (a) Layout of input lines. (b) Skews resulting from group velocity. (c) Modulation of input data.

where T denotes the oscillation period, and the VCO delay[6] and the change in the voltage across C_p are neglected. In this design, $K_{\rm VCO} \approx 2\pi \times 1$ Grad/s/V, $I_1 = I_2 = 0.5$ mA, and $R_p < 10\ \Omega$, yielding $\Delta T < 0.1$ ps. Note that for larger run lengths, the above integration still takes place for 87.5 ps.

B. Finite Group Velocity

The performance of the PD is also influenced by the finite group velocity of the 40-Gb/s input data as it travels from one end of the FF array to the other end.[7] As shown in Fig. 13(a), the input data flows on differential microstrip lines made of metal-6 on top of a metal-1 ground plane. The microstrip lines are designed to have a 100-Ω differential characteristic impedance with the input capacitance of the FFs included. This capacitance lowers the line group velocity to about 40% of the speed of light, resulting in a skew of nearly 2.9 ps between the inputs of the first and last FFs.

As shown in Fig. 13(b), the sampled zero crossings of the data before locking are shifted to the left by 0.75, 1.5, and 2.25 ps. However, upon lock, the loop tries to minimize the dc level generated by these samples, shifting the first sample to the right by 1 ps and the last to the left by 1 ps. This is equivalent to periodic phase modulation of the input by ± 1 ps at a rate of 10 GHz [Fig. 13(c)]. Fortunately, the limited bandwidth of the CDR rejects this jitter. Nonetheless, a skew of 1 ps is introduced in the sampling points.

Note that if the FFs use inductive peaking, the 32 inductors required in the PD would increase the distance between the first and last FF to several millimeters and the skew to 10–15 ps. In that case, the jitter tolerance of the circuit would be heavily compromised.

The linear placement of the PD FFs inevitably introduces some skew in the routing of the clock phases. However, the

[6]A VCO having a resonator quality factor of Q takes roughly Q cycles to change its frequency in response to a step on the control voltage.

[7]Unlike the diagram in Fig. 6(a), the eight FFs are actually laid out in a row to allow easier clock distribution.

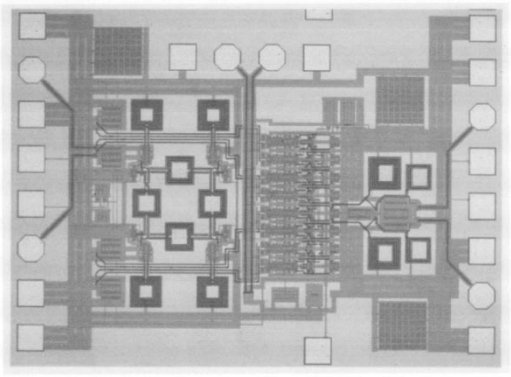


Fig. 14. Chip micrograph.

much narrower width of the clock lines and the absence of a ground plane under them result in a greater group velocity and negligible clock skew.

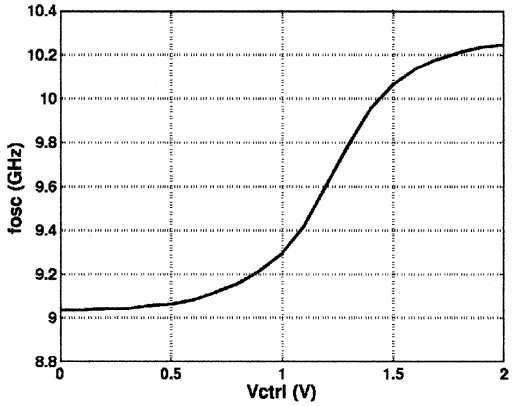
V. Experimental Results

The CDR circuit has been fabricated in a 0.18-μm CMOS technology. Fig. 14 shows a photo of the die, which measures 1.0×1.4 mm^2. The spirals employ a linewidth commensurate with electromigration limitations ($\sim$2 mA/μm for metal-6). The input and output are designed as 50-Ω microstrip structures consisting of metal-6 atop metal-1, and skews are minimized through symmetry in layout. The circuit is tested on a high-speed probe station with a 40-Gb/s Anritsu random data generator providing the input.

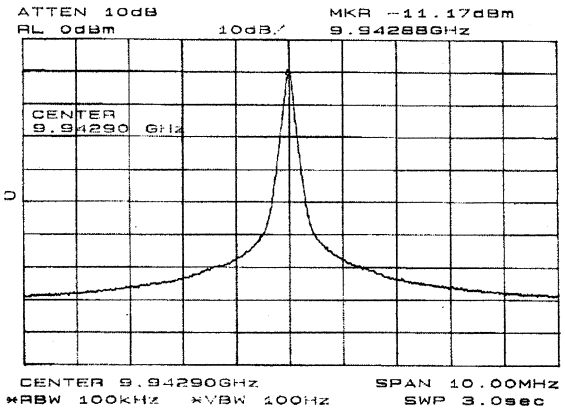
Shown in Fig. 15 are the VCO tuning characteristic and free-running spectrum. The VCO provides a tuning range of 1.2 GHz[8] with a phase noise of -105 dBc/Hz at 1-MHz offset. The Q of the differential inductors used in the VCO is estimated as follows. In the measurement, the oscillator output is monitored on a spectrum analyzer while the tail current of the $-G_m$ cells is reduced so as to place the circuit at the edge of oscillation. Next, the tail current thus obtained is used in the simulation and the equivalent parallel resistance of each inductor R_p is lowered until the circuit fails to oscillate. For such value of R_p, we have $Q = R_p/(L\omega)$. Yielding $Q = 6.5$, this technique of course assumes that the value of the inductor and oscillation frequency are predicted accurately. Note that other oscillator parameters such as phase noise and output swing are also functions of Q, but it is much easier to place the circuit at the edge of oscillation than to calculate the Q from phase noise or output swing measurements.

Fig. 16(a) depicts the CDR input and output waveforms under locked condition in response to a pseudorandom sequence of length $2^{31}-1$. The bit-error rate (BER) is measured using the setup shown in Fig. 16(b), where a high-speed 4-to-1 multiplexer sensing two relatively uncorrelated binary sequences generates a 40-Gb/s stream. One of the demultiplexed channels produced by the CDR circuit corresponds to channel

[8]In a redesign, the VCO inductors must be reduced by approximately 10% to raise the center frequency to 10 GHz.

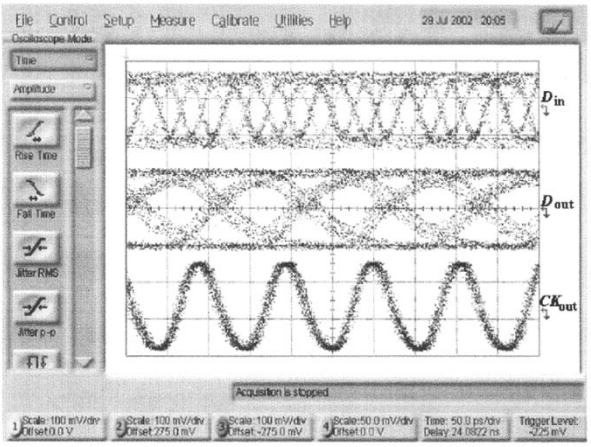


(a)

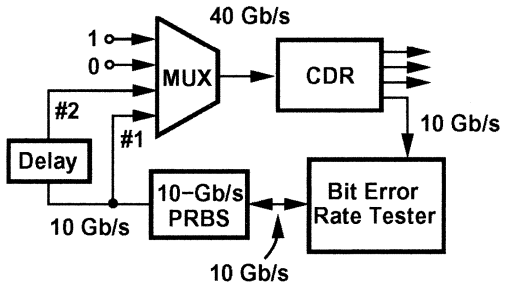


(b)

Fig. 15. VCO. (a) Tuning range. (b) Free-running spectrum.



(a)



(b)

Fig. 16. (a) Input and output waveforms. (Horizontal scale: 50 ps/div, vertical scale: 100 mV/div.) (b) BER test setup.

TABLE I
CDR PERFORMANCE SUMMARY

	[1]	[2]	[11]	This Work
Input Data Rate	40 Gb/s	40 Gb/s	10 Gb/s	40 Gb/s
Output Data Rate	2 x 20 Gb/s	4 x 10 Gb/s	2 x 5 Gb/s	4 x 10 Gb/s
Rec. Clock Jitter	0.8 ps,rms (With 2^7-1 PRBS)	0.7 ps,rms (With $2^{23}-1$ PRBS)	1.2 ps,rms (With $2^{31}-1$ PRBS)	0.9 ps,rms (With $2^{31}-1$ PRBS)
Power Diss.	1.6 W	4.3 W	360 mW	144 mW
BER	N/A	10^{-10}	0	10^{-6}
Sensitivity (single-ended swing)	400 mV	N/A	N/A	400 mV
Supply Voltage	5 V	5 V	1.8 V	2 V
Area	0.9 mm x 0.9 mm	3 mm x 3 mm	1.9 mm x 1.5 mm	1.0 mm x 1.4 mm
Technology	50-GHz Bipolar (Uses external VCO & divider)	72-GHz SiGe	0.18-um CMOS	0.18-um CMOS

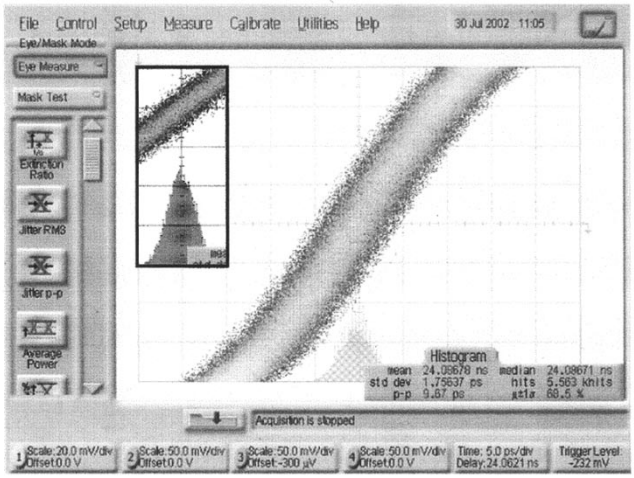


Fig. 17. Clock jitter measurement (horizontal scale: 5 ps/div for both histograms).

1 and is applied to the BER tester.[9] The resulting BER is equal to 10^{-6}. As observed in Fig. 16(a), D_{out} experiences some ISI due to the limited bandwidth of the output buffers, possibly degrading the BER. Other sources of the high BER relate to noise pickup in the probe station and static phase errors in the PD.

Fig. 17 shows the recovered clock, suggesting an rms jitter of 1.756 ps and a peak-to-peak jitter of 9.67 ps. However, as shown in the inset, the oscilloscope itself suffers from rms and peak-to-peak jitters of 1.508 and 8.89 ps, respectively. Thus, the CDR output contains a jitter of 0.9-ps rms and at most 9.67-ps peak-to-peak.[10] The jitter transfer and tolerance have not been measured due to lack of necessary equipment.[11] The performance of this work and some other previously published CDR circuits is summarized in Table I.[12]

VI. CONCLUSION

This work demonstrates the potential of standard CMOS technology for CDR circuits operating at tens of gigabits per second. The proposed oscillator, PD, and FF topologies resolve a number of circuit and architecture issues. Furthermore, the use of inductors boosts the raw speed of the technology considerably. In addition to a high speed, this CDR circuit achieves a power dissipation that is substantially lower than that of previous work.

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[9]This arrangement may be somewhat optimistic in that the multiplexer output does not contain long runs.

[10]It is unclear whether and how the peak-to-peak values can be subtracted.

[11]Integration of the phase noise of the recovered clock from -5-MHz offset to $+5$-MHz offset yields an rms jitter of 0.85 ps.

[12]The power dissipation noted here for the design in [2] excludes their limiting amplifier and frequency detector contribution and was obtained through private communication with the author of [2].

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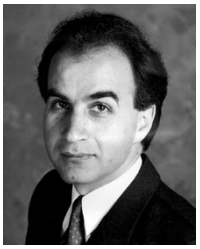

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