A 2.4-GHz 6.4-mW Fractional-N Inductorless RF Synthesizer

Long Kong, *Member, IEEE*, and Behzad Razavi, *Fellow, IEEE*

***Abstract*— A cascaded synthesizer architecture incorporates a digital delay-line-based filter and an analog noise trap to suppress the quantization noise of the $\Sigma\Delta$ modulator. Operating with a reference frequency of 22.6 MHz, the synthesizer achieves a bandwidth of 10 MHz in the first loop and 12 MHz in the second, heavily suppressing the phase noise of its constituent ring oscillators. Realized in 45-nm digital CMOS technology, the synthesizer exhibits an in-band phase noise of −109 dBc/Hz and an integrated jitter of 1.68 ps_{rms}.**

***Index Terms*— $\Sigma\Delta$ noise, cascaded phase-locked loop (PLL), fractional-*N* synthesizer, noise filter, noise trap, PLL.**

I. Introduction

RF SYNTHESIS using ring oscillators, rather than *LC* oscillators, benefits from several advantages: compact, multi-band designs, less coupling to and from other circuits, and the availability of multiple phases. It has been demonstrated that a certain phase-locked loop (PLL) architecture achieves a closed-loop bandwidth around $f_{REF}/2$ [1], thus suppressing the phase noise of a ring oscillator to the level necessary for 2.4-GHz WiFi standards such as IEEE 802.11g. [In such standards, the phase noise is typically determined by the signal constellation quality rather than by reciprocal mixing, i.e., the primary figure of merit (FoM) is the integrated jitter.] The natural question is how the architecture can accommodate fractional-*N* operation.

The design of fractional-*N* synthesizers generally faces two basic issues, namely, the phase noise peaking due to the $\Sigma\Delta$ modulator's shaped quantization noise and the noise folding caused by the charge pump (CP) nonlinearity. The former is typically tackled by choosing a narrow loop bandwidth, around $f_{REF}/740$ to $f_{REF}/200$ [2]–[4], an impractical remedy if we wish to rely on the loop to suppress the VCO phase noise. The latter is addressed through the use of current or timing offset techniques [5], [6].

This paper proposes a cascaded PLL architecture that performs fractional-*N* synthesis and yet achieves such a wide bandwidth as to allow the use of ring oscillators [7]. The in-band phase noise performance approaches that of the prior *LC*-oscillator-based work.

Manuscript received November 11, 2016; revised February 1, 2017 and March 14, 2017; accepted March 20, 2017. Date of publication April 24, 2017; date of current version July 20, 2017. This paper was approved by Associate Editor Woogeun Rhee. This work was supported in part by the Qualcomm Innovation Fellowship Program, in part by Broadcom Fellowship Program, and in part by Realtek Semiconductor. *(Corresponding author: Long Kong.)*

L. Kong was with the Electrical Engineering Department, University of California, Los Angeles, CA 90095 USA, and is now with Oracle, Santa Clara, CA 95054 USA (e-mail: longkong@ucla.edu).

B. Razavi is with the Electrical Engineering Department, University of California, Los Angeles, CA 90095 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2017.2686838

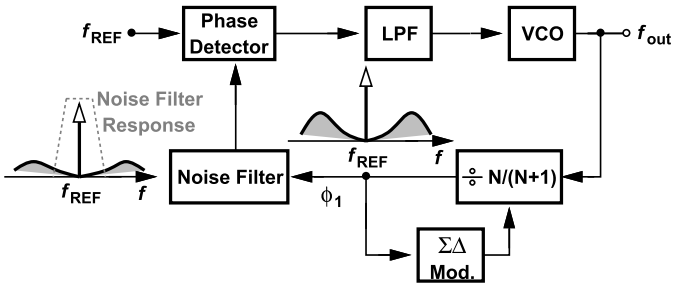


Fig. 1. Conceptual synthesizer with noise filter.

II. Prior Art

Two general approaches to $\Sigma\Delta$ noise cancellation can be identified in the prior art. The first incorporates a feedforward DAC to inject into the loop filter the negative of the $\Sigma\Delta$ noise traveling through the CP. This method relies on matching between the CP and the DAC current sources and, more importantly, assumes both the CP and the DAC are linear enough to negligibly fold down the high-frequency shaped noise of the $\Sigma\Delta$ modulator [8]. Various noise cancellation techniques have been developed to achieve better performance [9]–[11], but they require stringent matching or complex calibration while still imposing a narrow-loop bandwidth.

The second approach realizes an equivalent FIR filtering action on the $\Sigma\Delta$ noise through the use of multiple paths, each consisting of a feedback divider, a phase/frequency detector (PFD), and a CP [12]. In addition to a high power consumption, this architecture also demands linear CPs as they carry the unfiltered $\Sigma\Delta$ noise and perform the FIR summing function at their *outputs*, unless a large number of CPs are used to benefit from averaging. A related topology [13] avoids multiple paths while utilizing a phase interpolator, but still needs to deal with the mismatch between current sources in the interpolator.

III. Proposed Architecture

A. Noise Filter in Feedback Path

It is highly desirable to suppress the $\Sigma\Delta$ noise before it reaches a potentially nonlinear stage. In this spirit, let us place a noise filter immediately after the feedback divider (Fig. 1), surmising that if the filter attenuates the phase noise peaks below and above f_{REF}, then the loop bandwidth can be increased.

The bandpass noise filter can be implemented in analog or digital forms, but it must satisfy five conditions: 1) its

center frequency must be close enough to f_{REF}; 2) it must have a steep roll-off so as to provide an attenuation of more than 80 dB at $f_{REF} \pm f_{REF}/2$; 3) it must contribute negligible noise; 4) it must be linear enough to avoid noise folding; and 5) it must not limit the loop bandwidth or degrade the stability.

The first four issues preclude an analog implementation and the last issue merits some analysis. The passband of the filter must be chosen such that the integrated $\Sigma\Delta$ noise within the bandwidth is not prohibitively large. For a third-order $\Sigma\Delta$ modulator with a 1-b quantizer, the noise is given by

$$P_n = 2S_Q(f)\int_0^{f_{BW}} 4\pi^2\left[2\sin\left(\frac{\pi f}{f_{REF}}\right)\right]^4 df = \frac{\pi^2}{3}\left[\frac{6f_{BW}}{f_{REF}} - \frac{4}{\pi}\sin\left(2\pi\frac{f_{BW}}{f_{REF}}\right) + \frac{1}{2\pi}\sin\left(4\pi\frac{f_{BW}}{f_{REF}}\right)\right] \quad (1)$$

where $S_Q(f)$ denotes the unshaped quantization noise spectrum and f_{BW} the filter bandwidth. For P_n to be less than -50 dBc, we require that f_{BW} to be smaller than approximately $f_{REF}/40$.

We thus conclude that a filter that sufficiently rejects the $\Sigma\Delta$ noise also severely limits the loop bandwidth. Let us accept this constraint for now and deal with the implementation of the filter, recognizing that the divider output in Fig. 1 is a digital signal and we are only interested in the output *phase*, ϕ_1. Seeking a digital solution, we delay this output to obtain ϕ_2 and add ϕ_2 to ϕ_1 [Fig. 2(a)]. If the delay is long enough to invert the phase noise components of interest, then $\phi_1 + \phi_2$ contains less noise. Mathematically, for a delay of T_D seconds, the filter transfer function is given by

$$\frac{\phi_{filt}}{\phi_1}(s) = 1 + \exp(-T_D s). \quad (2)$$

For $s = j\omega$, we have

$$\frac{\phi_{filt}}{\phi_1}(j\omega) = 2e^{-j\pi f T_D}\cos(\pi f T_D) \quad (3)$$

which exhibits notches at $f = (2n+1)/(2T_D)$ for $n = 0, 1, \ldots$ [Fig. 2(b)]. The voltage transfer function has the same shape, but it is centered around f_{REF}.

The exemplary response plotted in Fig. 2(b) exhibits peaks equal to 2.0 between the notches and little roll-off up to about 40% of the first notch frequency, $1/(2T_D)$. According to our previous calculations, this notch must be placed around $f_{REF}/40$ to attenuate the $\Sigma\Delta$ noise sufficiently. For a typical value of $f_{REF} \approx 20$ MHz in WiFi applications, $f_{REF}/40 = 1/(2T_D)$ translates to $T_D \approx 1000$ ns, posing formidable challenges in the design of the delay line. In particular, if, for example, such a large T_D is realized by a chain of about 100 000 inverters, the power consumption and phase noise of the delay line become prohibitive. Moreover, the high peaks of the response in Fig. 2(b) still give rise to substantial unfiltered $\Sigma\Delta$ noise. We deal with the delay issue in the next two sections and with the peaks in Section V-A.

B. Synchronous Delay Line

In order to avoid the foregoing tradeoffs among delay, power consumption, and phase noise, we utilize a synchronous delay line, i.e., a chain of flip-flops. If clocked by the 2.4-GHz VCO output, each flip-flop contributes a delay of 417 ps, about a factor of 40 greater than does an inverter. As illustrated in Fig. 3(a), the idea is to realize a total delay of $\Delta T = kT_{VCO}$, where k is the number of flip-flops and T_{VCO} is the VCO period. An important advantage of this approach is that the clocking removes phase noise accumulation within the delay line; however, the power consumed in the clock path of the flip-flops must be managed. Specifically, for $T_D \approx 1000$ ns, the design still demands about 2400 flip-flops, potentially drawing a high power. It is possible to clock the flip-flops by a subharmonic of the VCO output so as to increase the delay, but such a scheme would "miss" some phase jumps at the divider output, increasing the phase noise.

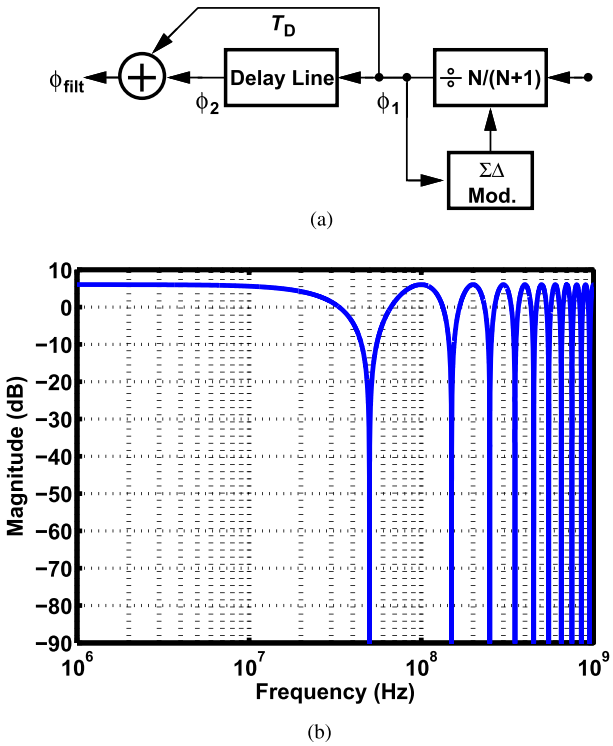
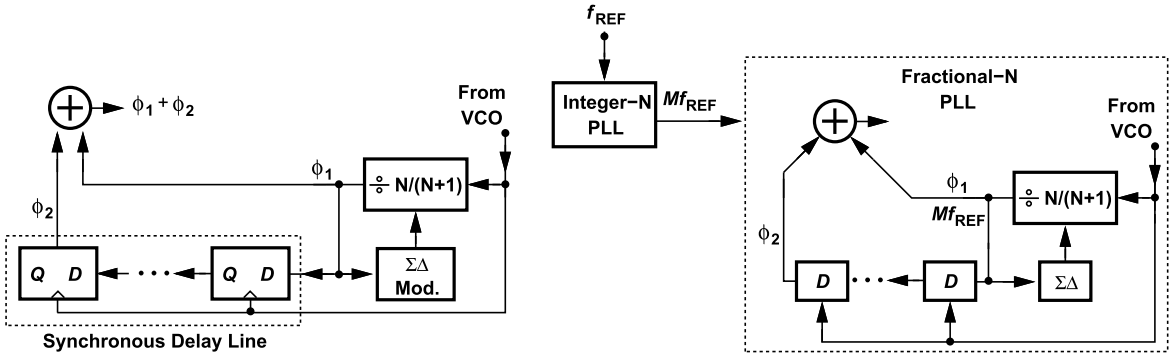


Fig. 2. (a) Noise filter architecture and (b) exemplary response with $T_D = 10$ ns.

C. Cascaded PLLs

We now address the problem of the large number of flip-flops necessary in the noise filter. We can reduce the number of flip-flops by a factor of M if f_{REF} is scaled up by the same factor. This can be seen from (1), where $S_Q(f)$ is inversely proportional to the reference frequency. To this end, we insert an integer-N PLL before the fractional-N loop [Fig. 3(b)]. Since N cannot be less than 2 in the latter, M has an upper bound of about 50. The first PLL multiplies $f_{REF} \approx 20$ MHz up to about 1 GHz, allowing the $\Sigma\Delta$ modulator to operate at this frequency. Our rule of thumb of filter BW $= f_{REF}/40$ thus requires that we place the first notch at 1 GHz/40 = 25 MHz, which translates to 48 flip-flops running at 2.4 GHz. In practice, the $\Sigma\Delta$ noise is also suppressed by the filter preceding the VCO, and hence, the notch can be around 50 MHz and



(a) (b)

Fig. 3. (a) Noise filter with synchronous delay line and (b) conceptual diagram of cascaded fractional-N synthesizer.

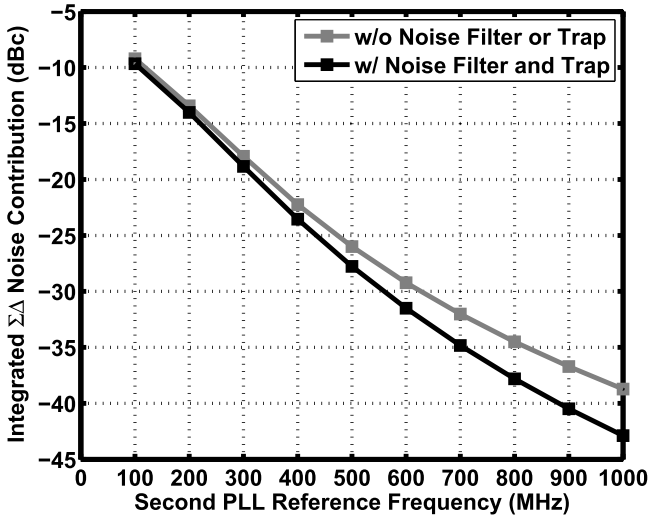


Fig. 4. Integrated $\Sigma\Delta$ noise contribution versus second PLL reference frequency.

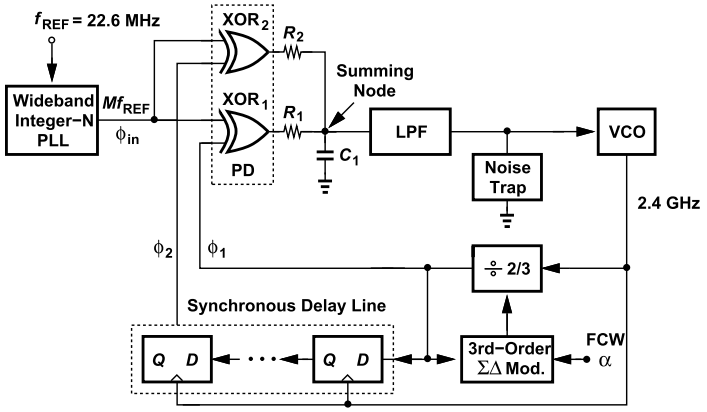


Fig. 5. Proposed fractional-N synthesizer architecture.

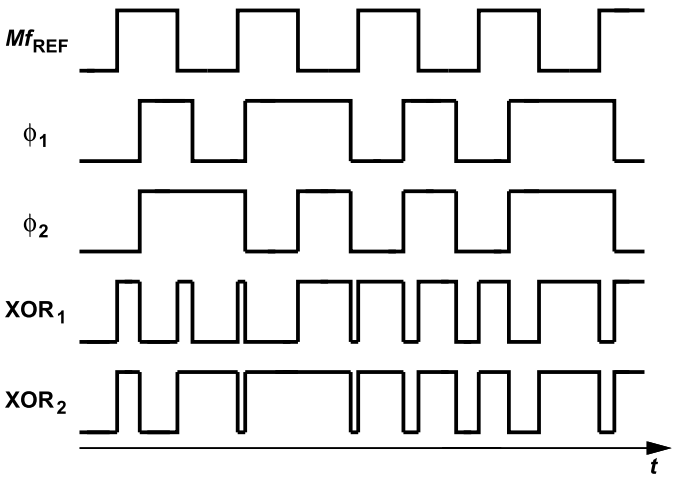


Fig. 6. XOR PDs' waveforms.

the number of flip-flops can be about 24. Of course, the $\Sigma\Delta$ modulator now runs at 1 GHz and can draw substantial power. However, the high oversampling ratio dramatically reduces the $\Sigma\Delta$ noise contribution, as shown in Fig. 4. As the second PLL reference frequency increases from 100 MHz to 1 GHz, the integrated noise drops by around 30 dB. With the noise filter and a "trap" on the control voltage (Section V-A), it is further reduced by 4 dB, reaching -43 dBc.

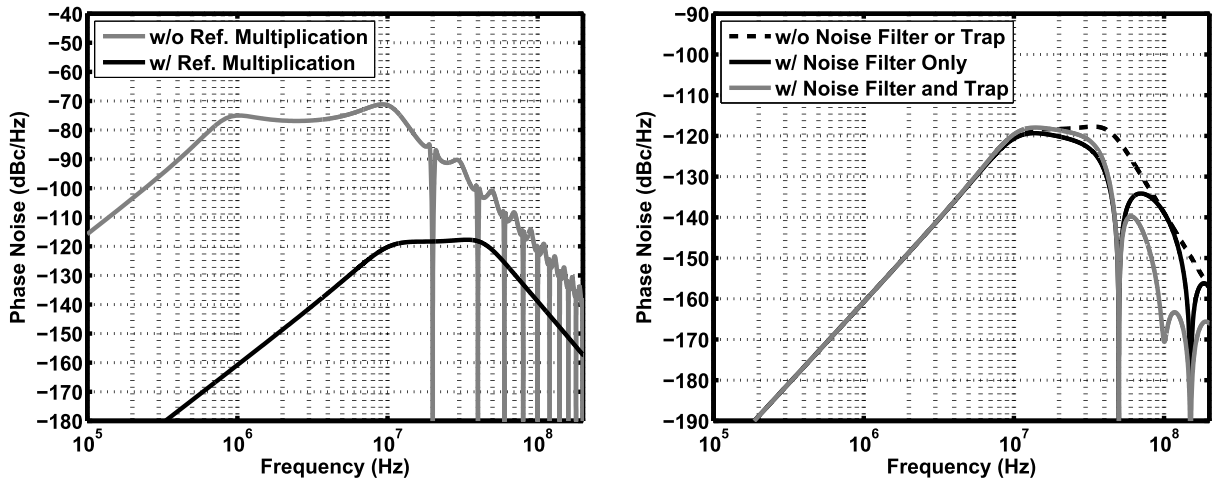
The cascading depicted in Fig. 3(b) relies on ring VCOs in both loops, assuming that acceptably low-phase noise and power dissipation can be achieved for the overall design. We return to this point in Section V-B.

D. Overall Architecture

Fig. 5 shows the overall synthesizer architecture. The fractional-N loop consists of a summing phase detector, a low-pass filter, a noise trap, a VCO, and the feedback topology developed in Fig. 3. We elaborate on four aspects of this loop. We should note that the design in [15] also employs cascaded PLLs but with an LC-VCO and a fractional-N loop bandwidth of around 1/800 times its input frequency.

First, to produce $\phi_1+\phi_2$, we first compute $\phi_{in}-\phi_1$ and $\phi_{in}-\phi_2$ by means of XOR$_1$ and XOR$_2$, respectively, and then sum the results with the aid of R_1 and R_2. Fig. 6 plots the PDs' waveforms, illustrating that the XORs compute the error between the reference phase and the divider's past output phases.[1] Compared with CPs, the XOR gates exhibit negligible nonlinearity, folding no $\Sigma\Delta$ noise before the cancellation occurs at the summing node. In our prototype design, R_1 and R_2 are chosen to be 4.5 kΩ. In the presence of resistor variation, say 10%, the notch depth of the noise filter is limited to about 26 dB, which is still sufficient for

[1]Since ϕ_1 and ϕ_2 in Fig. 6 can have a phase difference as large as 0.4 ns, interpolation—rather than two XORs—would be prone to noise and jitter.



(a) (b)

Fig. 7. Second PLL $\Sigma\Delta$ phase noise contribution without or with (a) reference multiplication and (b) feedback noise filter and trap.

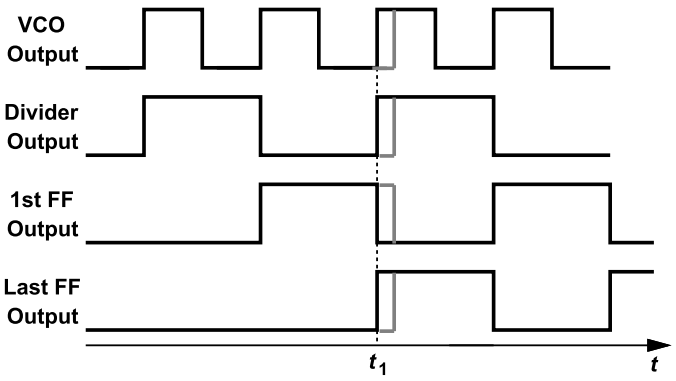
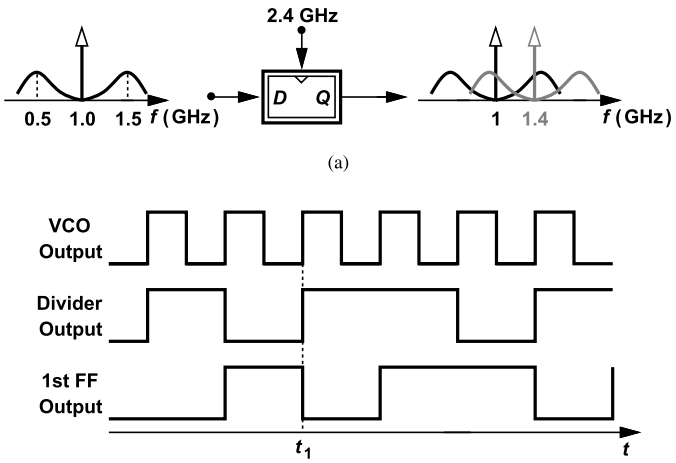


Fig. 8. Time-domain waveforms of VCO, divider, and FF outputs.



(a) (b)

Fig. 9. Illustration of aliasing in the (a) general case and (b) proposed architecture.

quantization noise reduction. Therefore, resistor calibration is not necessary.

Second, while experiencing a notch at an offset frequency of 50 MHz, the $\Sigma\Delta$ noise still travels past the summing junction at the peaks of the response shown in Fig. 2(b). Fig. 7(a) and (b) plot the $\Sigma\Delta$ noise contribution to the second loop in different scenarios: without or with the reference multiplication and without or with the feedback noise filter and a "trap" on the control voltage (Section V-A), respectively.

Third, as mentioned in Section III-A, the noise filter can potentially degrade the PLL's stability. In the proposed architecture of Fig. 5, however, the stability remains intact because the delay line is directly clocked by the VCO. This point can be understood with the aid of Fig. 8. The divider output is delayed by one T_{VCO} by the first FF and by $24T_{\mathrm{VCO}}$ by the entire line. To study the effect of the delay line, suppose the VCO output experiences a small phase step at $t = t_1$. This step simultaneously reaches the outputs of all flip-flops. That is, this step sees only the clock-to-output delay of one FF rather than a value as high as $24T_{\mathrm{VCO}}$. The phase margin is therefore unaffected. This differs from other feedback noise filtering techniques. For example, [14] places a PLL after the feedback divider to suppress the $\Sigma\Delta$ noise, but it faces direct bandwidth limitations and/or stability issues due to this PLL.

Fourth, noting that the divider output in Fig. 5 contains shaped noise with peaks at 1 GHz $\pm$ 500 MHz, we ask whether the delay line flip-flops, clocked at 2.4 GHz, create aliasing. Such a case is depicted in Fig. 9(a). However, this effect is absent in our architecture owing to the timing correlation between the divider output and the delay line clock. Fig. 9(b) illustrates the situation in the time domain, where the divider modulus changes from 2 to 3 at $t = t_1$, forcing the divider to swallow one more VCO cycle. The first FF now samples the divider output and delays it by one T_{VCO}, and the same applies to the remaining FFs. In other words, by virtue of the VCO and divider timing relationship, the delayed signal maintains its shape and duty cycle as it travels through the flip-flops, experiencing no aliasing.

E. Effect of Nonmonotonic PD Behavior

The XOR gates in Fig. 5 act as phase subtractors and exhibit nonmonotonic characteristics that repeat every 2π radians. The

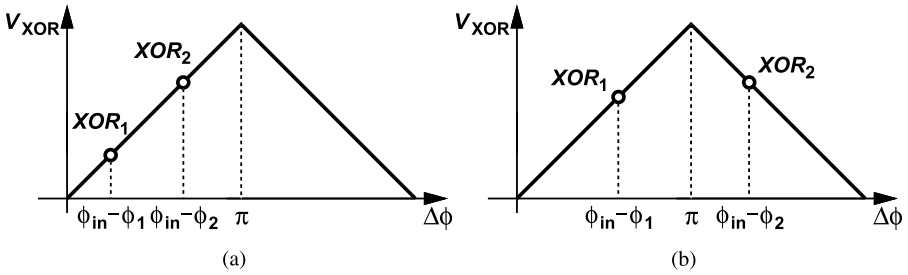


Fig. 10. Phase detector characteristics with (a) XORs on the same slope and (b) XORs on the opposite slopes.

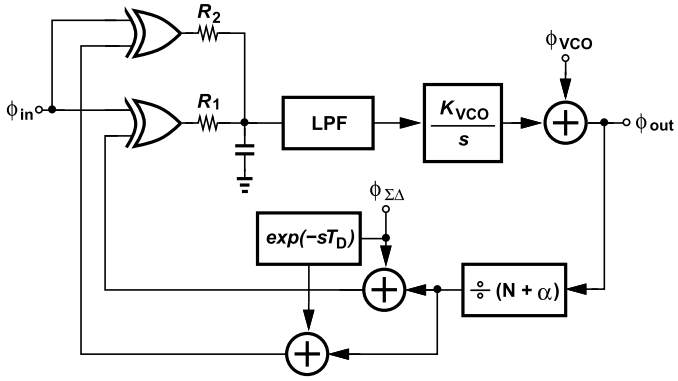


Fig. 11. Small-signal model of the fractional-N loop.

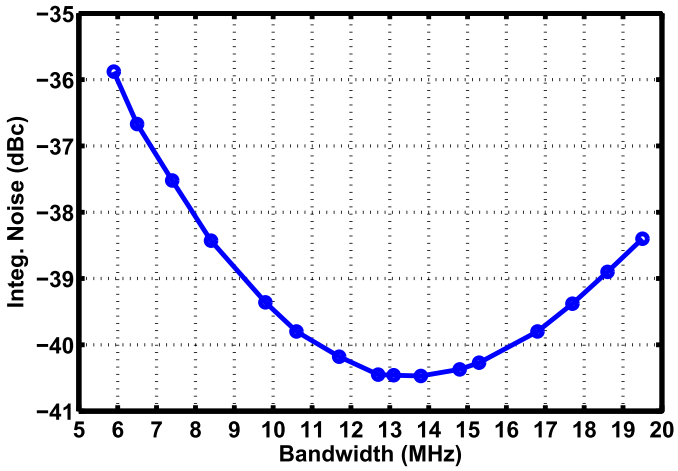


Fig. 12. Integrated phase noise versus loop bandwidth for PLL2.

XORs generate equal dc outputs only if the total filter delay T_D is equal to an integer multiple of the second PLL reference period, T_{REF2}. In the general case, we have

$$T_D = 24T_{VCO} = \frac{24T_{REF2}}{2+\alpha} \tag{4}$$

which means the XOR dc levels are equal only for $\alpha = 0.4$. As α departs from this value, the XORs generate unequal dc outputs, a benign effect so long as their slopes have the same polarity [Fig. 10(a)]. On the other hand, if, for example, α rises to 0.5, T_D and ϕ_2 fall, and $\phi_{in} - \phi_2$ exceeds π [Fig. 10(b)]. With the XORs providing opposite gains, the net loop gain may become excessively small, thereby prohibiting lock.

This issue is alleviated by means of two adjustments in tandem with the desired output frequency. As the frequency varies from 2.4 to 2.48 GHz, the integer-N PLL output frequency is programmed to change from 1 GHz to 1.04 GHz so that the delay value remains close to $10T_{REF2}$. Moreover, the delay line length is also programmed to provide a wider range of delay.

IV. Bandwidth Considerations

The overall phase noise in the architecture of Fig. 5 primarily arises from three sources, namely, the two ring oscillators and the $\Sigma\Delta$ modulator. Chosen wide enough to suppress the second VCO's phase noise, the second loop's bandwidth has little effect on the output phase noise of the first PLL. We therefore focus on the tradeoff between the contributions of the second VCO and the $\Sigma\Delta$ modulator, seeking the optimum bandwidth.

A. Noise Transfer Functions

Shown in Fig. 11 is a small-signal model of the fractional-N loop for calculating the transfer functions to ϕ_{out} from the VCO phase noise, ϕ_{VCO}, and the $\Sigma\Delta$-induced phase noise, $\phi_{\Sigma\Delta}$. Recall from Section III-D that the feedback noise filter does not affect the VCO signal propagation, that is, the loop transmission seen by ϕ_{VCO} is given by

$$H_1(s) = K_{PD}H_{LPF}(s)\frac{K_{VCO}}{(N+\alpha)s} \tag{5}$$

where K_{PD} denotes the PD gain and $H_{LPF}(s)$ the low-pass filter transfer function. It follows that $\phi_{out}/\phi_{in} = (N+\alpha)H_1(s)/[1+H_1(s)]$ and $\phi_{out}/\phi_{VCO} = 1/[1+H_1(s)]$, the same as in conventional PLLs. However, the $\Sigma\Delta$ noise experiences the filter's transfer function; beginning from the output in Fig. 11 and assuming $R_1 = R_2$, we can write

$$-\left(\frac{\phi_{out}}{N+\alpha} + \phi_{\Sigma\Delta}\frac{1+e^{-sT_D}}{2}\right)\frac{K_{PD}K_{VCO}}{s}H_{LPF}(s) = \phi_{out}. \tag{6}$$

This gives

$$\frac{\phi_{out}}{\phi_{\Sigma\Delta}}(s) = -\frac{(N+\alpha)H_1(s)}{1+H_1(s)}\frac{1+e^{-sT_D}}{2}. \tag{7}$$

As expected, this result differs from that of the conventional loop by a factor of $[1+\exp(-sT_D)]/2$, which has a unity peak magnitude. Simulations confirm these observations.

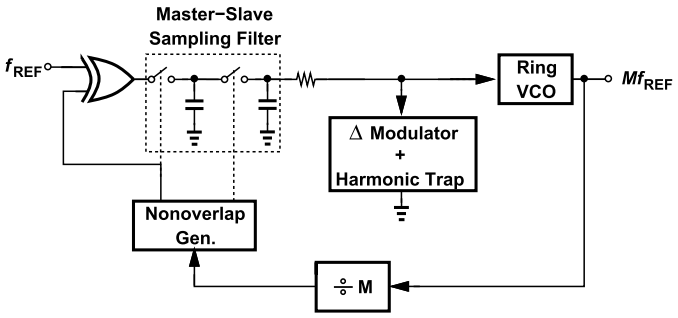


Fig. 13. First stage integer-N PLL architecture.

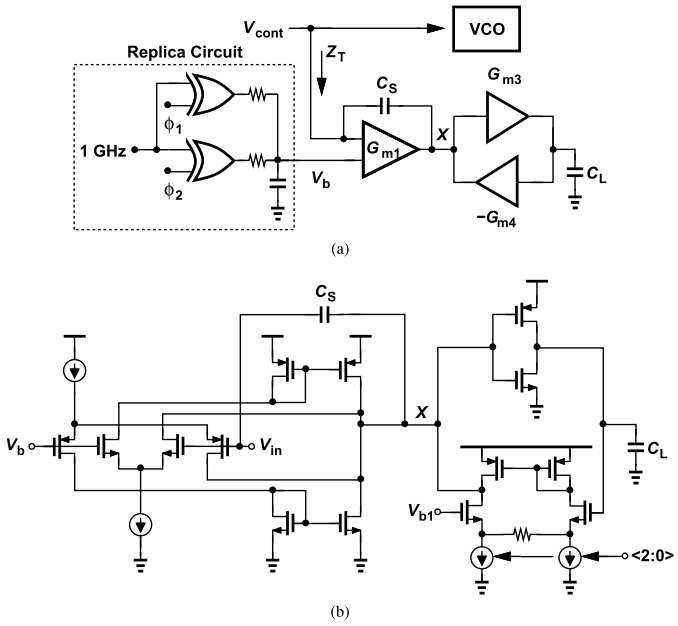


Fig. 14. Noise trap (a) topology and (b) implementation.

B. Optimum Bandwidth

The fractional-N PLL in Fig. 5 can afford a wide loop bandwidth for two reasons: 1) running at 1 GHz, the $\Sigma\Delta$ modulator exhibits a noise peak at 500-MHz offset and hence negligible noise for offsets as high as tens of megahertz, and 2) the feedback noise filter begins to suppress the quantization noise from around 20-MHz offset. Nevertheless, to attenuate the VCO phase noise aggressively, we must determine the optimum loop bandwidth.

As derived in [16], the $\Sigma\Delta$-induced phase noise at the divider output can be expressed as

$$S_{\Sigma\Delta}(f) = \frac{\pi^2}{3(N+\alpha)^2 f_{\text{REF2}}} \frac{1}{|2\sin(\pi f T_{\text{REF2}})|^2} |\text{NTF}(f)|^2 \tag{8}$$

where $\text{NTF}(f)$ denotes the noise transfer function of the $\Sigma\Delta$ modulator and is discussed in Section V-C. We can now write the $\Sigma\Delta$ and VCO noise contributions to the main output as

$$S_{\text{out}}(f) = S_{\Sigma\Delta}(f) \left| \frac{(N+\alpha)H_1(j\omega)}{1+H_1(j\omega)} \frac{1+e^{-j2\pi f T_D}}{2} \right|^2 + S_{\text{VCO}}(f) \frac{1}{|1+H_1(j\omega)|^2}. \tag{9}$$

The area under $S_{\text{out}}(f)$ must be minimized. With the VCO phase noise profile shown in Section V-B and integrating S_{out} from 10 kHz to 100 MHz (where most of the energy lies), we obtain the plot shown in Fig. 12 versus the loop bandwidth. The fractional-N loop must therefore operate with a bandwidth around 13 to 14 MHz. The relatively flat minimum suggests that the architecture has a high tolerance of PVT variations.

V. Building Blocks

In the proposed architecture of Fig. 5, the integer-N loop is similar to that described in [1], but designed for 1 GHz, with a varactor-tuned VCO consuming 2.7 mW. Fig. 13 shows the integer-N PLL architecture [1]. The type-I loop incorporating the master–slave sampling filter achieves a bandwidth close to $f_{\text{REF}}/2$ with a small reference spur. The harmonic trap further reduces the spur by creating a short circuit to ground at the reference frequency. The in-band noise of this PLL is less than -120 dBc/Hz to obtain a sufficient small phase noise at the cascaded synthesizer output, and the reference spur is less than -60 dBc. In the following section, we describe some of the building blocks of the fractional-N loop.

A. Loop Filter and Noise Trap

The loop filter in a fractional-N PLL typically suppresses the $\Sigma\Delta$ noise so as to avoid significant far-out phase noise peaking at the output. However, another important consideration is that the nonlinearity in the VCO control path can fold the $\Sigma\Delta$ noise, causing higher *close-in* phase noise. Whether the first or second consideration dominates the loop filter design depends on how nonlinear the VCO is. In other words, the loop filter bandwidth must be narrow enough to avoid both far-out peaking and close-in aliased phase noise. As explained in Section III-D, though creating periodically spaced notches, our feedback noise filter still exhibits peaks in its response, requiring substantial filtering after the summing junction in Fig. 5.

The low-pass filter in Fig. 5 consists of the section formed by R_1, R_2, and C_1, and four more cascaded RC sections, providing poles at 14.4 MHz, 65.4 MHz, 294 MHz, 659 MHz, and 1.11 GHz.[2] This filter's thermal noise translates to an in-band phase noise of -140 dBc/Hz.

The LPF attenuates the $\Sigma\Delta$ noise voltage excursions to 47.5 mV_{pp}. We achieve additional attenuation through the use of the noise trap in Fig. 5. Acting as a short circuit to ground between the first and second notches of the feedback noise filter, the trap is realized as shown in Fig. 14(a). The trap impedance Z_T is formed by an integrator that is loaded by a simulated inductor [17].

[2]If the second pole is reduced so as to provide significant attenuation at, say, 50 MHz, then it becomes comparable to the first, thus reducing the loop bandwidth.

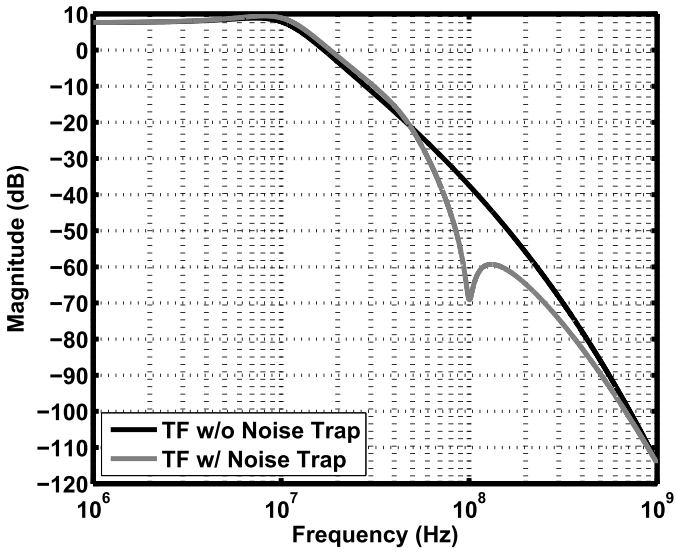


Fig. 15. PLL2 transfer function with and without noise trap.

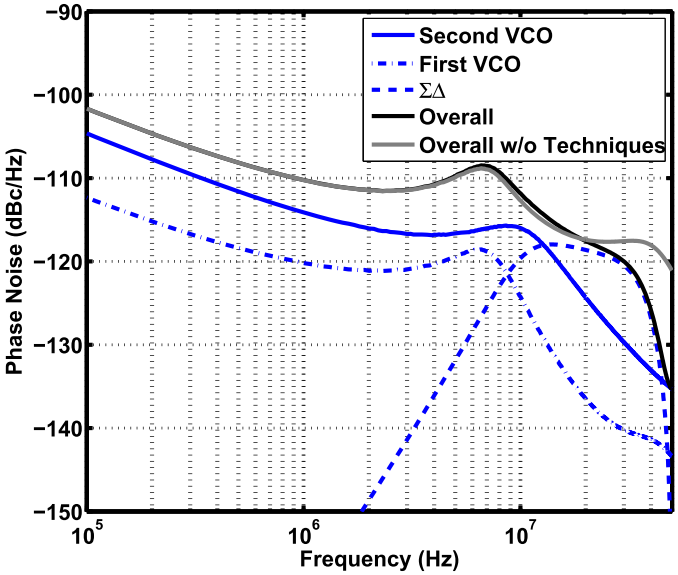


Fig. 16. Overall simulated PLL phase noise and main contributors.

The trap must satisfy four requirements: a high Q so as to provide sufficient suppression, wideband filtering, negligible in-band noise contribution, and the ability to operate across the nearly rail-to-rail control voltage range (as the VCO employs varactor tuning).

It can be shown [17] that Z_T in Fig. 14(a) is given by

$$Z_T(s) = \frac{1 + L_1 C_s s^2}{C_s s(1 + G_{m1} L_1 s)} \tag{10}$$

where $L_1 = C_L/(G_{m3}G_{m4})$. In addition to a notch at $\omega_N = 1/\sqrt{L_1 C_s} = \sqrt{G_{m3}G_{m4}/(C_L C_s)}$, the trap exhibits a real pole at $\omega_P = 1/(G_{m1}L_1)$, which can provide wideband attenuation beyond ω_N. In this design, $G_{m1} = 0.8$ mS, $G_{m3} = 0.4$ mS, $G_{m4} = 0.12$ mS, $C_s = 0.1$ pF, and $C_L = 1.2$ pF, yielding $\omega_N = 2\pi(100$ MHz), $\omega_P = 2\pi(8$ MHz), an active inductance of 25.3 μH, and a Q of 20. The actual Q is about 15 due to the output resistance of G_{m1}. Fig. 15 plots the fractional-N loop's response with and without the trap, revealing an additional attenuation from 60 to 300 MHz. The trap thus reduces the $\Sigma\Delta$ noise by 15 dB at 100 MHz with negligible effect on the loop bandwidth or stability. The total integrated jitter is reduced by 5% due to this trap.

In Fig. 14(a), G_{m1} has differential inputs for robust operation, but the noninverting input must be tied to the dc value of V_{cont}. This dc value V_b is generated by a replica circuit with the same XORs as the main path and also has a bandwidth of only 2 MHz to remove the $\Sigma\Delta$ noise.

Fig. 14(b) shows the noise trap implementation. NMOS and PMOS differential pairs provide a rail-to-rail common-mode range for G_{m1}. Since the trap manifests itself only at high frequencies, and since the fractional-N loop has a small divide ratio, the trap contributes negligible phase noise, about -141 dBc/Hz at a 5-MHz offset.

B. VCO Design

Both VCOs are configured as three-stage varactor-tuned ring oscillators [1]. Since the second PLL has a wider bandwidth, its VCO can be designed for a higher phase noise to save power. The first and second VCOs, respectively, draw 2.7 mW and 2.25 mW at 1 GHz and 2.4 GHz, while exhibiting the phase noises of -108 and -96 dBc/Hz at a 1-MHz offset.

Fig. 16 plots the overall simulated output phase noise along with the contributions from the two VCOs and the $\Sigma\Delta$ modulator. The $\Sigma\Delta$ noise exceeds the shaped ring-VCO noise at a 13-MHz offset. The overall integrated jitter is reduced by 23% with the proposed techniques while consuming only 8% of the total power.

C. Low-Power Digital Design

The $\Sigma\Delta$ modulator in Fig. 5 operates with a clock frequency of 1 GHz. Such a choice demands custom design of the modulator architecture and its constituent circuits so as to achieve an acceptably low power consumption. Since this loop receives a 1-GHz reference, α must have a 20-b word length for a frequency resolution of 1 kHz. A standard third-order modulator would require 70 registers and three 24-bit adders, draining considerable power. Instead, we turn to the "bus-splitting" technique proposed in [15] and [18] to save hardware and power. As shown in Fig. 17, the input drives a cascade of three first-order modulators, which generates a partially shaped output, Y_1. This result is added to the input LSBs, $\langle 12:19\rangle$, and then applied to another single-loop third-order modulator. By comparison, this architecture requires only 50 registers and three 13-b adders.

The modulator of Fig. 17 provides the following noise transfer function:

$$\text{NTF} = \frac{(1 - z^{-1})^3}{1 + z^{-1} - 4z^{-2} + 2.25z^{-3}} \tag{11}$$

which is different from the standard third-order noise shaping. As illustrated in Fig. 18 for FCW = 0.4, the noise spectrum flattens out beyond 50 MHz.

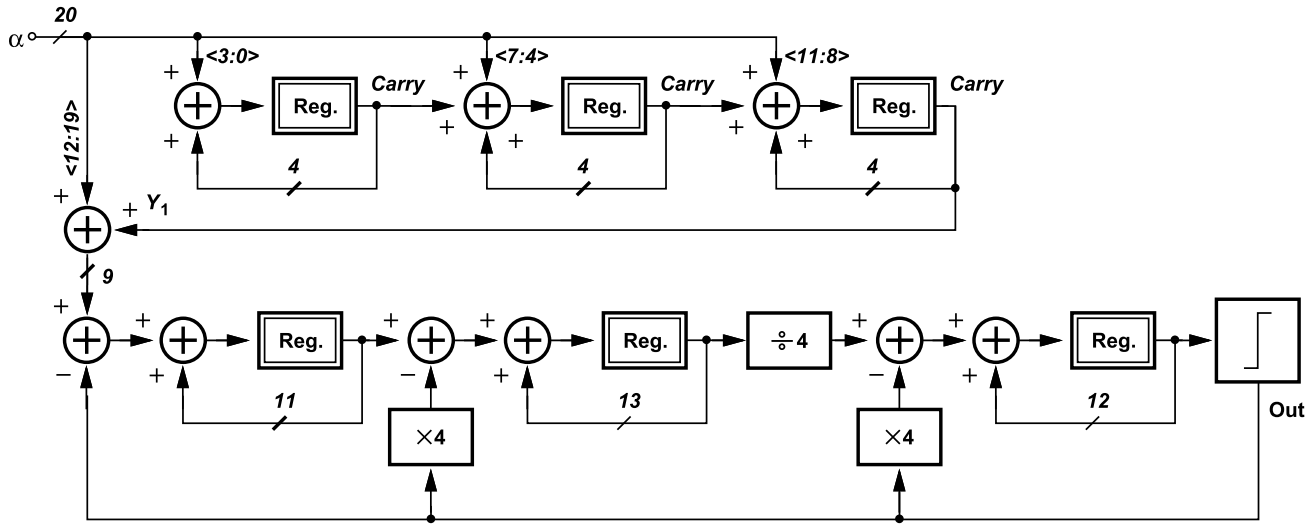


Fig. 17. ΣΔ modulator architecture.

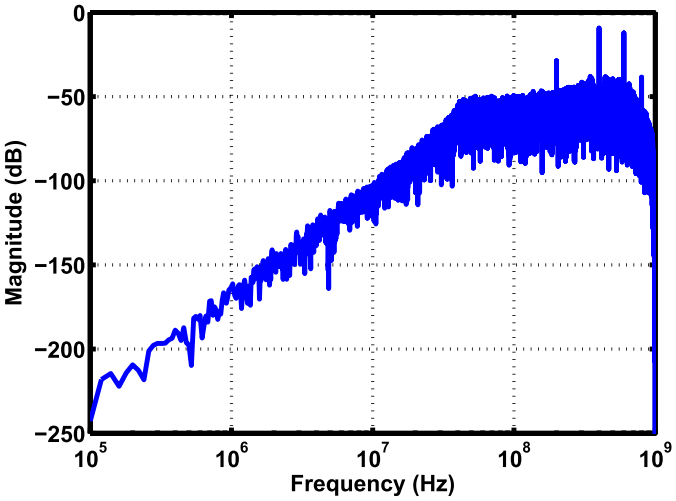


Fig. 18. Simulated spectrum of ΣΔ modulator.

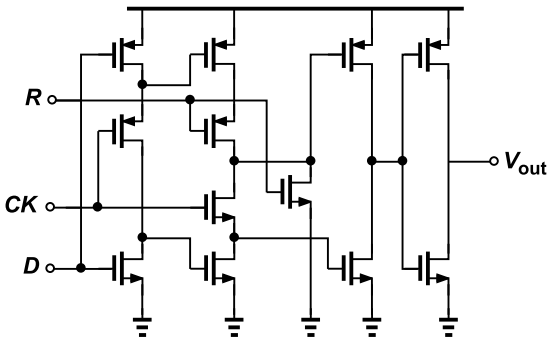


Fig. 19. TSPC FF schematic.

In order to minimize the modulator's power, we have designed and laid out the circuits "by hand" rather than rely on synthesis tools. The registers incorporate TSPC flip-flops [19] with a reset input (Fig. 19). The overall ΣΔ modulator draws 500 μW at 1 GHz. By virtue of the highly digital noise filter and the low-power techniques used in the 1-GHz ΣΔ modulator, the second fractional-N loop itself achieves 1.27 ps_{rms} jitter with only a 3.3-mW power consumption, yielding an FoM of −232.7 dB.

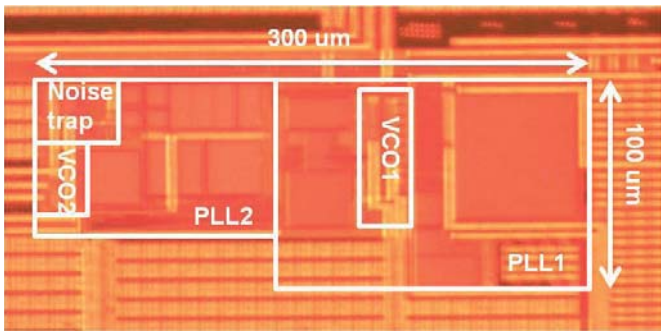


Fig. 20. Die micrograph.

VI. Experimental Results

The cascaded synthesizer has been fabricated in TSMC's 45-nm digital CMOS technology. Shown in Fig. 20 is the die micrograph, with an active area of 300 μm ×100 μm. The prototype operates with a 22.6-MHz crystal oscillator as the reference and generates an output from 2.3 GHz to 2.6 GHz. From a 1-V supply, the first PLL consumes 3.1 mW and the second dissipates 3.3 mW, with 2.25 mW in the second VCO, 0.5 mW in the ΣΔ modulator and divider, 0.35 mW in the feedback noise filter, and 0.2 mW in the noise trap.

Fig. 21 shows the measured output spectra before and after the feedback noise filter and the noise trap are turned ON. In this test, the first and second loops' divide ratios are equal to 45 and 2.3346, respectively. As can be seen, the Δ−Σ contribution is suppressed by 17 dB at a 50-MHz offset. The highest reference spur lies at $2f_{REF}$ offset and is around −70 dBc.

Fig. 22 plots the measured phase noise of the first PLL, revealing an in-band value of around −120.4 dBc/Hz. Fig. 23

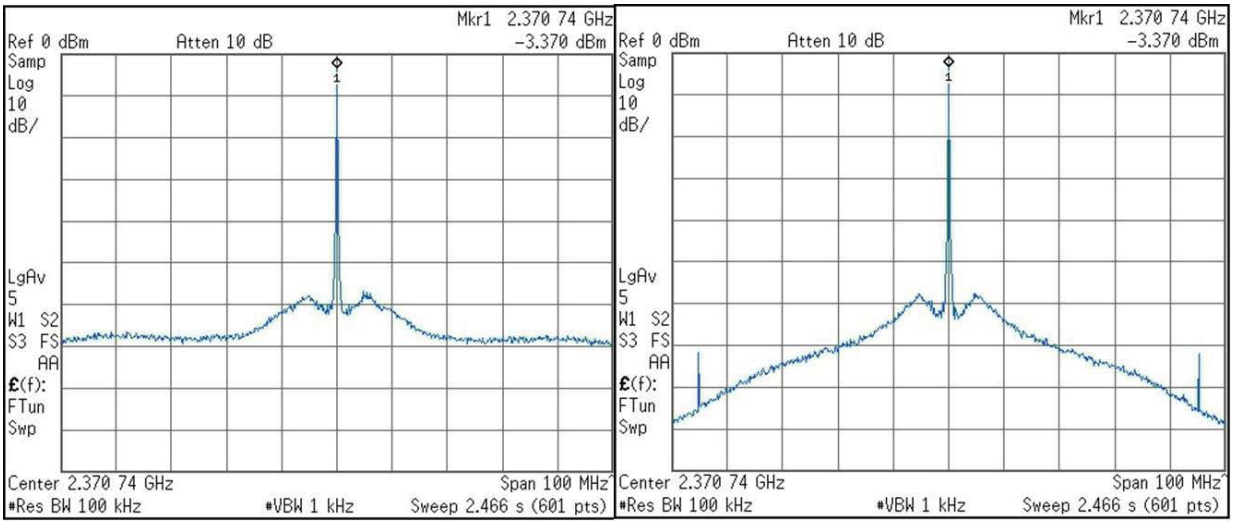


Fig. 21. Measured output spectra before (left) and after (right) noise filter and noise trap are turned ON.

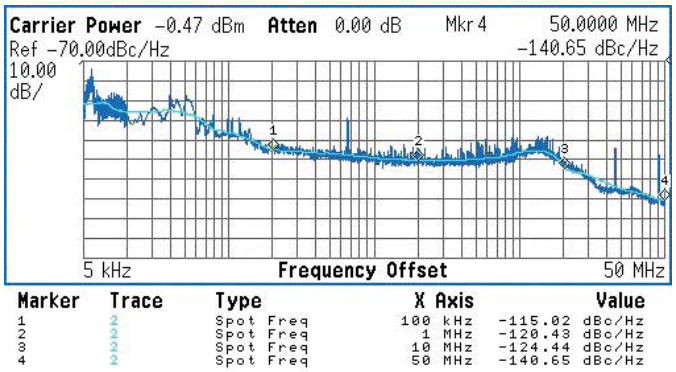


Fig. 22. Measured first PLL phase noise at 1.016 GHz.

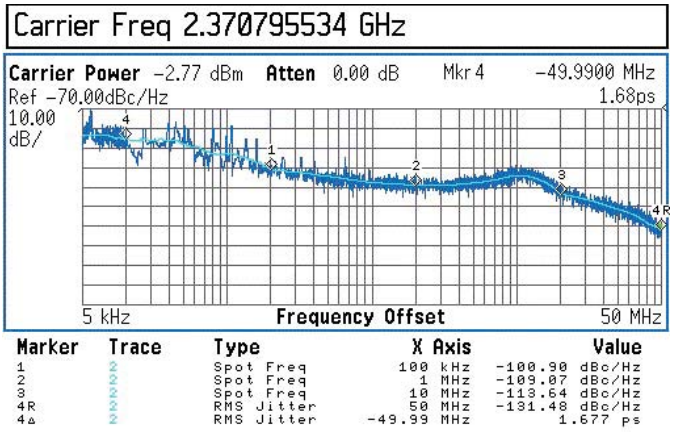


Fig. 23. Measured overall synthesizer output phase noise.

plots the overall synthesizer output phase noise. The in-band plateau is at −109 dBc/Hz and the integrated jitter from 10 kHz to 50 MHz is equal to 1.68 ps_{rms}. The measured phase noise matches well with the simulated one as shown in Fig. 16. Also plotted in Fig. 24 is the highest in-band

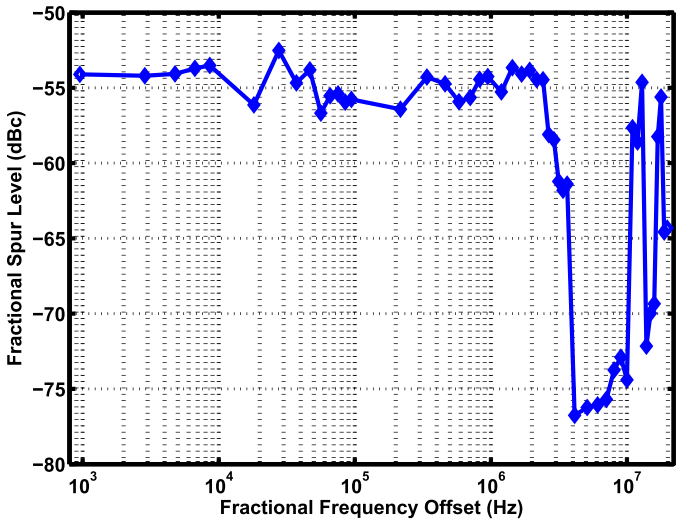


Fig. 24. Measured fractional spur versus frequency offset.

fractional spur level as a function of the fractional frequency offset. The largest spur is at −52.5 dBc, which satisfies IEEE 802.11a/g and Bluetooth blocking requirements. Fig. 25 shows a representative PLL output spectrum with fractional spurs.

Table I summarizes the measured performance of our proposed architecture and compares it to that of state-of-the-art fractional-N synthesizers in the range of 1.9 GHz–2.4 GHz. Our in-band noise is 11-dB lower than ring-VCO-based designs and our FoM approaches that of the LC-VCO-based work in [21] if we consider the twofold difference in the reference frequencies.

VII. Conclusion

This paper introduces a cascaded fractional-N synthesizer targeting 2.4-GHz RF standards without the use of LC oscillators and CPs. In order to suppress the $\Sigma\Delta$ noise while

TABLE I
PERFORMANCE SUMMARY

	ISSCC'13 [20]	JSSC'14 [21]	ISSCC'15 [22]	This Work
Oscillator Topology	Ring	LC	Ring	Ring
Reference Freq. (MHz)	26	48	26	22.6
Frequency Range (GHz)	1.87 ~ 1.98	2.12 ~ 2.4	2	2.3 ~ 2.6
f_{BW}/f_{REF}	0.077	0.01	0.058	0.44 (first PLL) 0.012 (second PLL)
Phase Noise @ 1MHz offset (dBc/Hz)	−98	−114	−98	−109
RMS Jitter (ps) Integ. range (MHz)	3.4 (0.004~2)	0.36 (0.01~30)	2.36 (0.001~40)	1.68 (0.01~50)
In−band Frac. Spur (dBc)	−50	−48	−70	−52.5
Ref. Spur (dBc)	−67	−55	−87	−70
Power (mW)	10	17.3	9.1	6.4
Area (mm^2)	0.047	0.75	0.046	0.03
Tech. (nm)	40	180	40	45
FoM_1 (dB)	−219.4	−236.5	−223	−227.4
FoM_2 (dB)	153.9	168.7	154.4	168.4

$$FoM_1 = 10\log_{10}\left[\left(\frac{\text{Jitter}}{1\text{ s}}\right)^2\left(\frac{\text{Power}}{1\text{ mW}}\right)\right] \quad FoM_2 = 10\log_{10}\left[\left(\frac{f_{osc}}{\Delta f}\right)^2\left(\frac{1\text{ mW}}{\text{Power}}\right)\right] - \text{Phase Noise (dBc/Hz)}$$

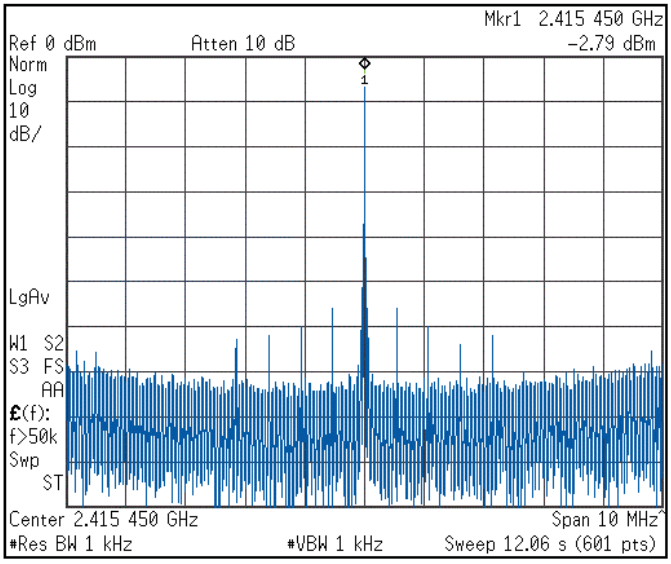


Fig. 25. PLL output spectrum with fractional spurs.

maintaining a moderate loop bandwidth, this paper employs a feedback noise filter in the second loop. The overall performance suggests promising results for inductorless synthesizers.

ACKNOWLEDGMENT

The authors would like to thank the TSMC University Shuttle Program for the chip fabrication.

REFERENCES

[1] L. Kong and B. Razavi, " A 2.4 GHz 4 mW integer-N inductorless RF synthesizer," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 626–635, Mar. 2016.

[2] B. D. Muer and M. S. J. Steyaert, "A CMOS monolithic ΔΣ-controlled fractional-N frequency synthesizer for DCS-1800," *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 835–844, Jul. 2002.

[3] W. Rhee, B.-S. Song, and A. Ali, "A 1.1-GHz CMOS fractional-N frequency synthesizer with a 3-b third-order ΔΣ modulator," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1453–1460, Oct. 2000.

[4] S.-A. Yu and P. Kinget, "A 0.65-V 2.5-GHz fractional-N synthesizer with two-point 2-Mb/s GFSK data modulation," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2411–2425, Sep. 2009.

[5] K. J. Wang, A. Swaminathan, and I. Galton, "Spurious tone suppression techniques applied to a wide-bandwidth 2.4 GHz fractional-N PLL," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2787–2797, Dec. 2008.

[6] Z. Tang, X. Wan, M. Wang, and J. Liu, "A 50-to-930 MHz quadrature-output fractional-N frequency synthesizer with 770-to-1860 MHz single-inductor LC-VCO and without noise folding effect for multistandard DTV tuners," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 358–359.

[7] L. Kong and B. Razavi, "A 2.4-GHz 6.4-mW fractional-N inductorless RF synthesizer," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2016, pp. 236–237.

[8] S. Pamarti, L. Jansson, and I. Galton, "A wideband 2.4-GHz delta-sigma fractional-NPLL with 1-Mb/s in-loop modulation," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 49–61, Jan. 2004.

[9] S. E. Meninger and M. H. Perrott, "A 1-MHZ bandwidth 3.6-GHz 0.18-μm CMOS fractional-N synthesizer utilizing a hybrid PFD/DAC structure for reduced broadband phase noise," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 966–980, Apr. 2006.

[10] M. Gupta and B.-S. Song, "A 1.8-GHz spur-cancelled fractional-N frequency synthesizer with LMS-based DAC gain calibration," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2842–2851, Dec. 2006.

[11] A. Swaminathan, K. J. Wang, and I. Galton, "A wide-bandwidth 2.4 GHz ISM band fractional-N PLL with adaptive phase noise cancellation," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2639–2650, Dec. 2007.

[12] X. Yu, Y. Sun, W. Rhee, and Z. Wang, "An FIR-embedded noise filtering method for ΔΣ fractional-N PLL clock generators," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2426–2436, Sep. 2009.

[13] D.-W. Jee, Y. Suh, B. Kim, H.-J. Park, and J.-Y. Sim, "A FIR-embedded phase interpolator based noise filtering for wide-bandwidth fractional-N PLL," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2795–2804, Nov. 2013.

[14] P. Park, D. Park, and S. Cho, "A 2.4 GHz fractional-N frequency synthesizer with high-OSR ΔΣ modulator and nested PLL," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2433–2443, Oct. 2012.

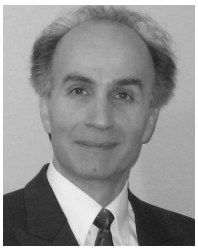
[15] D. Park and S. Cho, "A 14.2 mW 2.55-to-3 GHz Cascaded PLL With Reference Injection and 800 MHz Delta-Sigma Modulator in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2989–2998, Dec. 2012.

[16] M. H. Perrott, M. D. Trott, and C. G. Sodini, "A modeling approach for $\Sigma - \Delta$ fractional-N frequency synthesizers allowing straightforward noise analysis," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1028–1038, Aug. 2002.
[17] A. Zolfaghari and B. Razavi, "A low-power 2.4-GHz transmitter/receiver CMOS IC," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 176–183, Feb. 2003.
[18] B. Fitzgibbon, M. P. Kennedy, and F. Maloberti, "Hardware reduction in digital delta-sigma modulators via bus-splitting and error masking—Part II: Non-Constant Input," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 9, pp. 1980–1991, Sep. 2012.
[19] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," *IEEE J. Solid-State Circuits*, vol. 24, no. 1, pp. 62–70, Feb. 1989.
[20] T.-K. Kao, C.-F. Liang, H.-H. Chiu, and M. Ashburn, "A wideband fractional-N ring PLL with fractional-spur suppression using spectrally shaped segmentation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 416–417.
[21] W. S. Chang, P. C. Huang, and T. C. Lee, "A fractional-N divider-less phase-locked loop with a subsampling phase detector," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2964–2975, Dec. 2014.
[22] C.-F. Liang and P.-Y. Wang, "A wideband fractional-N ring PLL using a near-ground pre-distorted switched-capacitor loop filter," in *ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

Long Kong (M'16) received the B.S. degree in microelectronics from Shanghai Jiao Tong University, Shanghai, China, in 2011, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Los Angeles, CA, USA, in 2013 and 2016, respectively.

Since 2016, he has been a Senior Engineer with the Mixed-Signal Design Group, Oracle, Santa Clara, CA, USA. His research interest includes frequency synthesizers, high-precision on-chip measurement circuits, clock recovery for data communication systems, and wireline transceivers.

Dr. Kong was a recipient of the Qualcomm Innovation Fellowship (2013–2014), the Analog Devices Outstanding Student Designer Award (2015), and the Broadcom Fellowship (2015–2016).



Behzad Razavi (F'03) received the B.S.E.E. degree from the Sharif University of Technology, Tehran, Iran, in 1985, and the M.S.E.E. and Ph.D.E.E. degrees from Stanford University, Stanford, CA, USA, in 1988 and 1992, respectively.

He was an Adjunct Professor with Princeton University, Princeton, NJ, USA, from 1992 to 1994, and with Stanford University in 1995. He was with the AT&T Bell Laboratories and Hewlett-Packard Laboratories until 1996. Since 1996, he has been an Associate Professor and subsequently a Professor of Electrical Engineering with the University of California, Los Angeles, CA, USA. He has authored *Principles of Data Conversion System Design* (IEEE Press, 1995), *RF Microelectronics* (Prentice Hall, 1998, 2012) (translated to Chinese, Japanese, and Korean), *Design of Analog CMOS Integrated Circuits* (McGraw-Hill, 2001, 2016) (translated to Chinese, Japanese, and Korean), *Design of Integrated Circuits for Optical Communications* (McGraw-Hill, 2003; Wiley, 2012), and *Fundamentals of Microelectronics* (Wiley, 2006) (translated to Korean and Portuguese), and has edited *Monolithic Phase-Locked Loops and Clock Recovery Circuits* (IEEE Press, 1996), and *Phase-Locking in High-Performance Systems* (IEEE Press, 2003). His current research includes wireless transceivers, frequency synthesizers, phase-locking and clock recovery for high-speed data communications, and data converters.

Prof. Razavi is a member of the U.S. National Academy of Engineering. He was a recipient of the Beatrice Winner Award for Editorial Excellence at the 1994 ISSCC, the Best Paper Award at the 1994 European Solid-State Circuits Conference, the Best Panel Award at the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, the Best Paper Award at the IEEE Custom Integrated Circuits Conference in 1998, the McGraw-Hill First Edition of the Year Award in 2001, the 2012 Donald Pederson Award in Solid-State Circuits, the American Society for Engineering Education PSW Teaching Award in 2014, the Lockheed Martin Excellence in Teaching Award in 2006, the UCLA Faculty Senate Teaching Award in 2007, and the CICC Best Invited Paper Award in 2009 and in 2012. He was a co-recipient of the Jack Kilby Outstanding Student Paper Award, the Beatrice Winner Award for Editorial Excellence at the 2001 ISSCC, the 2012 and the 2015 VLSI Circuits Symposium Best Student Paper Awards, and the 2013 CICC Best Paper Award. He has served as an IEEE Distinguished Lecturer. He was also recognized as one of the top 10 authors in the 50-year history of ISSCC. He served on the Technical Program Committees of the International Solid-State Circuits Conference from 1993 to 2002 and VLSI Circuits Symposium from 1998 to 2002. He has also served as the Guest Editor and an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, and *International Journal of High Speed Electronics*.