# A 300-GHz 52-mW CMOS Receiver With On-Chip LO Generation

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***Abstract*— A fully integrated receiver employs a heterodyne architecture with 270- and 27-GHz local oscillators to alleviate phase mismatch issues. The system incorporates three on-chip phase-locked loops (PLLs) to generate the local oscillator phases for both downconversions. Realized in 28-nm CMOS technology, the prototype exhibits a noise figure of 16–20 dB, a gain of 17–21 dB, and a 1-dB compression point of −17.3 dBm. The phase noise (PN) of the 270-GHz PLL is −105 dBc/Hz at 10-MHz offset, amounting to an integrated jitter of 106 fs from 10 kHz to 10 MHz.**

***Index Terms*— CMOS, local-oscillator (LO) generation, phase-locked loop (PLL), quadrature, receiver (RX), subsampling, terahertz (THz).**

## I. Introduction

THE 300-GHz band holds great potential for high-speed data communication [1], [2], [3], [4], [5]. With the creation of the IEEE 802.15.3d standard in 2017 for radios operating in the unlicensed frequency band from 252 to 322 GHz [6], there is now a higher interest in developing terahertz (THz) transceivers. Moreover, a number of researchers have demonstrated the viability of such radios in CMOS technology [3], [4], [5], [7], [8], [9], [10], [11], [12], portraying a promising future. We should remark that these examples consume between 140 [8] and 650 mW [9] and employ off-chip local-oscillator (LO) signal generation.

In this article, we contend that the feasibility of THz data-communication radios hinges upon their power consumption. We then present a single-chip receiver (RX) and LO generator that draws 52 mW. The prototype has been fabricated in 28-nm CMOS technology and occupies an active area of 0.06 $mm^2$.

Section II deals with general issues related to THz RX design, and Section III describes the proposed RX architecture.

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TABLE I
Comparison of Wi-Fi, WiGig, and THzCom

| | WiFi | WiGig | THzCom |
|---|---|---|---|
| Carrier Frequency (GHz) | 6.5 | 60 | 300 |
| Available Bandwidth (GHz) | 1.2 | 8.6 | 50 |
| Ant. Size ($\lambda/4$ in air) (mm) | 24 | 2.42 | 0.5 |
| $f_{max}/f_c$ ($f_{max}\approx$450 GHz in 28-nm process) | 69 | 7.4 | 1.5 |
| Metal 9 Spiral | | | |
| Inductance (pH) | 1445 | 218 | 53 |
| Q | 16.8 | 13.7 | 9.3 |
| Varactor Q | 84.1 | 8.4 | 1.7 |

Sections IV–IX delve into the design of the building blocks, and Section X presents the experimental results.

## II. General Considerations

### A. Terahertz Versus Wi-Fi Versus WiGig

The principal attraction of THz radios is that they can access a wide bandwidth (BW) and, hence, carry high data rates. However, Wi-Fi and WiGig radios have also been under intense development [13], [14], [15] and prove formidable competitors. Table I summarizes some attributes of these three wireless systems in conjunction with 28-nm CMOS technology. In addition to the much greater BW, THz communication (THzCom) benefits from smaller antennas. However, it also faces two challenges. First, we write the path loss as [16]

$$\frac{P_{RX}}{P_{TX}} = G_{TX}G_{RX}\frac{\lambda^2}{4\pi d^2} \tag{1}$$

where $G_{TX}$ and $G_{RX}$ are the transmitter (TX) and RX antenna gains, respectively, $\lambda$ is the wavelength, and $d$ the is distance. With $G_{TX} = G_{RX} = 0$ dB, the loss per meter rises from 49 dB for Wi-Fi to 82 dB for THzCom. Thus, the latter must employ extensive beamforming if it is to compete with or complement Wi-Fi and WiGig. This point underscores the importance of low power consumption per beamforming element.

Second, the demands posed on circuit design are much more severe for THzCom. With an NMOS $f_{max}$ of about 450 GHz in 28-nm technology, the ratio of $f_{max}$ to the carrier frequency, $f_c$, falls from about 10 for Wi-Fi to about 1.5 at 300 GHz. Similarly, the quality factor of a single-turn metal-9 spiral varies from 16.8 at 6 GHz to 13.7 at 60 GHz to 9.3 at 300 GHz, presenting significant challenges in amplifier and oscillator design. The inductance values are chosen to provide the same

equivalent parallel resistance, $R_p$, at their respective carrier frequencies. The metal-9 thickness and distance from the substrate are roughly 0.9 and 4 $\mu$m. Moreover, $Q$ of the varactors is projected to drop to single digits [17].

### B. Direct Versus Heterodyne Downconversion

Despite its simplicity, direct downconversion suffers from several drawbacks at THz frequencies. First, it loads the RF path with two mixers and, hence, doubles the capacitance and conductance presented to the signal. As will be explained in Section II-C, this leads to a 2-dB RX NF advantage for heterodyning. Since low-noise amplification and buffering prove difficult at these frequencies, the use of a single mixer by a heterodyne RX makes this architecture more attractive. Second, it requires the generation and distribution of in-phase (I) and quadrature (Q) components of the LO waveform, a daunting task at such high frequencies. For example, compared to the differential VCO presented in this article, a quadrature topology suffers from 12.6 dB higher phase noise (PN) while drawing twice the power. Third, I/Q matching at 300 GHz calls for extremely tight timing skews. For example, a phase mismatch of 10° translates to about 45 fs, a formidable layout challenge.

### C. LO Generation Issues

Terahertz systems commonly begin with a fairly low LO frequency, e.g., in the range of tens of gigahertz, and subsequently multiply it up by means of frequency doublers or triplers [18], [19], [20]. This method avoids THz fundamental-mode oscillators and frequency dividers. However, it also faces two issues.

1) Frequency multipliers typically provide only a single-ended output and require bulky baluns to deliver differential phases. The work in [21], for example, operates with the third harmonic to deliver differential outputs at 60 GHz while drawing 44 mW.
2) The high loss associated with multipliers and baluns dictates the use of gain stages at the final frequency, thereby consuming high power. For example, the multiplier chain in [18] raises an external 15-GHz input to 240 GHz while drawing 1 W. As another example, one can envision an oscillator operating at half of the frequency of interest and doubling the output by means of multipliers [22], [23], [24], [25]. However, the approach in [22], for example, introduces a loss of 14 dB, which must be compensated by several power-hungry stages (given the low transistor gain), so as to drive the RX mixers with sufficient voltage swing. Moreover, the inductors in such stages lead to a complex floor plan. According to simulations, three inductively loaded gain stages in 28-nm technology would require nearly 20 mW to afford 14 dB of gain while driving the mixer in our RX.

One could argue that the high phase noise of fundamental-mode oscillators makes them less attractive than oscillator/multiplier cascades. However, given the large power necessary for the latter, we demonstrate in this article that cascaded phase-locked loops (PLLs) can suppress the phase noise more efficiently. We surmise that fundamental-mode oscillators are more efficient.

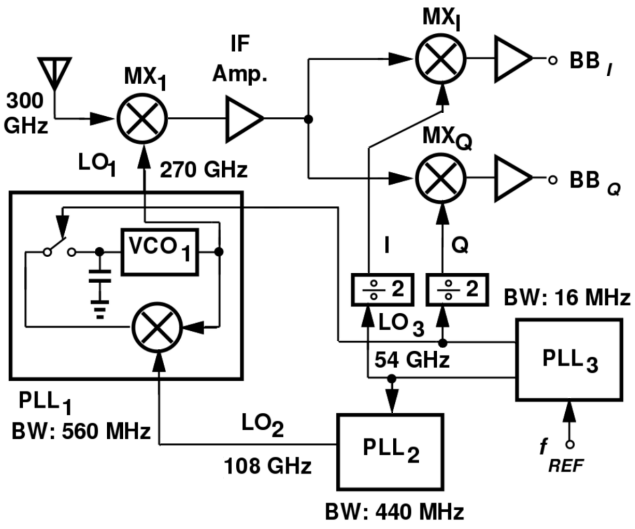



Fig. 1. Proposed RX with LO generation.

Another critical issue is the reference phase noise. For example, a 450-MHz crystal oscillator (Crystek CRBSVS-01-450.000) with a phase noise of −168 dBc/Hz at offset frequencies above 200 kHz yields significant jitter at 300 GHz. For this reason, the PLL BW must be reduced, but then the (fundamental-mode) oscillator contributes excessively. These thoughts point to the use of cascaded PLLs as a more viable solution.

## III. Proposed RX Architecture

For the reasons presented in Section II, this work employs heterodyne downconversion. Fig. 1 shows the RX architecture. The input signal is applied to mixer $MX_1$, which is driven by a 270-GHz LO. The 30-GHz intermediate-frequency (IF) signal is then amplified and downconverted to baseband by $MX_I$ and $MX_Q$ using the quadrature phases of a 27-GHz LO. The LO generation network in Fig. 1 consists of three PLLs and two ÷2 stages. $PLL_3$ receives a 450-MHz reference and synthesizes a 54-GHz differential output, as denoted by $LO_3$ in Fig. 1. This signal drives the dividers and $PLL_2$, which acts as a frequency doubler. $PLL_1$ produces a 270-GHz waveform with the aid of $LO_2$. The cascade of PLLs affords considerable leverage for reducing the overall jitter that the LO path imparts to the RF signal. The reason for incorporating three PLLs becomes clear in Section VI.

To quantify the advantage of this mixer-first heterodyne RX, we plot the simulated noise figure (NF) in three cases, namely, for a heterodyne RX, including an inductively degenerated common-source low-noise amplifier (LNA), a direct-conversion RX presenting two mixers to the input signal, and the proposed RX. Fig. 2 shows the results, predicting NF values of 21.6, 18.6, and 14.1 dB, respectively. For a fair comparison, all of the RX designs target a conversion gain of 15 dB with a 3-dB BW of 20 GHz. It is seen that the

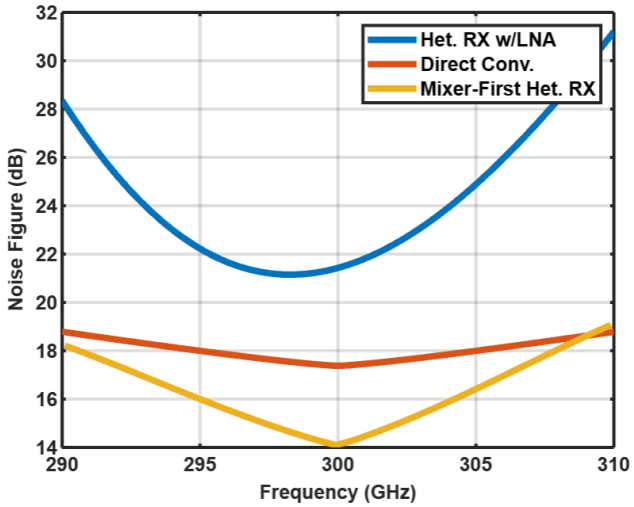



Fig. 2. Comparison of different RX architectures: direct downconversion with LNA, mixer-first direct downconversion, and proposed RX.[1]

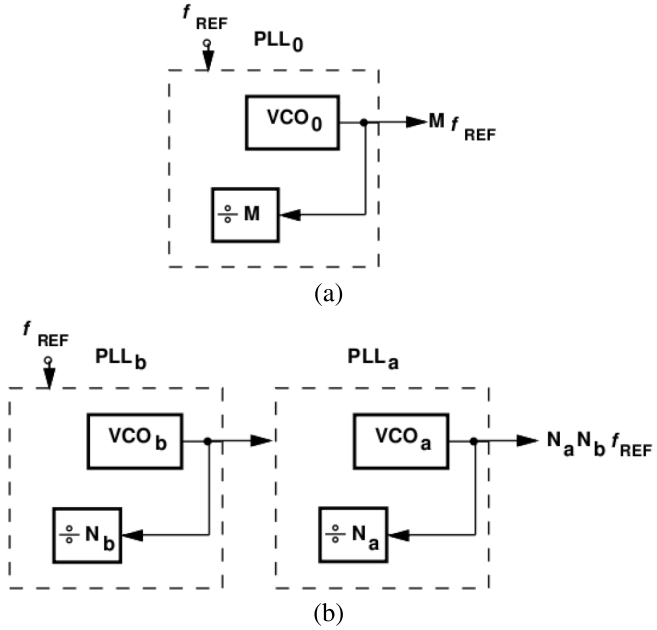



Fig. 3. (a) Single PLL and (b) cascaded PLLs equivalent to the single PLL.

limited transistor gain at 300 GHz prohibits the LNA from reducing the RX NF.

We describe the LO generation circuits later, but we should remark here that the proposed choice of the PLL frequencies and BWs leads to a compact, low-noise design. Specifically, with a reference frequency of 54 GHz, $PLL_1$ benefits from a BW of 560 MHz, greatly suppressing its oscillator phase noise. Similarly, $PLL_2$ achieves a BW of 440 MHz. For $PLL_3$, on the other hand, the BW is selected, so as to minimize the *sum* of the oscillator and reference contributions. The proposed RX saves power by means of two techniques: it avoids typical frequency multipliers and employs no buffers in the RF and LO paths.

## IV. LO Path Optimization

The premise behind the proposed frequency plan in Fig. 1 is that it avoids THz frequency dividers, lossy frequency multipliers, and lossy I/Q separation. The resulting three-PLL solution is justified and optimized, as explained in the following. For illustration purposes, we neglect the phase noise due to flicker noise.

It has been shown in [26] that cascaded PLLs outperform a single loop under certain conditions. Specifically, suppose that we wish to synthesize a given frequency $Mf_{\text{REF}}$ from a crystal oscillator operating at $f_{\text{REF}}$ and exhibiting a relatively flat phase noise of $S_{\text{REF}}$. We first develop $VCO_a$ at this desired frequency, obtaining its phase noise profile, $S_{\Phi na}(f)$. A single PLL is created and optimized by writing $S_{\Phi na}(f_1) = M^2 S_{\text{REF}}$ and selecting the loop BW equal to $f_1$ [see Fig. 3(a)]. Alternatively, we can seek $M = N_a N_b$, cascade two loops containing $VCO_a$ and $VCO_b$, and divide ratios equal to $N_a$ and $N_b$, respectively [see Fig. 3(b)]. If the phase noise of $VCO_b$, $S_{\Phi nb}(f)$, satisfies the following inequality:

$$S_{\phi na}(f) > N_b^2 S_{\phi nb}(f) \tag{2}$$

then cascading is advantageous [26].

[1]The direct-conversion example uses small devices with a simple matching network.

With the inductor and varactor degradations observed in Section II, we expect (2) to hold in our case. In particular, as will be discussed in Sections VI-A and VIII, a 270-GHz 2.5-mW VCO exhibits a phase noise, $S_{\Phi na}(f = 40\text{ MHz}) = -107$ dBc/Hz, whereas a 54-GHz 11.8-mW VCO displays $S_{\Phi nb}(f = 40\text{ MHz}) = -138$ dBc/Hz. We note that raising $S_{\Phi nb}$ by $10\log(270/54)^2 = 14$ dB still leaves a 13-dB margin with respect to $S_{\Phi na}$. Thus, cascading proves beneficial here.

The proposed heterodyne frequency plan in Fig. 1 naturally leads to the 270- and 54-GHz PLL frequencies. The latter is optimized by selecting its loop BW equal to the intersection of its free-running VCO phase noise, $S_{\text{VCO3}}(f)$, and the "amplified" reference phase noise, $(120)^2 S_{\text{REF}}$. With $S_{\text{REF}} = -168$ dBc/Hz, this yields $\text{BW}_3 \approx 25$ MHz, but, to suppress the VCO flicker noise contribution, we select $\text{BW}_3 \approx 40$ MHz.

As explained in Section VI, $PLL_2$ and $PLL_1$ can be jointly viewed as a frequency-quintupling circuit. We, thus, consider $PLL_3$ and $PLL_1$ as $PLL_b$ and $PLL_a$ in Fig. 3(b), respectively, with $N_b = 120$ and $N_a = 5$. In the simplest case, we would find the intersection of $N_a^2 N_b^2 S_{\text{REF}}$ with the phase noise of $VCO_1$, but, in our design, the former lies below the latter [see Fig. 4(a)]. Some optimization is, therefore, necessary so that the sum of the shaped $VCO_1$ phase noise, and that of $PLL_3$ is minimized. Selecting a BW of 560 MHz for $PLL_1$ [see Fig. 4(b)] yields an rms jitter of 43.3 fs from this PLL and another 33.9 fs from $PLL_3$. (The jitter contributed by $PLL_2$ is only 4.8 fs.)

## V. RX Design

The heterodyne path depicted in Fig. 1 receives and down-converts the 300-GHz input to an IF of 27 GHz. Plotted in Fig. 5 are the simulated NF and voltage conversion gain of a standard single-balanced active mixer serving this purpose. The mixer output loads are realized as resistors rather than an $LC$ tank to maximize the BW. We note the high NF and the

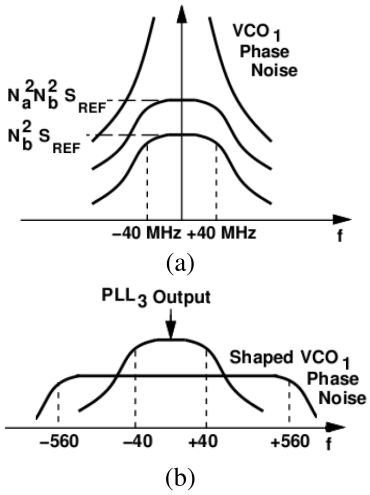



Fig. 4. (a) Noise contributions of cascaded stages. (b) $VCO_1$ noise shaping.

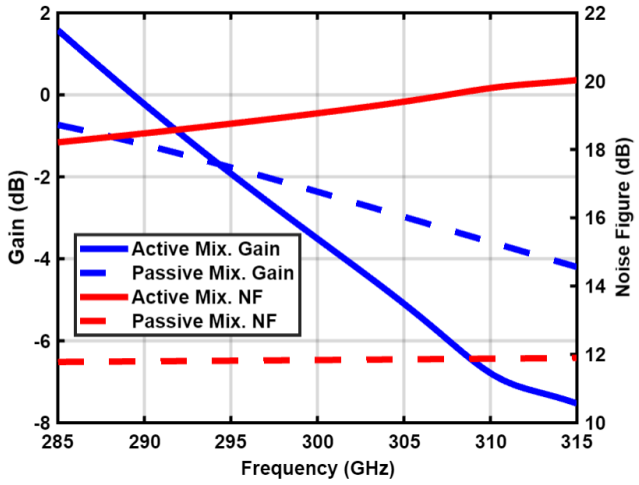



Fig. 5. Active and passive mixer gain and NF comparison.

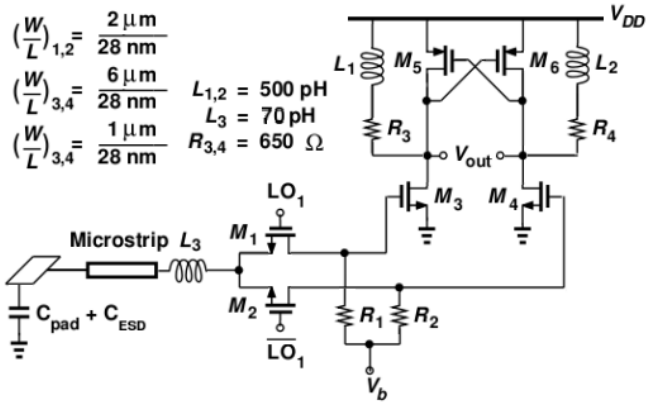
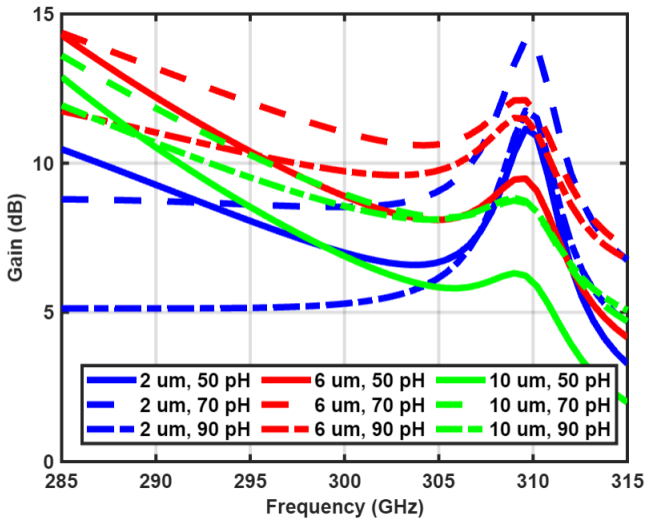



Fig. 6. Proposed input mixer and IF amplifier.

low gain. Similarly, a passive implementation with capacitive loads yields the results shown in Fig. 5, still poor performance, yet better than the active mixer case.

The mixer employed in this work is illustrated in Fig. 6 along with the IF amplifier. The gate of the mixer is directly biased by the LO common-mode level. The drain and the source are directly biased with the external $V_b$, which also provides the gate bias of the IF amplifier. The use of series peaking inductor $L_3$ alleviates the effect of pad and electrostatic discharge (ESD) device capacitances. The switching action of $M_3$ and $M_4$ with sinusoidal LO waveforms presents a real part at the input, which, along with the resistive losses of the microstrip and $L_3$, yields reasonable matching. The transmission line is implemented with a 1.4-$\mu$m-wide metal-9 RF line atop a 14.4-$\mu$m-wide metal-3 ground. The principal tradeoff encountered here, namely, that between the loss of $M_1$ and $M_2$ and the input capacitance of $M_3$ and $M_4$, is also relaxed by $L_1$.



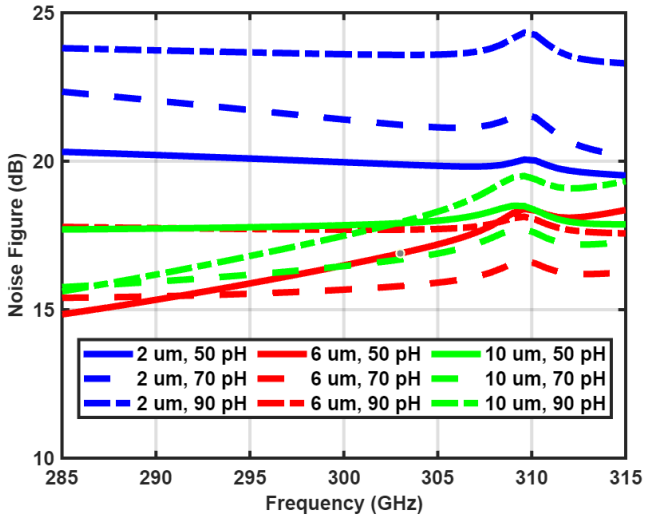




Fig. 7. (a) Gain and (b) NF of mixer/IF amplifier cascade for $W_{3,4} = 2$, 6, and 10 $\mu$m and $L_3 = 50$, 70, and 90 pH.

The tradeoffs in the design are quantified by the simulated gain and NF plots shown in Fig. 7, where $W_{3,4}$ varies from 2 to 10 $\mu$m (the channel lengths are 28 nm), while their drain current density remains constant. Inductor $L_3$ assumes values of 50, 70, and 90 pH, revealing that the optimum occurs for $W_{3,4} = 6$ $\mu$m and $L_3 = 70$ pH. We should remark

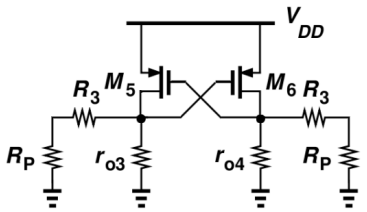



Fig. 8. Small-signal model of the IF amplifier.

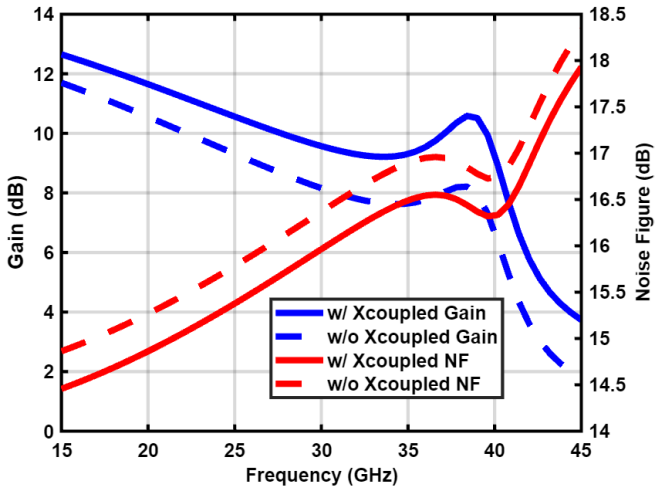



Fig. 9. RF mixer and IF amplifier gain and NF with and without PMOS cross-coupled pair.

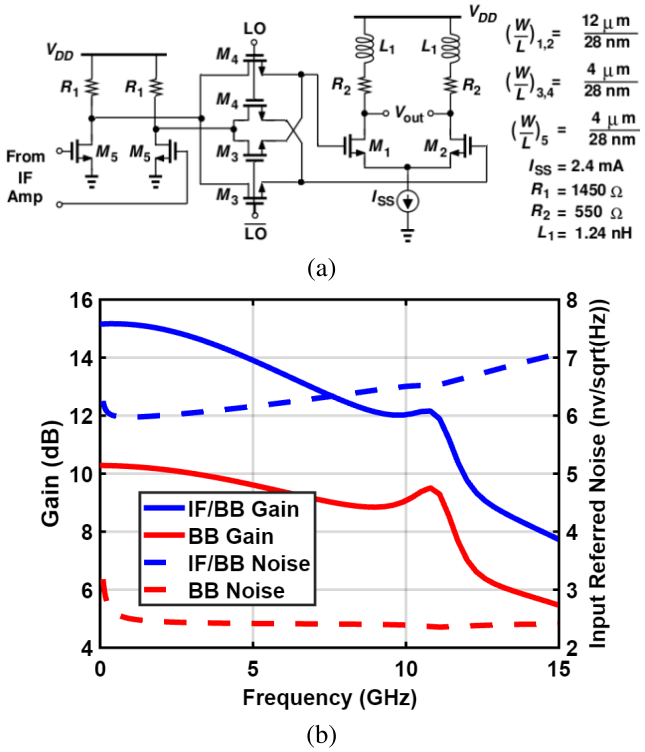



Fig. 10. (a) IF mixer and baseband amplifier and (b) their combined gain and input referred noise.

that these simulations incorporate the logic models for intrinsic transistors, and the remainder of the layout is extracted by Ansoft's HFSS [27]. Thus, all resistive, capacitive, and inductive parasitics associated with vias and interconnects are included.

In order to achieve a high gain across a wide BW, the IF amplifier incorporates shunt peaking but also a cross-coupled PMOS pair. The latter provides 16% of the bias current of $M_3$ and $M_4$, and also raises the gain. The loop gain provided by $M_5$ and $M_6$ must remain below unity at dc to avoid latchup and at high frequencies to preclude oscillation. The latter condition prevails as the resonance of the tanks raises the loop gain. With the aid of the simplified model depicted in Fig. 8, where $R_p$ denotes the equivalent parallel resistance of the tanks, we have

$$\text{Loop Gain} = g_{m5}^2\left[(R_3 + R_p)||r_{o5}||r_{o6}\right]^2. \tag{3}$$

This value is set to about 0.6 in this design in the worst case. Fig. 9 plots the simulated gain and NF of the mixer and the amplifier before and after $M_5$ and $M_6$ added. We note that the gain rises by 1 dB on average, and the NF falls by 0.4 dB. The circuit draws 0.92 mW, and the 3-dB IF BW reaches 40 GHz. No matching network is implemented between the RF mixer and IF amplifier to preserve the high BW and prevent further matching losses between the components.

The IF mixers in Fig. 1 consist of common-source stages driving passive double-balanced mixers. These mixers are followed by a baseband gain stage [see Fig. 10(a)]. The simulated gain and input-referred noise voltages of the baseband amplifier and the overall IF mixer/amplifier chain are plotted in Fig. 10(b). The chain draws 4.3 mW.

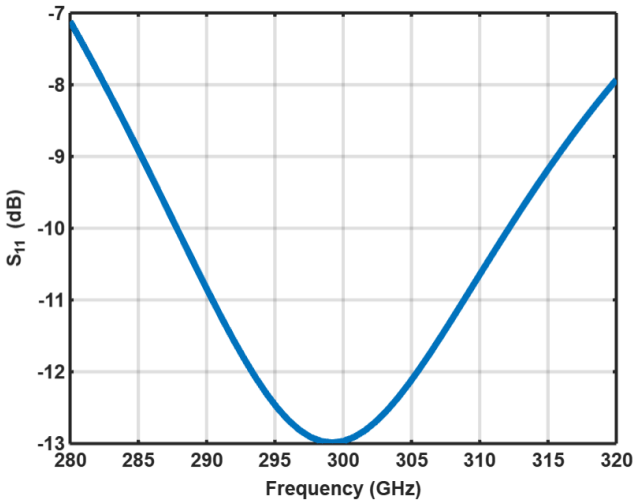



Fig. 11. Simulated $S_{11}$ of the RX.

Overall, RX achieves a minimum NF of 16 dB, with 48% of the noise contributed by the input matching network and the pad parasitics. Another 41% is due to the RF mixer, and the rest is due to the IF amplifier and mixers.

Fig. 11 plots the simulated $S_{11}$ of the RX (with the mixer switching). $S_{11}$ is below $-10$ dB across a BW of about 25 GHz.

## VI. RF PLL

In the proposed architecture of Fig. 1, $\text{PLL}_1$ generates an LO waveform at 273 GHz for the RF mixer. In this section, we study the design of this PLL and its building blocks.

### A. PLL Architecture

We wish to employ a fundamental-mode differential VCO to generate the 273-GHz waveform; our conjecture is that such an endeavor consumes less power than beginning with a low-frequency oscillator and using multipliers. Nonetheless, we face several challenges that impact the choice of the architecture and circuit topologies. First, the VCO must deliver large voltage swings to the passive RF mixer, so as to ensure a low ON-resistance for the transistors and, hence, a low loss. Second, as mentioned in Section II-C, MOS varactors suffer from a low $Q$ at these frequencies [17], degrading the phase noise and possibly prohibiting oscillation startup. Third, even without the varactor issue, the VCO phase noise generally rises at higher frequencies. For a standard $LC$ oscillator having a tail current of $I_{SS}$, the phase noise is generated due to the cross-coupled transistors, and the tank's thermal noise is given by [28]

$$S_{\Phi n}(f) = \frac{\pi^2(\gamma+1)kT}{2R_p I_{SS}^2}\left(\frac{f_0}{2Q\Delta f}\right)^2 \tag{4}$$

where $\gamma$ is the excess noise coefficient of MOSFETs, $R_p$ is the equivalent parallel resistance of the tanks, $f_0$ is the oscillation frequency, and $\Delta f$ is the offset frequency. As an example, according to HFSS simulations, a 45-pH inductor used in a 56-GHz synthesizer [29] has $Q$ of about 20, and $R_p = 320\ \Omega$, whereas, at 273-GHz, $Q = 15$ and $R_p = 636\ \Omega$. Thus, for the same bias current, the oscillator phase noise rises by a factor of 21.2, as we go from 56 to 273 GHz.

The key point here is that the VCO phase noise can be suppressed to acceptable levels only if $\text{PLL}_1$ provides a very wide BW, which, in turn, requires a high reference frequency. With $f_{\text{LO}_3} = 54$ GHz in Fig. 1, this condition is satisfied.

The fourth challenge relates to the need for a 273-GHz frequency divider. Such a circuit must present a small capacitance to the VCO, achieve a sufficiently wide lock range, and drive the next divider stage with proper voltage swings. To avoid these daunting requirements, we turn to a subsampling PLL architecture [30].

Fig. 12(a) shows a possible realization, where $S_1$ samples the VCO voltage on $C_1$ when the reference falls. Unfortunately, such an arrangement fails to lock, a phenomenon caused by the finite fall time of the reference. As illustrated in Fig. 12(b), the difficulty is that the ON-resistance of $S_1$ climbs, while $V_{\text{VCO}}$ makes several cycles. As a result, the last cycle reaching $C_1$ is heavily attenuated, carrying little phase information or, from another perspective, leading to a low phase detector (PD) gain. This effect is quantified by the simulated PD gain shown in Fig. 12(c) as a function of the LO fall time. Here, $V_{\text{VCO}}$ arrives at 270 GHz and $V_{\text{REF}}$ at 54 GHz. Given the nearly sinusoidal waveforms at our frequencies of interest, we predict failure to lock.

The foregoing difficulty is resolved if the feedback frequency sensed by the PD is lowered, preferably without resorting to a frequency divider. This is possible by means of offset mixing, as depicted in Fig. 13(a). Selecting $f_3 = 2 \times 54\ \text{GHz} = 108\ \text{GHz}$, we observe that $f_b = 168\ \text{GHz} = 3f_{\text{REF1}}$. Thus, the PD subsamples by a factor of 3. We expect

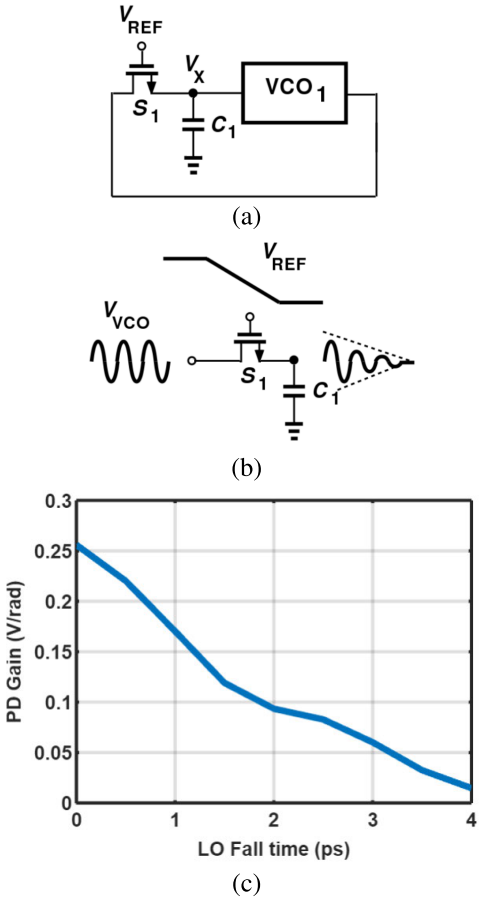



Fig. 12. (a) Simple subsampling PLL, (b) subsampling failure due to long high rise/fall time, and (c) effect of rise/fall time on PD gain.

the 65% reduction in the frequency sensed by the PD to raise its gain considerably. Fig. 13(b) repeats the PD simulation versus the subsampling ratio, assuming that the reference has a sinusoidal waveform. Reducing the ratio from 5 to 3 suggests a tenfold increase in the PD gain.

We should remark that the proposed PLL does not carry to its output spurs created by mixer $\text{MX}_0$. Since $\text{MX}_0$ generates frequencies equal to $mf_{\text{VCO1}} \pm nf_3$, where $m$ and $n$ are integers; since $f_{\text{VCO1}} = 5f_{\text{REF1}}$ and $f_3 = 2f_{\text{REF1}}$, we note that the PD transistor senses only harmonics of $f_{\text{REF}}$ at its inputs and, hence, does not produce spurs at $X$. This is an advantage of the proposed LO generation scheme.

The actual implementation of $\text{PLL}_1$ is depicted in Fig. 14(a). The high-frequency paths operate differentially, and $V_b$ is connected to the ground, so as to provide a proper common-mode level for the $G_m$ stage, which employs PMOS input devices; as shown in Fig. 14(b).

### B. $\text{PLL}_1$ Dynamics

In order to quantify the properties of $\text{PLL}_1$, we construct the linear phase model shown in Fig. 15(a). Subsampling by a factor of 3 is modeled by a phase tripler and the offset mixer by a phase adder sensing $2\Phi_{\text{in}}$. This is because the two inputs to this PLL only differ in frequency by a factor of 2 but are, otherwise, identical if the noise of $\text{PLL}_2$ in Fig. 1 is neglected.

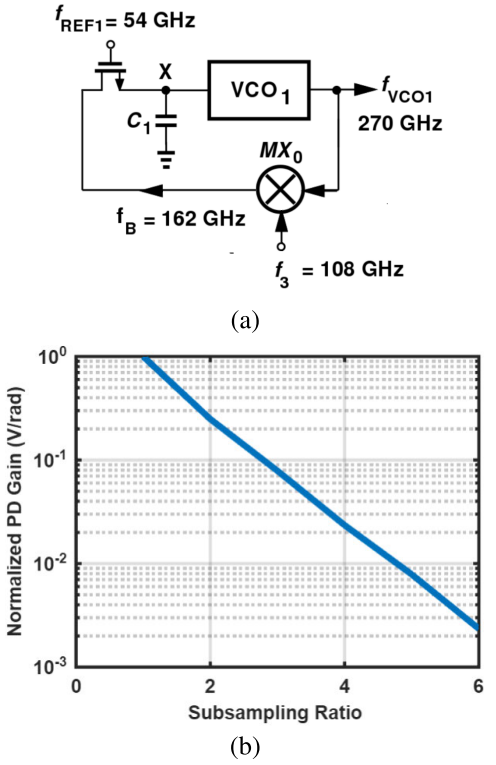



Fig. 13. (a) Lowering subsampling PD input frequency with the aid of an offset mixer and (b) effect of frequency reduction on PD gain.

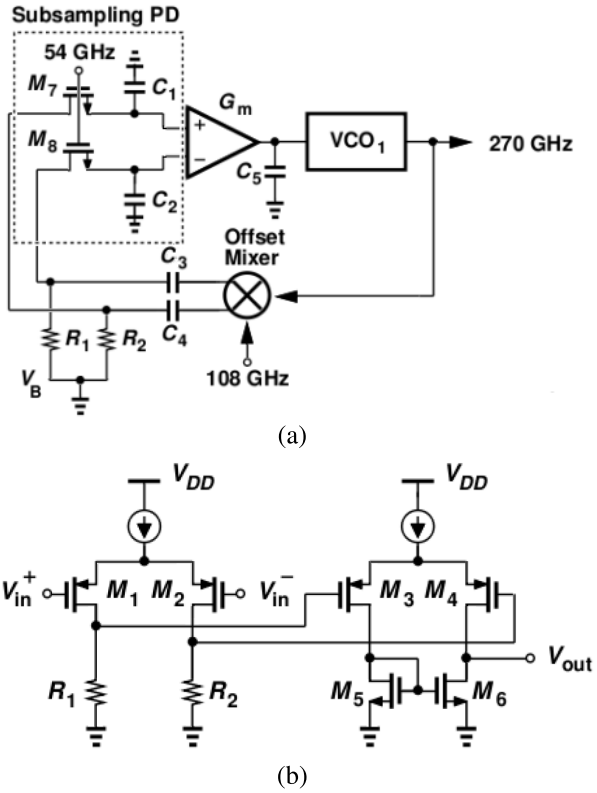



Fig. 14. (a) $PLL_1$ implementation and (b) $G_m$ stage.

Since the phase error, $\Phi_e$, is equal to $3\Phi_{\text{in}} - (\Phi_{\text{out}} - 2\Phi_{\text{in}}) = 5\Phi_{\text{in}} - \Phi_{\text{out}}$, we can reduce the loop to that shown in Fig. 15(b), where $\Phi_{\text{in}}$ is equivalently multiplied by a factor of 5. Note that

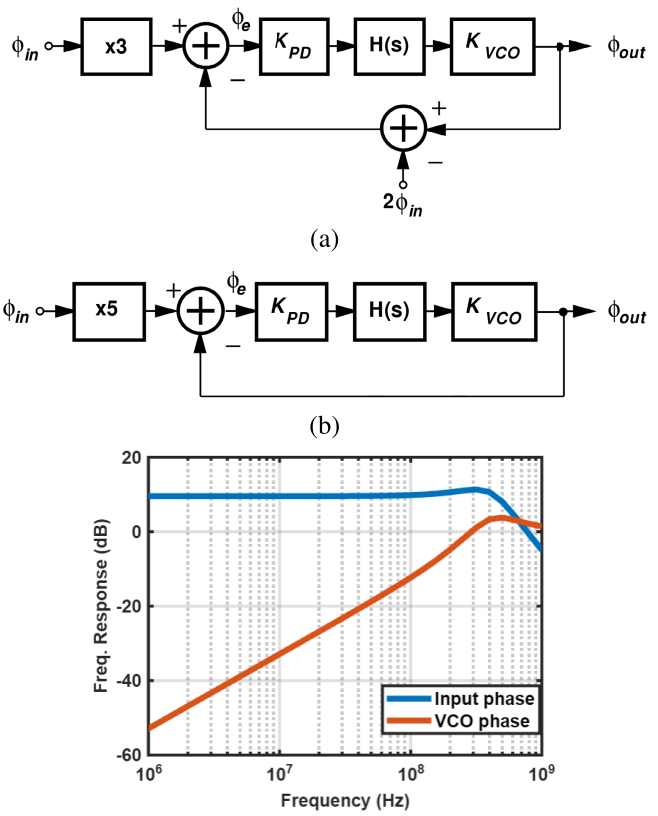



Fig. 15. (a) Linear phase model of $PLL_1$, (b) equivalent model without an offset mixer, and (c) closed-loop phase responses of $PLL_1$.

the mixer's downconversion gain does not appear directly in this model, but its output swing sets the PD gain.

In this work, $H(s)$ is defined by the $G_m$ stage and $C_1$, and expressed as $A_0/(1 + s/\omega_0)$, where $A_0 = 8$ V/V and $\omega_0 = 2\pi \times (2$ GHz). The loop transmission, thus, emerges as

$$T(s) = 5K_{\text{PD}} \frac{A_0}{1 + \frac{s}{\omega_0}} \frac{K_{\text{VCO}}}{s}. \tag{5}$$

With $K_{\text{PD}} = 32$ mV/rad and $K_{\text{VCO}} = 30$ GHz/V, the loop BW is about 560 MHz. Fig. 15(c) plots the simulated closed-loop responses of the PLL from the input phase and also from the VCO phase to the output. The loop suppresses the VCO phase noise by more than 30 dB up to an offset of 10 MHz. Illustrated in Fig. 16 is the settling behavior, suggesting that the loop locks in about 20 ns.

### C. 270-GHz VCO

The RF PLL VCO must provide relatively large differential swings to $MX_1$ in Fig. 1. Prior work on fundamental-mode oscillators has demonstrated operation at 300 GHz in 65-nm technology [31]. We, thus, surmise that achieving 270 GHz in our 28-nm process is feasible, but we must now add frequency tuning. All simulation results in this section are reported for the extracted layout.

While MOS varactors are generally the preferred choice for tuning, studies indicate that their $Q$ falls to single digits at the frequency of interest here [17]. According to simulations, our

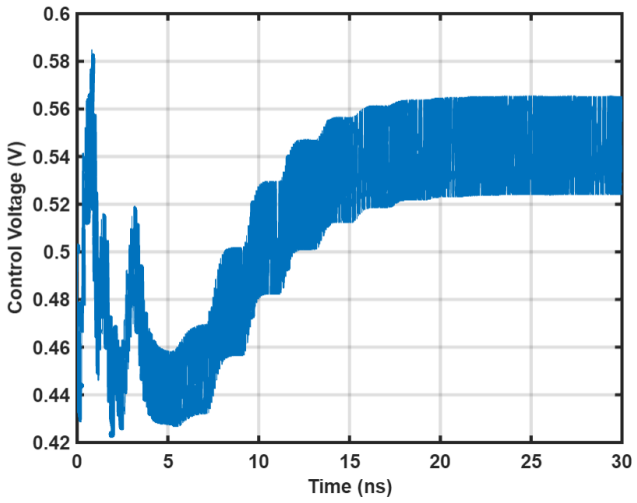



Fig. 16. Settling behavior of $PLL_1$.

varactors' $Q$ drops to 1.7 at 270 GHz.[2] As a result, a VCO using such a varactor may even fail to oscillate. We, therefore, propose a different tuning mechanism that exploits the voltage dependence of the gate–source capacitance of the transistors within the oscillator core.

The proposed VCO is shown in Fig. 17(a). The core consists of $M_1$–$M_4$ and $L_1$ and $L_2$ [31], and the CM level is adjusted by $M_5$. Resistors $R_1$ and $R_2$ provide part of the bias currents of the two pairs, so as to ensure oscillation startup even if the PLL initially holds $V_{\text{cont}}$ near $V_{\text{DD}}$. As $V_{\text{cont}}$ varies from near zero to about $V_{\text{DD}} - |V_{\text{TH5}}|$, the CM level at $X_1$ and $Y_1$ falls from 0.91 to 0.50 V, and consequently, the single-ended capacitance at $X_1$ and $Y_1$ declines. The CM change also affects the output swing, but we simply design the stage for an acceptable swing in the worst case. The load presented to $VCO_1$ consists of the input ports of the RF mixer and the offset mixer along with the interconnects. Inductors $L_1$ and $L_2$ are so chosen to accommodate these capacitances with no intervening buffers.

Fig. 17(b) plots both the oscillation frequency and the peak-to-peak single-ended voltage swings at $X_2$ and $Y_2$ as a function of $V_{\text{cont}}$. The worst case swing is around 700 mVpp, sufficient to drive the RF mixer in Fig. 6. The varying amplitude affects the PD gain as well. According to simulations, the PD gain changes by 22% across the VCO tuning range.

The VCO's coupled inductors are realized as the nested structure depicted in Fig. 17(c), each having a linewidth of 3.3 $\mu$m. The diameters are 26.7 and 33.0 $\mu$m for $L_1$ and $L_2$, respectively, and the line spacing is 1.45 $\mu$m. According to HFSS simulations, $Q$ reaches about 15.6 at 270 GHz. Since the lengths of $L_1$ and $L_2$ are not much less than the wavelength, these inductors should be treated as distributed networks (transmission lines). S-parameter models provided by HFSS simulations, of course, represent these effects. Nonetheless, we refer to these structures as "inductors" for the sake of intuition.

[2]The process does not allow a channel length less than 200 nm for varactor devices.

With a total bias current of 2.5 mA at mid-range, the VCO operates at 271 GHz and exhibits the simulated phase noise shown in Fig. 17(d). At a 10-MHz offset, the PN is about −93.6 dBc/Hz, yielding a figure of merit (FOM) of −178 dB. For a simple cross-coupled $LC$ oscillator with an ideal tail current source, the FOM would be around −195 dB if no flicker noise is upconverted. In the PN profile of Fig. 17(d), on the other hand flicker noise dominates up to about 10-MHz offset. Nevertheless, by virtue of cascaded PLLs, the flicker noise contribution to the overall jitter becomes negligible.

At 10-MHz offset, the PN contributions are given as follows: 57% by $M_3$ and $M_4$, 5% by $M_1$ and $M_2$, 33% by the loss of $L_1$ and $L_2$, and 4.5% by the offset mixer connections and parasitics. Due to its large dimensions, $M_5$ adds 0.4% to the output phase by its flicker noise.

The PN is fairly constant across the tuning range, changing from −93.9 and −93.1 dBc/Hz as the oscillation frequency varies from 266 to 273 GHz.

The proposed fundamental-mode VCO displays a relatively high phase noise, an issue addressed at the architecture level by a wide loop BW. This is possible only by cascading PLLs.

### D. Offset Mixer

The offset mixer in Fig. 14 must sense the VCO output with minimal loading yet provide a sufficiently large voltage swing to the PD. The circuit is realized as an active double-balanced topology with inductive loads (see Fig. 18) The connection of the 270- and 108-GHz waveforms to the two input ports is decided as follows. The small transistors driven by $VCO_1$ cannot produce a large drain current, whereas those attached to the 108-GHz input can. For this reason, the top switching quad is tied to $VCO_1$. Resistors $R_1$ and $R_2$ provide about 40% of the bias currents of $M_1$ and $M_2$, thereby increasing the mixer's conversion gain. The remainder of the current flows through $M_1$–$M_4$. Drawing 1.2 mA, the circuit generates a single-ended peak-to-peak output swing of 420 mV.

### E. Overall Phase Noise

With $PLL_1$ realized entirely at the transistor level, we can examine its output phase noise. If the PN of the 54- and 108-GHz inputs is neglected, the result emerges as shown in Fig. 19. Due to the type-I nature of the PLL, the profile follows a $1/f$ fall up to about 20 MHz and remains relatively flat and equal to −120 dBc/Hz up to 400 MHz.

The integrated jitter amounts to 22.2 $\text{fs}_{\text{rms}}$ from 10 kHz to 10 MHz and 605.2 $\text{fs}_{\text{rms}}$ from 10 kHz to 1 GHz. At the 10-kHz offset, the VCO and the PD $kT/C$ noise (where $C$ is equal to 5 fF) contribute about 16.8% and 75.2%, respectively, and the remainder arises from the amplifier. At the 1-GHz offset, the VCO contribution jumps to 88.9%, and the rest of the contribution comes from the $kT/C$ noise.

## VII. 108-GHz PLL

As explained in Section III, $PLL_2$ in Fig. 1 acts as a frequency doubler, creating an offset frequency of 108 GHz for $PLL_1$. In contrast to such doubling techniques as push–push

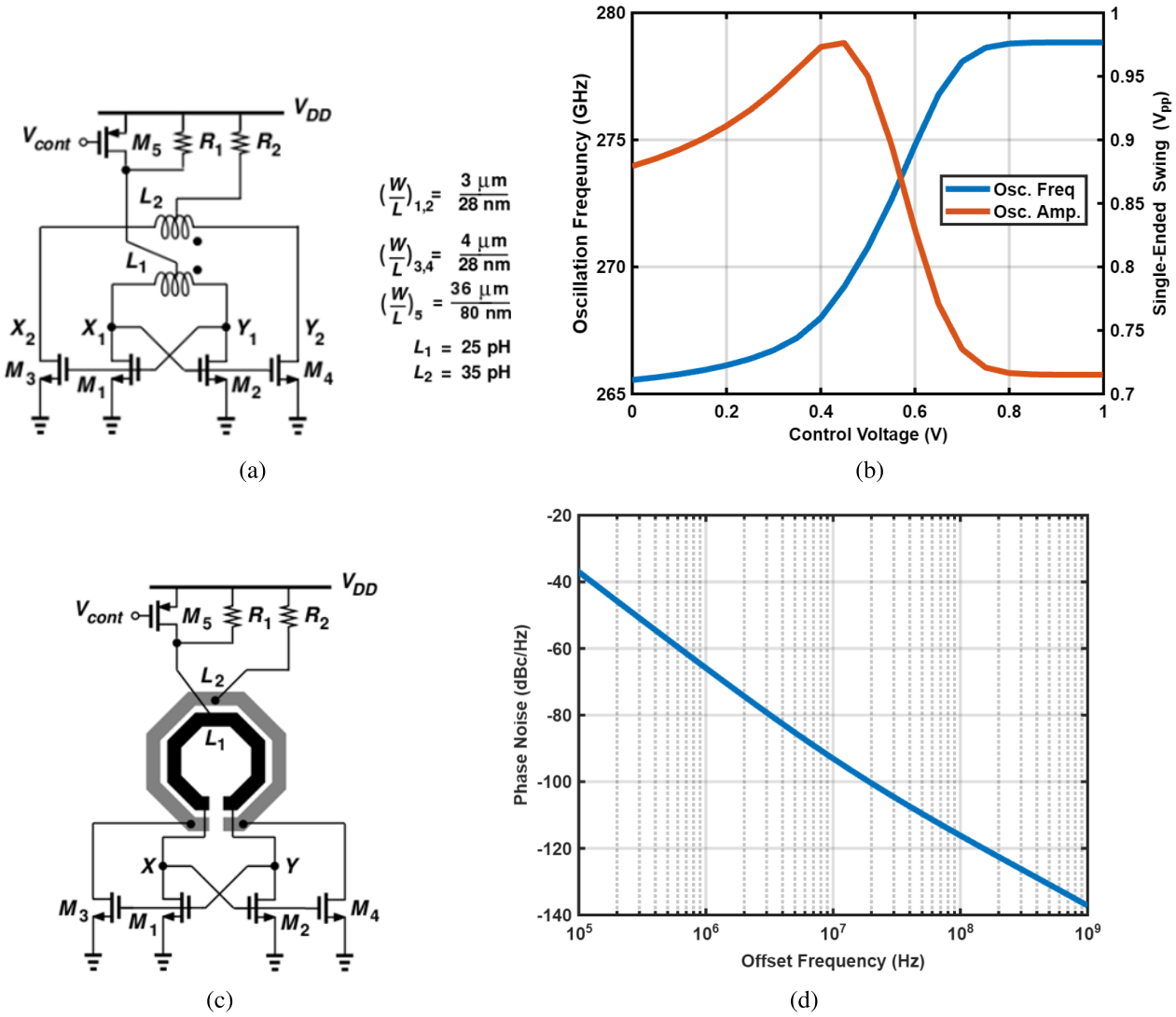



Fig. 17. (a) 270-GHz VCO implementation, (b) frequency and amplitude of oscillation versus control voltage, (c) coupled inductor layout and connections, and (d) simulated VCO phase noise at 270 GHz.

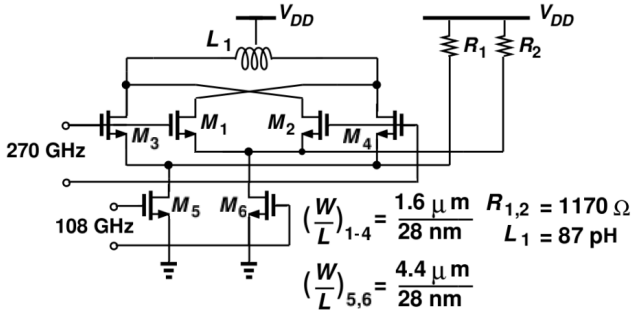



Fig. 18. Offset mixer in $PLL_1$.

networks [18], [19], [20], this approach proves more efficient because it directly delivers differential waveforms.

As shown in Fig. 20(a), $PLL_2$ employs subsampling as well. The actual implementation is similar to that in Fig. 14 but without offset mixing; the VCO output is directly sampled by the switch. The VCO design is also similar to $VCO_1$. Drawing 9.7 mA from the supply, this PLL displays the simulated phase noise plotted in Fig. 20(b) if the 54-GHz input is assumed noiseless. We observe that this PLL contributes negligible

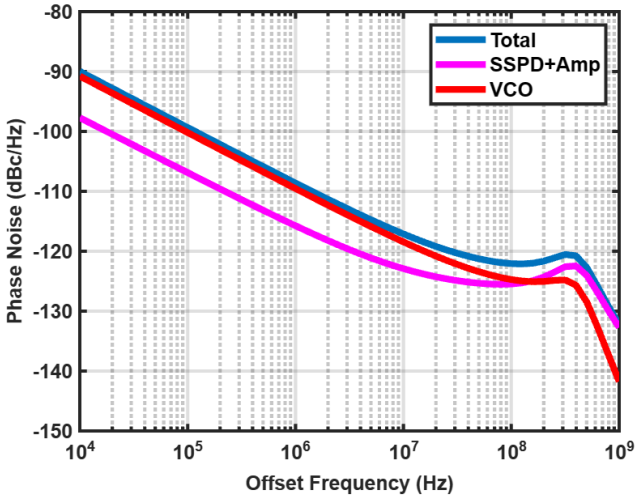



Fig. 19. 270-GHz PLL phase noise without $PLL_2$ and $PLL_3$ contributions.

phase noise compared to $PLL_1$. As with the 270-GHz PLL, the loop BW is dictated by the amplifier's dominant pole, reaching 270 MHz.

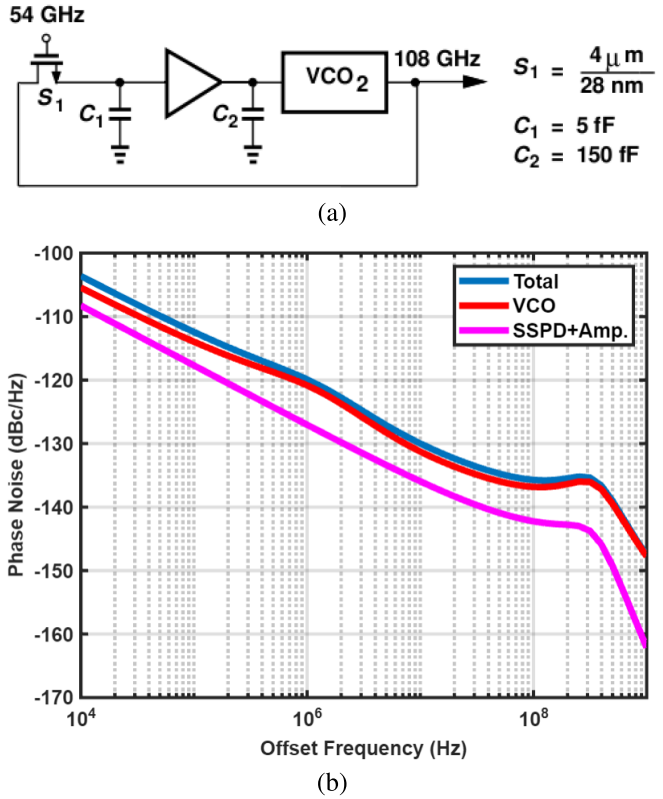



Fig. 20. (a) $PLL_2$ implementation and (b) its phase noise without reference contribution.

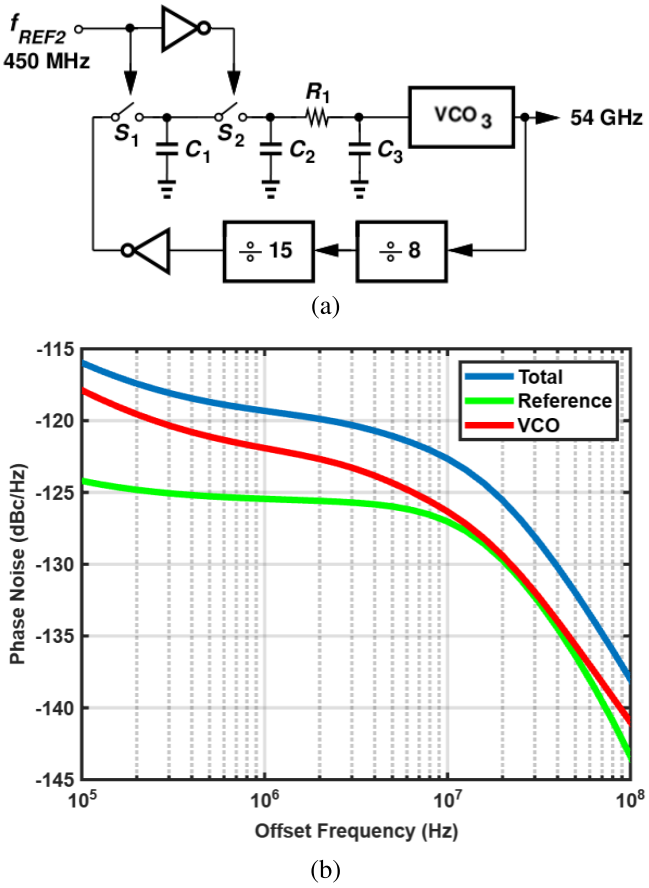



Fig. 21. (a) $PLL_3$ implementation and (b) its phase noise.

## VIII. 54-GHz PLL

The 54-GHz integer-N PLL is depicted in Fig. 21(a). The sampling PD consisting of $S_1$, $C_1$, $S_2$, and $C_2$ [32] receives a 450-MHz reference from Crystek's CRBSVS-01-450.000 crystal oscillator. The loop BW is selected as follows. Upon traveling to the PLL output, the reference phase noise, $S_{REF}$, is multiplied by $M^2 S_{REF}$, where $M = 8 \times 15 = 120$. As illustrated in Fig. 21(b), the BW is chosen, so as to minimize the sum of this phase noise and that of the VCO. With $S_{REF} \approx -168$ dBc/Hz, we obtain $f_{BW} \approx 40$ MHz.

The VCO is implemented as a conventional complementary $LC$ topology with tail resonance tanks. Consuming 11.8 mW, this VCO exhibits a phase noise of $-121.9$ and $-134.0$ dBc/Hz at 1- and 40-MHz offsets, respectively. The difference between the reference noise and the total noise arises from the reference buffer, the PD, and the divider.

The $\div 8$ circuit in this PLL can potentially consume high power and/or require inductors. We propose a $\div 2$ stage that obviates the need for either. Consider the arrangement shown in Fig. 22(a) where each latch is realized by a switch and an inverter. The finite delay through the stages limits the division speed. We surmise that adding *feedforward* paths can raise the maximum toggle rate. For example, we envision that the *unclocked* feedforward paths in Fig. 22(b) begin to impress the states at $X$ and $Y$ before the main clocked paths do so. Fig. 22(c) depicts another example [29]. We expect that feedforward boosts the higher end of the "lock range" but also raises the lower end. Thus, the choice among different feedforward topologies is governed by how well the lock range

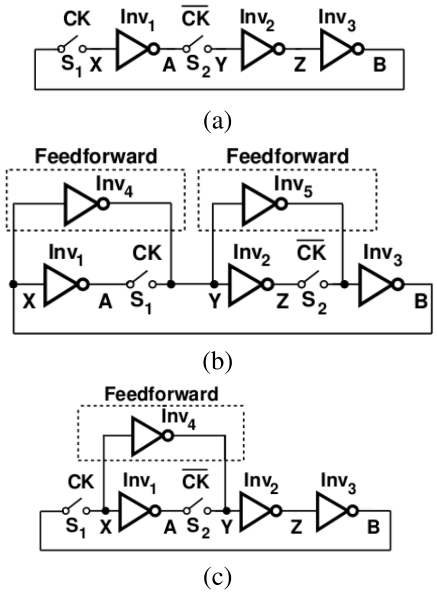



Fig. 22. (a) Simple divide-by-2 implementation, (b) possible feedforward paths, and (c) alternative topology.

encloses the desired frequency in the presence of process, supply voltage, and temperature (PVT) variations.

The speed limitations of the proposed divider can be estimated as follows. Suppose, as shown in Fig. 23(a), $B$ is high and CK rises at $t = 0$ to activate $S_1$. Now, $X$ goes high,

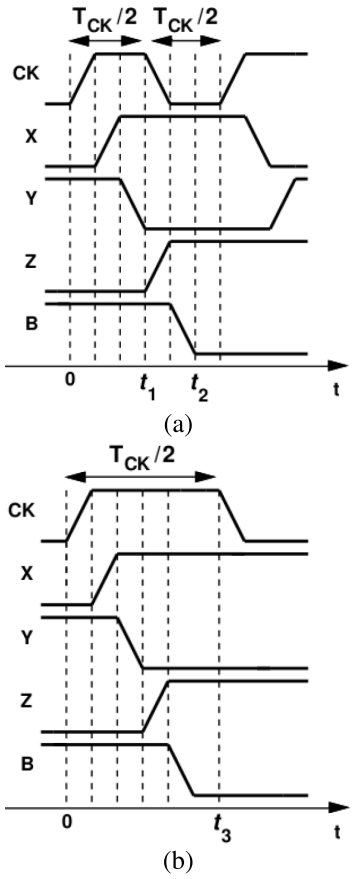



Fig. 23. (a) Divider high-speed limitation timing diagram. (b) Divider low-speed limitation timing diagram.

TABLE II
COMPARISON OF DIVIDER INPUT FREQUENCIES OF FIG. 22 WITH RESPECT TO PROCESS CORNERS

| | SS | TT | FF |
|---|---|---|---|
| Fig. 22(a) | 0-46.3 | 0-52.6 | 0-57.4 |
| Fig. 22(b) | 44.2-58.7 | 52.1-66.0 | 60.1-76.3 |
| Fig. 22(c) | 38.5-56.2 | 41.7-61.4 | 46.6-66.3 |

is inverted by $INV_4$, and reaches $Y$. Thus, $Y$ should complete its transition before CK falls, requiring that $t_1 < T_{CK}/2$. Similarly, the edge on $Y$ must reach $B$ before CK rises again, i.e., we must have $t_2 < T_{CK}/2$. Viewing $t_2$ as roughly four gate delays, we conclude that $T_{CK}$ must exceed this amount. This signifies the upper end of the lock range.

For the lower end, we observe that, when $S_1$ is ON, the loop is "transparent." As depicted in Fig. 23(b), the edge on $Y$, thus, travels to B, causing $X$ to change again and, hence, the circuit to fail. We must then have $t_3 < T_{CK}/2$. Approximating $t_3$ by four gate delays, we estimate the longest $T_{CK}$ to be eight gate delays. The ideal lock range, thus, spans an octave. In practice, sinusoidal clocks narrow this range to some extent.

In order to quantify these effects, we simulate the extracted layout of the circuits shown in Fig. 22 and tabulate their input frequency ranges in Table II. The switches are implemented by single NMOS devices whose gates reside at a dc level equal to $V_{DD}$ and receive the input through capacitive coupling. We consider the slow-slow (SS) and fast-fast (FF) corners of the process. Table II shows the results for the three dividers. We observe that feedforward raises the maximum speed in the SS corner to 58.7 GHz for topology in Fig. 22(b) and 56.2 GHz for that in Fig. 22(c). However, the *lower* end of the lock range in the FF corner exceeds the desired value of 54 GHz in Fig. 22(b). For this reason, we opt for Fig. 22(c).

The proposed ÷2 structure does not directly produce quadrature phases for the IF mixers. We, thus, incorporate two copies, with their CK and $\overline{CK}$ inputs swapped (see Fig. 1).

The two other ÷2 stages in the ÷8 circuit are similar to the topology in Fig. 22 but with complementary switches. The ÷15 block is based on the Vaucher topology [33].

The 54-GHz PLL draws 17 mW, of which 9.5 mW are consumed by the VCO and 1.2 mW by the ÷15 chain. A fractional-N version of this PLL has been reported in [29] and can be utilized here for fine channel spacings.

## IX. Floor Planning Issues

The proposed system employs a large number of inductors to boost the performance in both the signal path and the LO path. While the individual blocks can be laid out in a fairly compact form, the interconnection among them poses daunting challenges. This is particularly prominent here as we wish to avoid terminated transmission lines (which would demand power-hungry drivers). The compact placement of inductors raises concerns about injection pulling among oscillators, but their large frequency separations avoid this issue. Also, according to simulations, $Q$ of the inductors falls negligibly due to these proximity effects.

The most critical interface in Fig. 1 is that between the 270-GHz VCO, and the RF and offset mixers. We must decide how to arrange this VCO's nested inductors and those preceding the RF mixer and serving as the load of the offset mixer. To minimize the parasitics at the VCO output, we place the two mixers' transistors within the VCO's active area [see Fig. 24(a)]. We also position the 108-GHz VCO in the same vicinity. This means that the offset mixer's output current in Fig. 24(a) must travel a fairly long distance (≈50 $\mu$m) to reach its load inductor. Fortunately, this interconnect can be exploited for series peaking to cancel the mixer output capacitance. As illustrated in Fig. 24(b), the idea is to sense the output at position B (rather than at A) so that the trace inductance does not degrade the conversion gain.

The 54-GHz PLL can occupy the left-hand side of the 270-GHz VCO, but it would incur long interconnects to reach the PD in $PLL_1$. For this reason, $PLL_3$ is placed near the offset mixer inductor.

The simulation of the layout relies on parasitic extraction for short local connections and Ansoft's HFSS for longer lines and inductors. This methodology has led to less than 4% measured error in the center frequencies of the VCOs. The simulated leakage of the 270-GHz LO to the RF input is −54.6 dBm.

## X. Experimental Results

The 300-GHz system has been fabricated in TSMC's 28-nm CMOS technology. As shown in Fig. 25, the active area of the

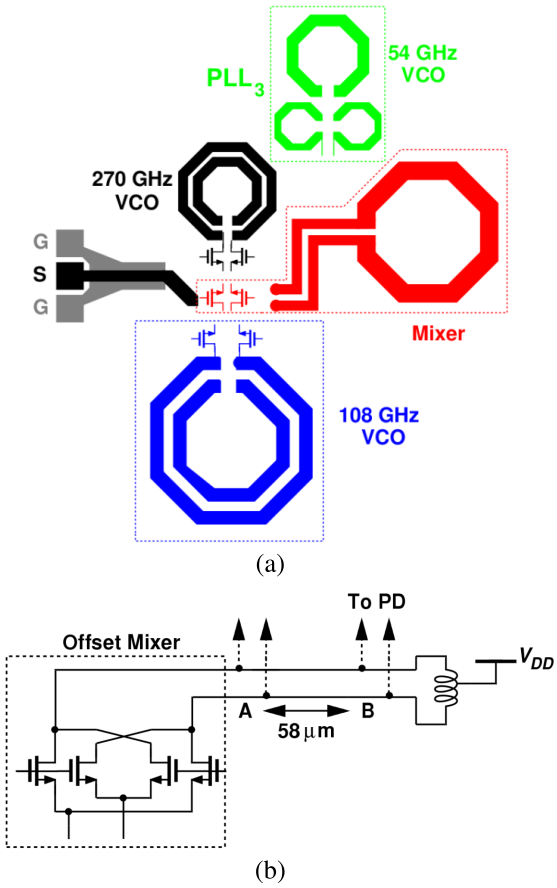



Fig. 24. (a) RX floor plan and (b) series peaking realized in an offset mixer.

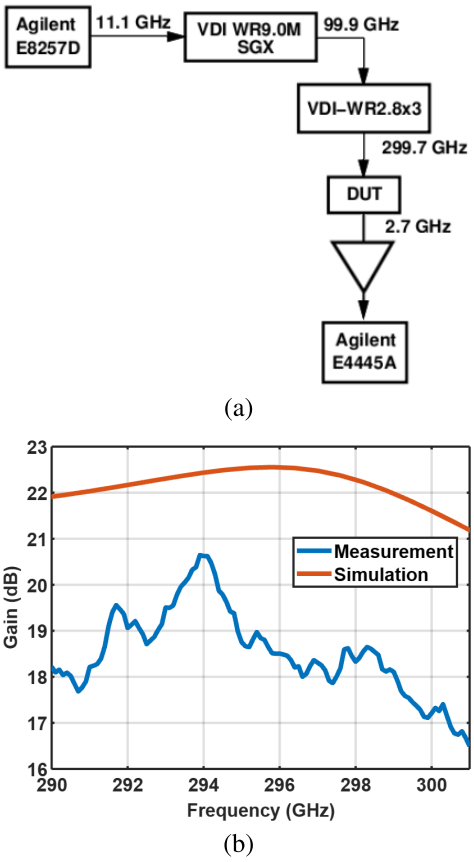



Fig. 26. (a) Receiver gain setup and (b) gain measurement results.

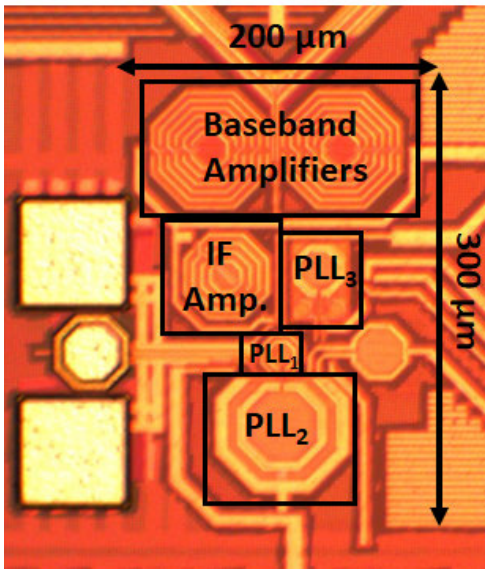



Fig. 25. Rx die micrograph.

die occupies about 200 $\mu$m $\times$ 300 $\mu$m. Such a small footprint makes the system well-suited to beamforming with a large number of elements. The circuit has been tested on a probe station with the RF input applied through a waveguide probe having a loss of 2.2 dB.

Fig. 26(a) depicts the setup for measuring the RX gain and NF. An Agilent E8752D drives a Virginia Diodes' multiply-by-9, which connects to a Virginia Diodes' tripler. The resulting amplitude is controlled by adjusting the output level of the E8257D.

For gain measurements, we first connect the tripler's output to a power meter, the VDIPM5B. Next, we apply the signal to the device under test (DUT), which delivers the baseband output to a spectrum analyzer (SA). Subtracting the 2.2-dB probe loss yields the gain plot shown in Fig. 26(b). The close agreement between these results and simulations indicates that the RF mixer is switched as expected, and hence, the 270-GHz LO swings are as large as the values mentioned in Section VI-C.

The NF measurement presents serious challenges as no specific equipment is available for this purpose at these frequencies. In fact, even an accurate 300-GHz noise source cannot be found. The only solution appears to be the "gain method," whereby a 50-$\Omega$ source resistance, $R_s$, drives the RX (see Fig. 27), and the baseband noise spectrum, $S_{\mathrm{BB}}(f)$, is measured by an SA, We then have

$$\mathrm{NF} = \frac{S_{\mathrm{BB}}(f)}{A_0^2} \cdot \frac{1}{4kTR_S} \tag{6}$$

where $A_0$ denotes the voltage gain from $V_{\mathrm{in}}$ to the baseband output. Such an approach requires both a precise value for $A_0$ and a sufficiently high gain to make the SA's noise floor negligible. The setup in Fig. 26(a) is, thus, used: we simply turn the tripler on to find the gain and turn it off to measure $S_{\mathrm{BB}}(f)$. In this case, the DUT is followed by an off-chip

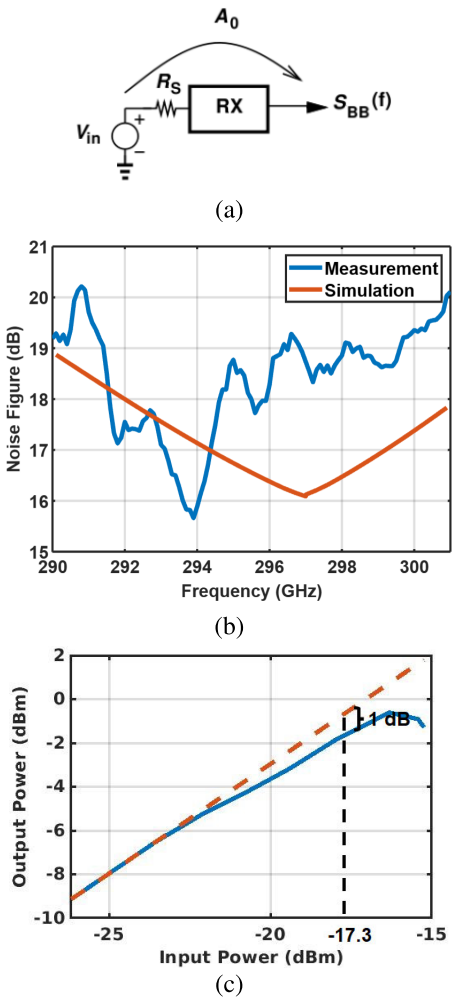



Fig. 27. (a) NF measurement using the gain method, (b) NF measurement results, and (c) 1-dB compression point at 298 GHz.

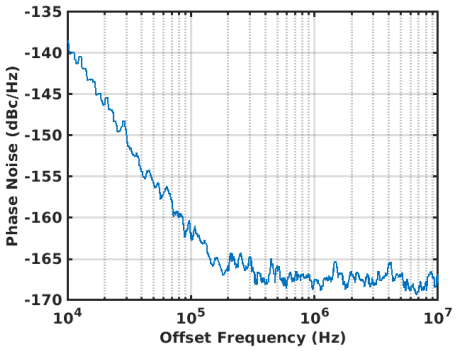



Fig. 28. Crystek's CRBSVS-01-450.000 crystal oscillator phase noise.

amplifier module, so as to overwhelm the SA noise floor. The result is plotted in Fig. 27(b).

The RX nonlinear behavior is depicted in Fig. 27, suggesting an input 1-dB compression point of −17.3 dB.

The phase noise of the LO generation section is measured on a separate chip that excludes the receive path. For this purpose, we examine the phase noise of the crystal oscillator providing $f_{\mathrm{REF}} = 450$ MHz in Fig. 1, the 270-GHz PLL, and the 54-GHz PLL. Crystek's CRBSVS-01-450.000 crystal oscillator exhibits the phase noise profile plotted in Fig. 28,

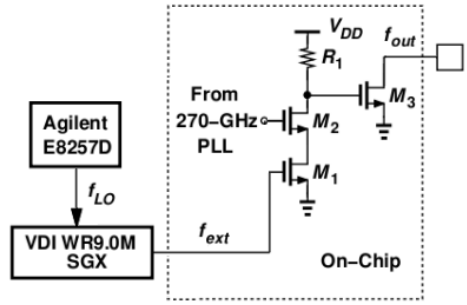



Fig. 29. 270-GHz PN measurement with on-chip mixer.

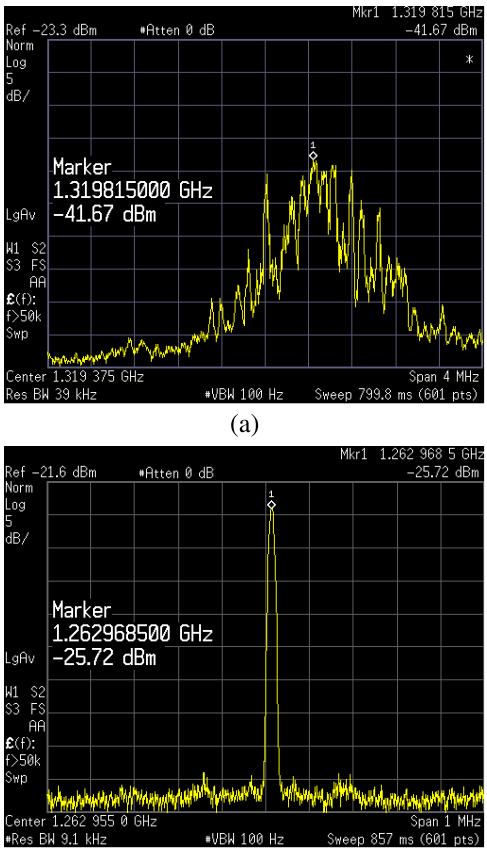
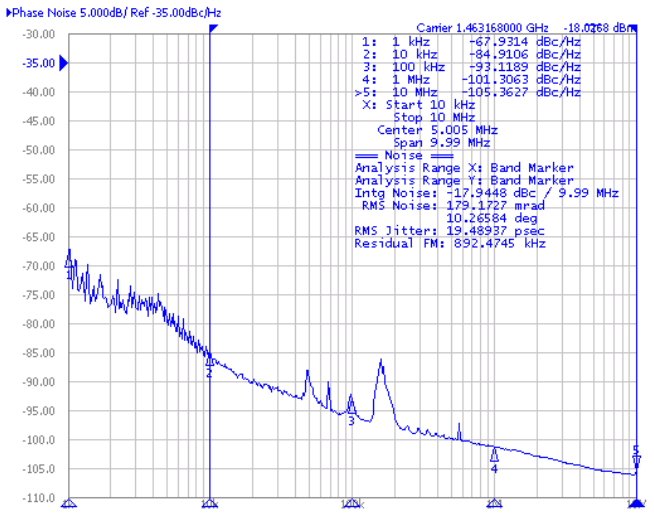



Fig. 30. Output spectra with $f_{\mathrm{ext}} = 89.579$ GHz for (a) unlocked $\mathrm{PLL}_1$ and (b) locked $\mathrm{PLL}_1$.

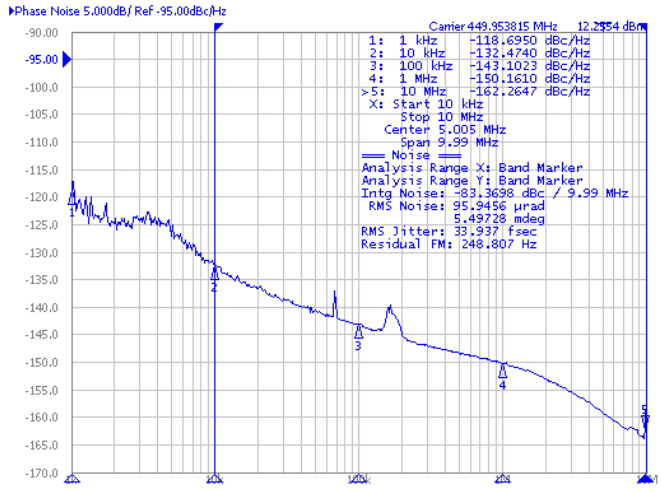
reaching a plateau of about −168 dBc/Hz beyond an offset of 200 kHz.

The 270-GHz PLL output is applied to an on-chip mixer, as shown in Fig. 29, which also receives an external LO frequency of $f_{\mathrm{ext}} \approx 89.579$ GHz from the VDI WR9.0M SGX. Upon mixing the third harmonic of this frequency with the PLL waveform, the circuit delivers $f_{\mathrm{out}} = 1.263$ GHz.

Extreme care has been taken to ensure that the measured output is indeed a downconverted copy of the 270-GHz signal rather than a harmonic of $f_{\mathrm{ext}}$. This is verified by three methods: 1) we change $f_{\mathrm{REF2}}$ in Fig. 1 by $\Delta f$ and observe that $f_{\mathrm{out}}$ changes by $600\Delta f$; 2) to ensure that $f_{\mathrm{out}} = 270 - 3f_{\mathrm{ext}}$, we change $f_{\mathrm{ext}}$ by $\Delta f$ and observe that $f_{\mathrm{out}}$ changes by $3\Delta f$; and 3) we intentionally drive the 108- or 270-GHz PLL out of the lock and compare the resulting downconverted spectrum with that of the locked case. Shown in Fig. 30 are the




(a)




(b)

Fig. 31. (a) 270-GHz PLL PN with $f_{ext} = 89.512$ GHz. (b) 54-GHz PLL divided PN.

unlocked and locked downconverted spectra, suggesting that, when unlocked, the oscillator waveform exhibits high phase noise and some undesired offset mixer spurs in its waveform. However, once the PLL is locked, the mixer spurs vanish, and we obtain a clean signal.

The downconverted output phase noise is depicted in Fig. 31(a). It reaches −105 dBc/Hz at a 10-MHz offset. The spurs in the vicinity of 100-kHz offset are artifacts of the phase noise analyzer (Keysight SSA E5052A). The analyzer also provides less averaging for offsets below 10 kHz, primarily because the settings are so chosen to optimize measurements at higher offsets. The total integrated jitter from 10 kHz to 10 MHz is 105.61 $fs_{rms}$. We note that this is the lowest jitter reported for synthesized frequencies in this range. We estimate the following contributions from different blocks in Fig. 1: 33.9 $fs_{rms}$ due to $PLL_3$, 4.8 $fs_{rms}$ due to $PLL_2$, and 43.3 $fs_{rms}$ due to $PLL_1$.[3]

[3]The discrepancy is attributed to inaccuracies in transistor models in the 270-GHz VCO.

| | This Work | JSSC'19 [7] | MTT-S'20 [8] | APMC'18 [9] | RFIT'17 [10] |
|---|---|---|---|---|---|
| $f_{min}$ (GHz) | 289 | 255 | 278 | 286.5 | 287 |
| $f_{max}$ (GHz) | 305 | 275 | 304 | 313.5 | 320 |
| Gain (dB) | 18 | 3 | −16.5 | −19.5 | −18 |
| Noise Fig. (dB) | 20 | 22.9 | NA | 27 | 25.5 |
| Power (mW) | 52 | 897* | 140* | 650* | 416* |
| Chip area ($mm^2$) | 0.72 | NA | 1.9 | NA | 2.29 |
| Tech. (nm) | 28–nm CMOS | 40–nm CMOS | 65–nm CMOS | 40–nm CMOS | 40–nm CMOS |

*with external LO

Fig. 32. 300-GHz RX comparison with the state-of-the-art.

We should remark that the type-1 architecture employed for the 270-GHz PLL suppresses its VCO flicker phase noise to a lesser extent than could a type-II topology. As a result, both Figs. 21 and 31(a) reveal substantial flicker components.

The measured lock range of the 270-GHz PLL is 5.2 GHz, less than the VCO tuning range. This is partly due to a frequency misalignment between the 108-GHz VCO and the 270-GHz VCO.

The output phase noise of the 54-GHz PLL has also been measured. We monitor the output of the divide-by-15 circuit in Fig. 21(a), obtaining the profile shown in Fig. 31(b). The PN at 54 GHz is $20\log(120) = 41.6$ dB higher. The jitter integrated from 10 kHz to 10 MHz is 33.93 $fs_{rms}$, which is close to the simulated value of 31.25 $fs_{crms}$.

Fig. 32 summarizes the performance of our prototype and compares it to that of the state of the art. In comparison to [10], which requires an external 40-GHz LO, the conversion gain is improved by 36 dB, and power consumption is reduced by a factor of 2.6. In comparison to the RX in [7], which uses an external 44-GHz LO, the conversion gain is improved by about 15 dB, and the power is lowered by a factor of 17.

Another option is to use a sub-harmonic mixer, e.g., as in [34], where $f_{LO}$ is half of the input frequency. This approach provides an NF between 13.9 and 19 dB while requiring an external LO power of +5 dBm, which would be difficult to generate on-chip.

## XI. Conclusion

This article describes a fully integrated 300-GHz RX that consumes less power than the prior art and occupies a small area. A heterodyne architecture is presented, and a number of LO generation techniques are proposed.

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