A 12-Bit 200-MHz CMOS ADC

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***Abstract*—A pipelined ADC incorporates a blind LMS calibration algorithm to correct for capacitor mismatches, residue gain error, and op amp nonlinearity. The calibration applies 128 levels and their perturbed values, computing 128 local errors across the input range and driving the mean square of these errors to zero. Fabricated in 90-nm digital CMOS technology, the ADC achieves a DNL of 0.78 LSB, an INL of 1.7 LSB, and an SNDR of 62 dB at an analog input frequency of 91 MHz while consuming 348 mW from a 1.2 V supply.**

***Index Terms*—Adaptive systems, blind least mean square (LMS) calibration, low-gain op amp, nonlinearity correction, pipelined analog-to-digital converter.**

I. Introduction

THE design of high-speed, high-resolution analog-to-digital converters (ADCs) continues to present greater challenges as the device dimensions and supply voltages are scaled down. While generic issues such as capacitor mismatch provided the impetus for earlier calibration techniques [1], deep-submicron low-voltage technologies have made it increasingly difficult to realize high-gain op amps, requiring additional calibration that corrects for gain error [2]–[16] and nonlinearity [10], [15]. With the declining intrinsic gain of transistors, it is expected that the notion of fast-settling, low-voltage, high-gain op amps will eventually become obsolete.

This paper introduces a blind calibration algorithm that corrects for capacitor mismatch, residue gain error, and op amp nonlinearity. Incorporated in a 12-bit pipelined ADC using an op amp with an open-loop gain of 25, the calibration leads to a measured signal-to-(noise+distortion) ratio (SNDR) of 62 dB at an input frequency of 91 MHz.

Section II of the paper describes the ADC architecture and pipelined ADC modeling concepts that prove essential to calibration. Section III presents the calibration algorithm and discusses its issues. Section IV deals with the design of the building blocks and Section V summarizes the experimental results.

II. ADC Architecture and Modelling

A. ADC Architecture

Fig. 1 shows the architecture of the 12-bit pipelined ADC. It consists of 15[1] 1.5-bit stages followed by a one-bit stage, producing digital outputs $D_1, \ldots, D_{16}$. Since the design employs a high-speed, inevitably low-gain op amp, the third-order nonlinearity is corrected in the first two stages. Moreover, the offsets, gain errors, and mismatches are corrected in all of the stages. In Fig. 1, the digital blocks denoted by $1/G_n$ represent inverse gain operation and those shown as $f_n^{-1}(x)$ serve as the inverse of each stage's nonlinear characteristic. The least-mean-square (LMS) machine adapts the coefficients of these blocks to drive a cost function to zero (Section III). It is assumed that both $f_n(x)$ and $f_n^{-1}(x)$ can be approximated by a third-order polynomial, i.e., higher orders are negligible.

The ADC avoids a dedicated front-end sample-and-hold amplifier (SHA) [4], [17], eliminating the additional noise and power consumption associated with such a circuit. That is, the multiplying digital-to-analog converter (MDAC) and the 1.5-bit ADC in the the first stage sample the signal simultaneously. Such an approach nonetheless entails two issues. First, the mismatches between the delays of the two paths lead to inconsistent sampled values. Second, the time consumed by the 1.5-bit ADC limits the time available for the MDAC settling because the two must add up to half a clock cycle.

It is worth noting some of the shorcomings of the prior art in relation to low-voltage, deep-submicron realizations of the pipelined architecture. Summarized in Table I, these shortcomings are avoided in this work.

B. ADC Modeling

The calibration algorithm proposed in Section III views the operation and non-idealities of a pipeline from a certain perspective. In this section, we formulate the behavior of the ADC so as to arrive at this perspective.

Suppose the open-loop input-output static characteristic of an op amp can be approximated by a third-order polynomial across the voltage range of interest:

$$V_{\text{out}} \approx \alpha_1 V_{\text{in}} + \alpha_2 V_{\text{in}}^2 + \alpha_3 V_{\text{in}}^3. \tag{1}$$

If placed in a feedback circuit, the op amp sustains an input voltage that is the inverse of the above function. Approximating the inverse function also by a third-order polynomial,

$$V_{\text{in}} \approx \beta_1 V_{\text{out}} + \beta_2 V_{\text{out}}^2 + \beta_3 V_{\text{out}}^3, \tag{2}$$

we substitute for V_{out} from (1), expand, and equate the like powers. It follows that

$$\beta_1 = \frac{1}{\alpha_1} \tag{3}$$

$$\beta_2 = \frac{-\alpha_2}{\alpha_1^3} \tag{4}$$

$$\beta_3 = \frac{2\alpha_2^2}{\alpha_1^5} - \frac{\alpha_3}{\alpha_1^4}. \tag{5}$$

We apply the above results to an MDAC employing such an op amp. Depicted in Fig. 2 are two MDAC topologies, where

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[1]Since the gain of each stage is approximately equal to 1.72, a total of 15 stages are required to provide 2 additional bits for calibration and achieve 12-bit linearity.

TABLE I
SUMMARY OF PRIOR ART

Reference	Gain Error Correction	Capacitor Mismatch Correction	Nonlinearity Correction	Notes
[2]	√	√		Restricts input signal bandwidth to $2/3$ of Nyquist.
[4], [5]	√	√		Addition of random input reduces dynamic range.
[6]	√	√		
[7]		√		
[8]	√			
[22]	√	√	√	
[9]	√			Reduced input dynamic range, accurate calibration signals, and slow-but-accurate ADC.
[10]	√		√	Does not correct capacitor mismatch, requires additional bit for stage under calibration, corrects nonlinearity of only one stage, and assumes a calibrated back end.
[11]	√	√		Requires 13-b accurate DAC for calibration.
[12], [13]	√	√		Requires one clock for ADC (f_C) and one clock for SHA (f_S).
[14]	√	√		Needs 13-b accurate $\pm V_{REF}/4$ for calibration; Mismatch between main signal path and slow ADC path introduces error.
[15]	√	√	√	Requires 13-b accurate signal for calibration, one clock for ADC (f_C), and one clock for SHA (f_S). Also, for background calibration $f_C > f_S$.

C_X denotes the input capacitance of the op amp. In the "flip-around" structure of Fig. 2(a), capacitor mismatch results in *unequal* voltage gains for the input and the reference. Specifically, with a linear op amp having a gain of A,

$$V_{\rm out} = \frac{1+\frac{C_S}{C_F}}{1+\frac{1}{A}\left(1+\frac{C_S}{C_F}+\frac{C_X}{C_F}\right)}V_{\rm in} + \frac{\frac{C_S}{C_F}}{1+\frac{1}{A}\left(1+\frac{C_S}{C_F}+\frac{C_X}{C_F}\right)}KV_{\rm REF} \quad (6)$$

in the hold mode. On the other hand, the "non-flip-around" topology of Fig. 2(b) presents equal gains and nonlinearities to the input and the reference by subtracting the latter from the former *before* amplification. The penalty is somewhat lower loop gain and slower settling. This distinction between the two topologies proves important as it implies fewer adaptation coefficients for the circuit of Fig. 2(b) and hence less complexity in the digital calibration machine. Applied to the non-flip-around MDAC in this work, the proposed calibration algorithm can be used with the flip-around topology as well but it would require twice[2] the number of adaptation coefficients. In Fig. 2, $D_{\rm in}$ and $D_{\rm out}$ represent the digital equivalents of $V_{\rm in}$ and $V_{\rm out}$, respectively, while D_1 denotes the output of the sub-ADC.

For the MDAC in Fig. 2(b), the conservation of charge from the sampling mode to the hold mode yields

$$C_S V_{\rm in} = (KV_{\rm REF} - V_X)C_S + V_X C_X + (V_{\rm out} - V_X)C_F \quad (7)$$

regardless of the op amp characteristic. Substituting for V_X from (2), we have

$$V_{\rm in} = KV_{\rm REF} + \left(\frac{C_F}{C_S}+\gamma\beta_1\right)V_{\rm out} + \gamma\beta_2 V_{\rm out}^2 + \gamma\beta_3 V_{\rm out}^3 \quad (8)$$

where

$$\gamma = \frac{C_X - C_F}{C_S} - 1$$

We now express the digital equivalent of the input and output of the stage as $D_{\rm in} \equiv V_{\rm in}/V_{\rm REF}$ and $D_{\rm out} \equiv V_{\rm out}/V_{\rm REF}$, respectively. Also, from Fig. 2(b), $D_1 \equiv K$. Thus, (8) can be written as

$$D_{\rm in} = D_1 + \left(\frac{C_F}{C_S}+\gamma\beta_1\right)D_{\rm out} + \gamma\beta_2 D_{\rm out}^2 + \gamma\beta_3 D_{\rm out}^3. \quad (9)$$

Note that this representation also includes capacitor mismatch (departure of C_F/C_S from 2.0) and residue gain error (departure of β_1 from 0).

[2]Equation (6) indicates that calibrating for the linear gain error of the flip-around topology requires the estimation of two coefficients. Similarly, for third-order nonlinearity, six coefficients are necessary.

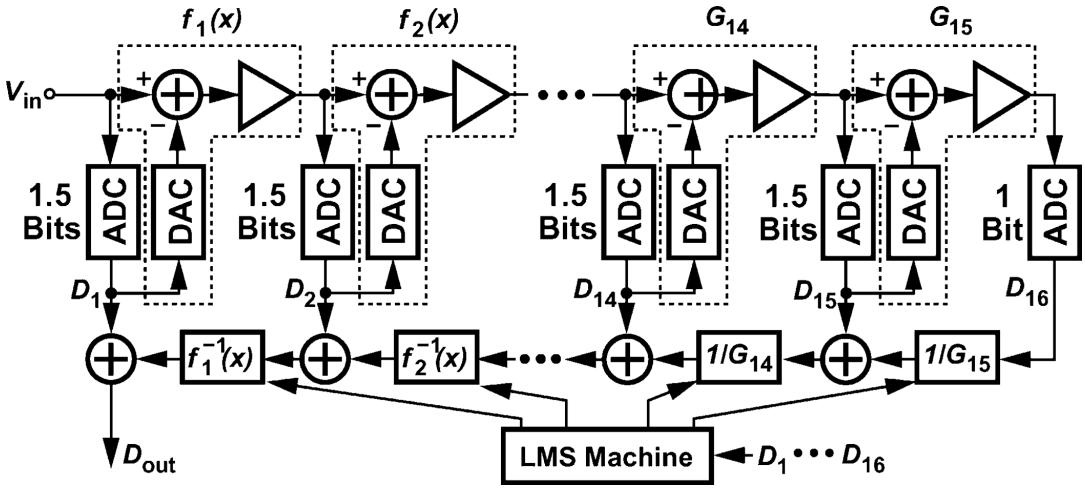

Fig. 1. ADC architecture.

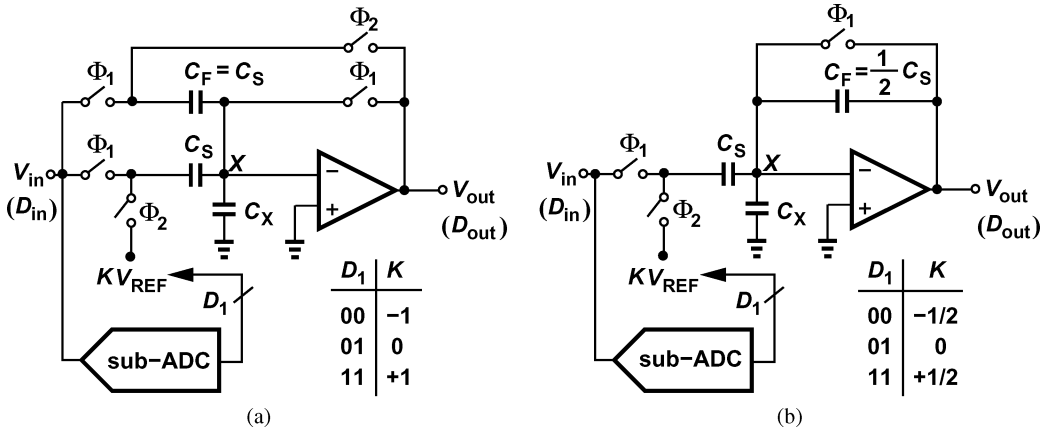

Fig. 2. 1.5-bit/stage (a) flip-around, and (b) non-flip-around MDACs.

The inverse function expressed by (9) can cancel the nonidealities of the MDAC stage if the coefficients of D_{out}^n are set properly. The task of calibration therefore reduces to accurate estimation of these coefficients.

The foregoing results can be extended to multiple stages in a pipeline. Rewriting (9) in abbreviated form

$$D_{\text{in}} = D_1 + \eta_1 D_{\text{out}} + \eta_2 D_{\text{out}}^2 + \eta_3 D_{\text{out}}^3 \tag{10}$$

where $\eta_1 = C_F/C_S + \gamma\beta_1$, $\eta_2 = \gamma\beta_2$, and $\eta_3 = \gamma\beta_3$, we have

$$\begin{aligned} D_{\text{in},1} &= D_1 + \eta_{1,1} D_{\text{out},1} + \eta_{2,1} D_{\text{out},1}^2 \\ &\quad + \eta_{3,1} D_{\text{out},1}^3 \end{aligned} \tag{11}$$

$$\begin{aligned} D_{\text{in},2} &= D_2 + \eta_{1,2} D_{\text{out},2} + \eta_{2,2} D_{\text{out},2}^2 \\ &\quad + \eta_{3,2} D_{\text{out},2}^3 \end{aligned} \tag{12}$$

$$\begin{aligned} D_{\text{in},3} &= D_3 + \eta_{1,3} D_{\text{out},3} + \eta_{2,3} D_{\text{out},3}^2 \\ &\quad + \eta_{3,3} D_{\text{out},3}^3 \end{aligned} \tag{13}$$

$$\vdots$$

$$\begin{aligned} D_{\text{in},N} &= D_N + \eta_{1,N} D_{\text{out},N} + \eta_{2,N} D_{\text{out},N}^2 \\ &\quad + \eta_{3,N} D_{\text{out},N}^3 \end{aligned} \tag{14}$$

where $D_{\text{in},j}$ and $D_{\text{out},j}$ are digital equivalents of the input and output of stage number j, respectively. Also, note that $D_{\text{in},j+1} = D_{\text{out},j}$. The key point here is that the digital representation of the main analog input can be obtained recursively, beginning from the last stage and moving toward the first. This recursion is shown in Fig. 1, where D_{16} is applied to a gain correction block $1/G_{15}$, combined with D_{15}, applied to the next correction block, and so on. With differential operation and small mismatches, $\eta_{2,j} = 0$. Also, since the nonlinearity is not corrected for $j > 2$, $\eta_{3,j} = 0$ for $j > 2$.

The above observations suggest that the digital correction chain shown in Fig. 1 can be viewed as a finite impulse response (FIR) filter whose taps are defined by $\eta_{1,j}$ for $j = 1$–15 and $\eta_{3,j}$ for $j = 1$–2. Fig. 3 conceptually depicts a possible implementation of the FIR filter, which requires 8 multipliers and 15 two-input adders.

III. Calibration Concept

The proposed calibration algorithm begins in the foreground mode and subsequently moves to background. The algorithm avoids or significantly alleviates the drawbacks highlighted in Table I for the prior art.

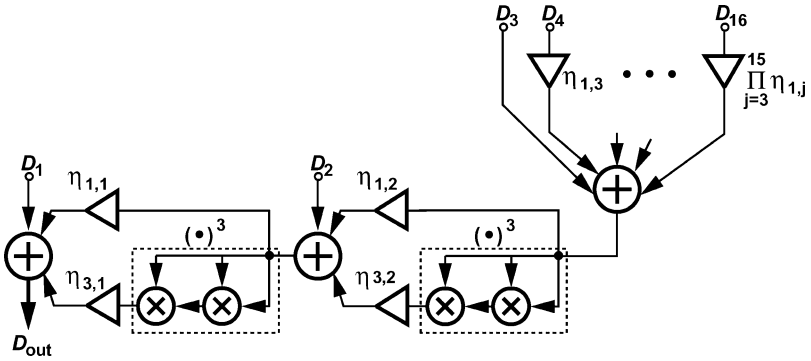

Fig. 3. Conceptual implementation of FIR filter ($D_1 - D_{16}$ are aligned by means of flip-flops not shown here).

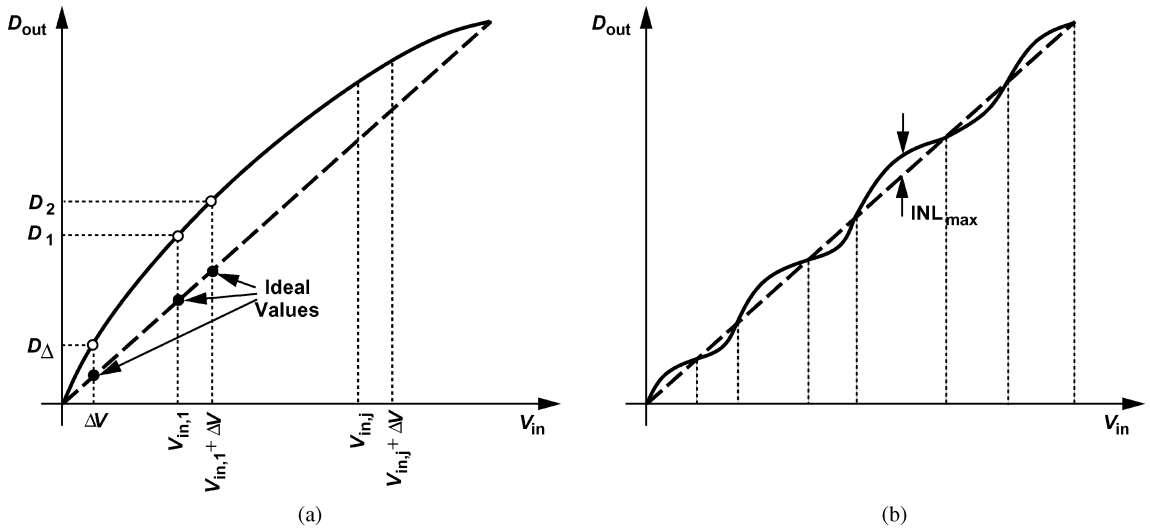

Fig. 4. (a) Calibration concept. (b) Input-output characteristic after calibration.

A. Foreground Mode

Fig. 4(a) conceptually illustrates the algorithm. Calibration begins by digitizing three dc levels: $V_{\mathrm{in},1}$, $V_{\mathrm{in},1}+\Delta V$, and ΔV, where ΔV denotes a relatively small increment, e.g., 64 LSB. In the ideal case, all three outputs lie on a straight line and $D_2 - D_1 = D_\Delta$, suggesting that the difference between $D_2 - D_1$ and D_Δ can serve as the error to be minimized. In other words, we surmise that, *if* $D_2 - D_1$ and D_Δ are made equal, *then* all three fall on the ideal characteristic. We elaborate on this conjecture in Section III-B.

The above measurement must be repeated for various input levels, $V_{\mathrm{in},j}$, and their perturbed values, $V_{\mathrm{in},j} + \Delta V$, such that the entire range is swept. If the cost function is defined as $\epsilon = [(D_2 - D_1) - D_\Delta]^2$ for different j, then we may expect that minimizing it moves D_Δ to its ideal value and hence D_2 and D_1 (for each $V_{\mathrm{in},j}$) also to their ideal values [Fig. 4(b)]. To achieve a small integral nonlinearity, $INL_{\max}$ in Fig. 4(b), the spacing between the input levels at which the incremental measurement is performed must remain below a certain amount. In this work, the spacing is equal to 32 LSB, i.e., the characteristic is corrected at 128 points.

Before describing the details of the algorithm we make a number of remarks. First, the perturbation voltage, ΔV, need not be known accurately—because its digitized value is incorporated in the adaptation—but it must remain constant as j covers the input range. This is guaranteed by design: a single capacitor tied to a virtual ground and switched between zero and full scale realizes this increment. Second, as evident from the above description and Fig. 4(b), the input levels, $V_{\mathrm{in},j}$, need not be equally spaced, implying that the DAC generating the various levels need not be linear. Third, the illustration in Fig. 4 assumes a zero offset for the characteristic, but the digital output corresponding to the overall offset (with the analog input set to zero), D_{OS}, can simply be subtracted from the cost function, i.e., $\epsilon^2 = [(D_2 - D_1) - D_\Delta - D_{OS}]^2$. Fourth, an excessively small value of ΔV nulls the autocorrelation of the derivative of the cost function (Appendix A), prohibiting convergence. In this work, convergence fails if $\Delta V < 32$ LSB.[3]

In a 1.5-bit/stage architecture, the increment requires further attention. As illustrated in Fig. 5(a), if ΔV is added to all input levels, then the residue overflows. For this reason, ΔV is subtracted from V_{in} for $V_{\mathrm{in}} > -V_{\mathrm{REF}}/4$, which is simply decided by the 1.5-bit flash ADC in the first stage [Fig. 5(b)].

B. Properties of the Cost Function

The foregoing description of the calibration algorithm is predicated on the assumption that minimizing the cost function,

[3]This has been determined through extensive MATLAB simulations.

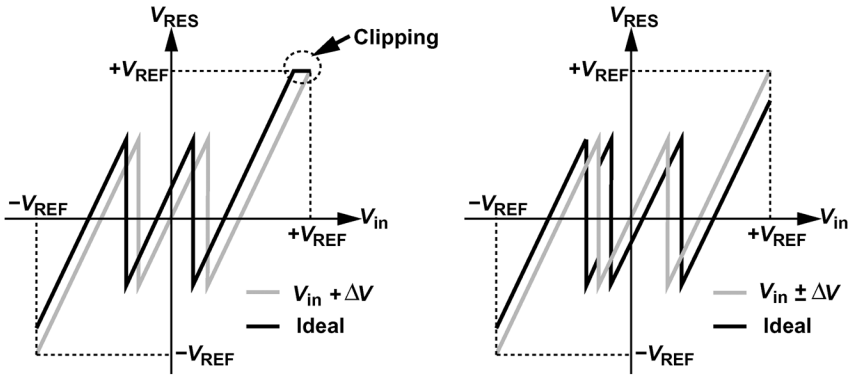

Fig. 5. Residue characteristic with (a) ΔV added to all input levels, and (b) ΔV subtracted for $V_{\rm in} > -V_{\rm REF}/4$.

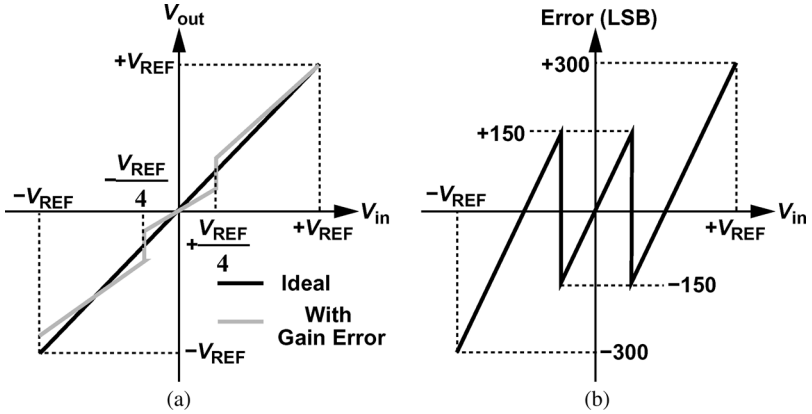

Fig. 6. (a) Input-output characteristic with 15% gain error. (b) Resulting INL profile.

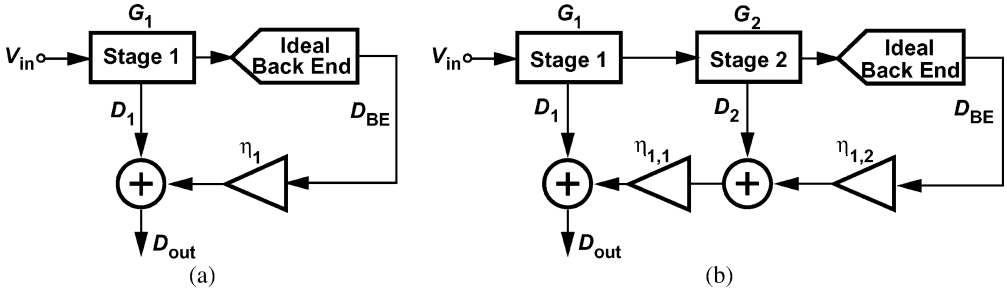

Fig. 7. Pipeline ADC with ideal back-end and non-ideal (a) stage 1, (b) stage 1 and stage 2.

$\epsilon^2 = [(D_2 - D_1) - D_\Delta]^2$, across the entire input range eventually transforms the characteristic in Fig. 4(a) to that in Fig. 4(b). In this section, we study the properties of ϵ so as to develop insight into the convergence of the calibration algorithm.

Let us begin with a simple case: the first stage of the pipeline suffers from only a gain error while the remaining stages are ideal. (We say the ADC has an "ideal back-end.") The input-output characteristic of such a system is shown in Fig. 6(a), where large jumps appear at $V_{\rm in} = \pm V_{\rm REF}/4$. The INL profile is plotted in Fig. 6(b). As shown in Fig. 7(a), the digital calibration must divide the output of the back-end, D_{BE}, by the gain of the first stage, G_1 (ideally equal to 2), and add the result to the output of the first stage, D_1. In accordance with the notation in (10),

$$D_{\rm out} = D_1 + \eta_1 D_{BE} \tag{15}$$

where η_1 must converge to $1/G_1$. This output is computed for $V_{{\rm in},j}$, $V_{{\rm in},j} + \Delta V$, and ΔV, thereby yielding, respectively:

$$D_{{\rm out},j} = D_{1,j} + \eta_1 D_{BE,j} \tag{16}$$

$$D_{{\rm out},j,\Delta} = D_{1,j,\Delta} + \eta_1 D_{BE,j,\Delta} \tag{17}$$

$$D_{{\rm out},\Delta} = D_{1,\Delta} + \eta_1 D_{BE,\Delta}. \tag{18}$$

The mean square error is then expressed as

$$\epsilon^2_{\rm MSE} = \frac{1}{128}\sum_{j=1}^{128} \left[|D_{{\rm out},j} - D_{{\rm out},j,\Delta}| - D_{{\rm out},\Delta}\right]^2. \tag{19}$$

Fig. 8(a) plots $\epsilon_{\rm MSE}$ as a function of η_1, revealing a minimum close to zero at $1/G_1 = 0.56$. This plot is obtained using a MATLAB simulation whereby the gain of the first stage is set

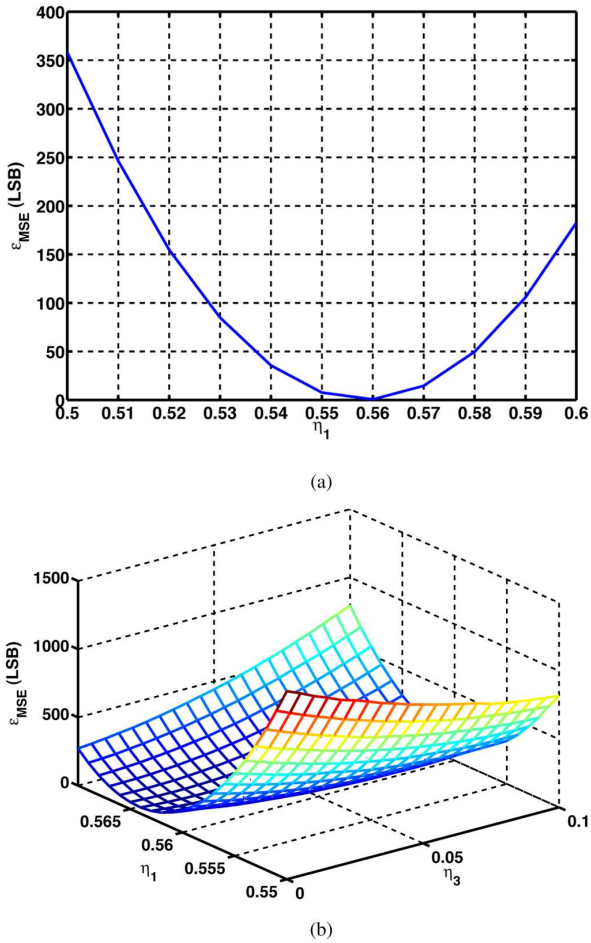

Fig. 8. MSE error curve with one non-ideal stage including (a) gain error, and (b) gain error and nonlinearity.

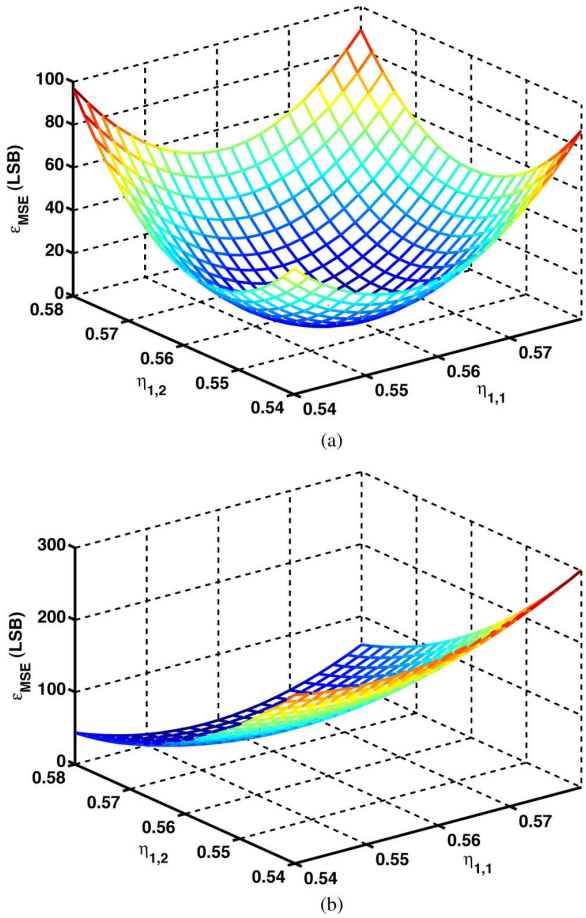

Fig. 9. MSE curves with two non-ideal stages including (a) finite op amp gain, and (b) finite op amp gain and capacitor mismatch.

to 1.78. The proof of convergence of the LMS procedure for this case is shown in Appendix A.

We next assume that the first stage also suffers from third-order nonlinearity and rewrite (15) as

$$D_{\text{out}} = D_1 + \eta_1 D_{BE} + \eta_3 D_{BE}^3. \tag{20}$$

The LMS procedure must therefore search for optimum values of η_1 and η_3 so as to minimize ϵ_{MSE}. Fig. 8(b) plots ϵ_{MSE} across a range of η_1 and η_3 when the first stage characteristic is expressed as $V_{\text{out}} = \alpha_1 V_{\text{in}} + \alpha_3 V_{\text{in}}^3$, and $\alpha_1 = 1.78$ and $\alpha_3 = -0.3$. As expected ϵ_{MSE} reaches a minimum for $\beta_1 = 1/\alpha_1$ and $\beta_3 = -\alpha_3/\alpha_1^4$. The proof of convergence is shown in Appendix A.

Lastly, let us assume the first two stages suffer from gain error, but the remaining stages act as an ideal back-end [Fig. 7(b)]. That is,

$$D_{\text{out}} = D_1 + \eta_{1,1}(D_2 + \eta_{1,2} D_{BE})$$

where $\eta_{1,1}$ and $\eta_{1,2}$ denote the inverse of the gains of the first and the second stages, respectively. Ideally, $\eta_{1,1} = \eta_{1,2} = 0.5$ and $D_{\text{out}} = D_1 + D_2/2 + D_{BE}/4$. When sensing $V_{\text{in},j}$, $V_{\text{in},j} + \Delta V$, and ΔV, the ADC produces, respectively,

$$\begin{aligned} D_{\text{out},j} &= D_{1,j} + \eta_{1,1}(D_{2,j} + \eta_{1,2} D_{BE,j}) \\ D_{\text{out},j,\Delta} &= D_{1,j,\Delta} + \eta_{1,1}(D_{2,j,\Delta} + \eta_{1,2} D_{BE,j,\Delta}) \\ D_{\text{out},\Delta} &= D_{1,\Delta} + \eta_{1,1}(D_{2,\Delta} + \eta_{1,2} D_{BE,\Delta}). \end{aligned}$$

In this case, the LMS must seek the values of $\eta_{1,1}$ and $\eta_{1,2}$ which minimize ϵ_{MSE} [(19)]. Fig. 9(a) plots ϵ_{MSE} for a range of $\eta_{1,1}$ and $\eta_{1,2}$ if the closed-loop gains of the first and second stages are equal to 1.78. With capacitor mismatch, on the other hand, the behavior becomes asymmetric [Fig. 9(b)] while still exhibiting a single minimum in the region of interest.

The above development can be extended to N stages having both gain error and nonlinearity, with the overall ϵ_{MSE} curve still displaying a minimum. The LMS procedure thus adjusts $(\eta_{1,1}, \eta_{3,1})$ in the first stage, $(\eta_{1,2}, \eta_{3,2})$ in the next stage, etc., so as to drive ϵ_{MSE} towards the minimum.

Proper convergence of the algorithm requires that some estimate of the gain errors and nonlinear coefficients be provided as a starting point. Fortunately, the closed-loop MDAC used in

[4]If the calibration inputs are applied as a ramp, the LMS engine sees a decreasing error as the input goes from $-V_{\text{REF}}$ to 0 and an increasing error as the input goes from 0 to $+V_{\text{REF}}$. If the ramp is repeated, then the LMS engine updates the coefficients either less aggressively ($-V_{\text{REF}}$ to 0) or more aggressively (0 to $+V_{\text{REF}}$), causing oscillation around the converged value.

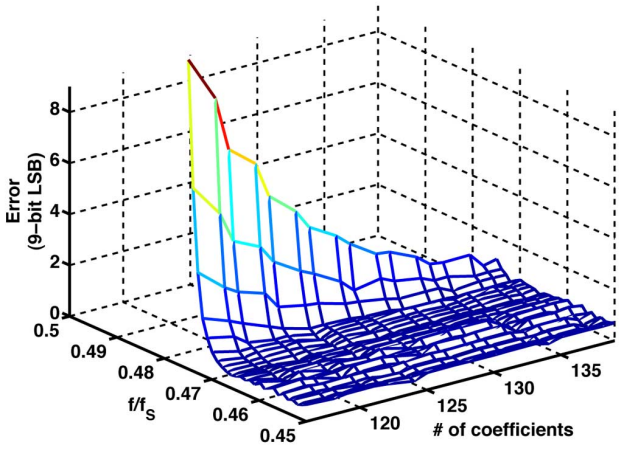

Fig. 10. Interpolation error as a function of input frequency and number of taps.

this work yields relatively predictable analog characteristics, allowing the initial estimates to be close to the final values. For example, with a nominal open-loop op amp gain of 25, the closed-loop gain remains in the vicinity of 1.8. Thus, the initial estimate is chosen equal to $1/1.8 = 0.55$. Simulations indicate that even an initial estimate of 0.5 guarantees convergence.

Another property of the algorithm is that it converges only if $V_{\text{in},j}$ are applied in a random sequence rather than monotonically from zero to full scale. Otherwise, the coefficients oscillate around their desired values.[4] Thus, the ADC includes a 7-bit pseudorandom generator that selects one of 128 levels with uniform distribution.

Lastly, the calibration signals $V_{\text{in},j}$, $V_{\text{in},j} + \Delta V$, and ΔV are applied at full clock rate, thereby correcting for incomplete settling components in the MDAC output. But, the LMS update is run at 6.25 MHz, i.e., 1/16 of the clock frequency.

It is worth mentioning that, in contrast to the design reported in [10], the proposed approach: 1) calibrates for capacitor mismatches; 2) need not increase by one bit the resolution of the stage to be calibrated; 3) calibrates the nonlinearity of two stages; and 4) requires no "ideal" back-end because it calibrates all of the stages concurrently.

C. Background Mode

While a closed-loop MDAC exhibits more stable linear and nonlinear coefficients than does an open-loop residue amplifier, temperature variations may still require frequent calibration to retain 12-bit precision. The calibration concept illustration in Fig. 4 can be placed in the background mode by occasionally digitizing not the analog input but $V_{\text{in},j}$, $V_{\text{in},j} + \Delta V$, and ΔV, where $V_{\text{in},j}$ denotes one of the 128 dc levels. Such a measurement in turn demands an input sample to be occasionally skipped. As described in [3], the skipped sample can be reconstructed by nonlinear interpolation if the maximum input frequency is slightly lower than half of the sampling rate, f_s.

Fig. 10 plots the simulated performance degradation of the ADC as a function of the back-off from the Nyquist rate and the number of taps in the interpolation filter.[5] If 1) one out of 16,384 samples is skipped; 2) the input frequency is limited to 94% of $f_s/2$; and 3) the nonlinear interpolation filter has 122 coefficients to produce an interpolated value with 9-bit accuracy, then the average SNR degrades by 0.1 dB. Under these conditions, the overall characteristic is swept every $16384 \times 128 \times 2 \approx 4.1$ million samples, i.e., 21 ms. (Since the interpolated signal is only 9-bit accurate, it yields a lower SNR for the skipped sample but little degradation in the average SNR.)

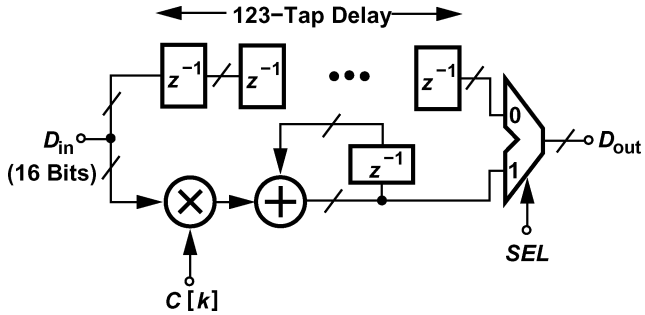

Fig. 11. Interpolation filter.

The interpolation filter can be implemented by a multiplier/accumulator (MAC) block. Fig. 11 depicts the implementation of the 122-tap interpolation filter, where D_{in} is the 16-bit digital output of the ADC. Operating on the unskipped samples, the upper path delays D_{in} by 123 clock cycles. The lower path, on the other hand, performs interpolation on the past 122 values and future 122 values to provide the present value, $D_{\text{out}}[0]$. Specifically, from [2] and [3]:

$$D_{\text{out}}[0] = \sum_{k=-1}^{-122} D_{\text{in}}[k]C_k + \sum_{k=1}^{122} D_{\text{in}}[k]C_k \qquad (21)$$

where C_k is formulated in [3].

The constant coefficients C_k are stored in a memory of size 1.9 kbits. The SEL signal selects the interpolated value every 16,384 clock cycles with a latency of 122 clock cycles.

IV. Circuit Implementation

A prototype 12-bit pipelined ADC has been designed and fabricated in 90-nm CMOS technology. This section describes the implementation details of the prototype.

A. Input Sampling Network

As mentioned in Section II, the ADC's first stage employs simultaneous sampling in the MDAC and the flash converter to avoid the noise, nonlinearity, and power dissipation of a front-end sample-and-hold circuit.[6] Fig. 12 illustrates the input sampling network in simplified form. Capacitor $C_S (= 4\text{ pF})$ is

[5]The interpolated sample is produced with 9-bit resolution. Higher resolutions require a greater latency. The latency due to interpolation may prove undesirable in some applications.

[6]Such a circuit would consume about as much power as the first MDAC, 192 mW.

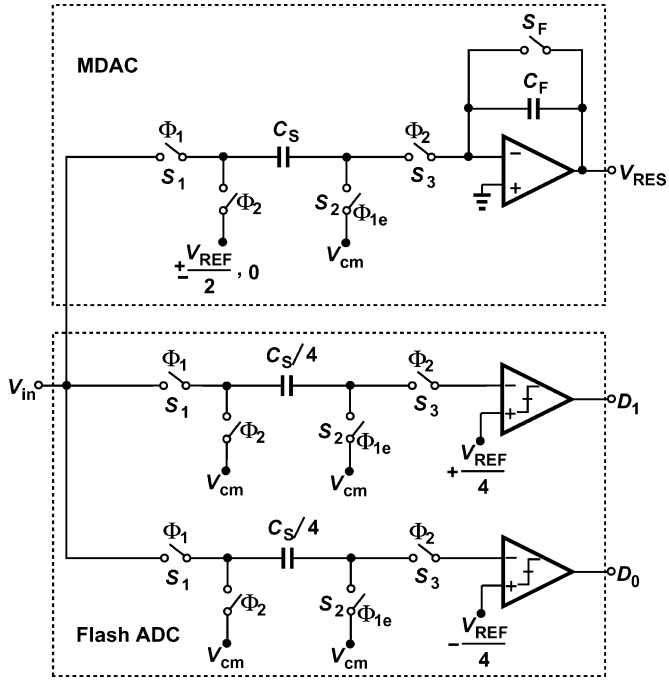

Fig. 12. Path matching in the sampling network.

chosen such that the noise voltage, $\sqrt{2kT/C_S}$ (for differential implementation), falls below 0.2 LSB, degrading the SNR by 1.1 dB.

The absence of a front-end SHA dictates that the MDAC and comparator sampling networks in Fig. 12 exhibit closely-matched time constants and sampling points [4], [17]. Since the comparator does not create a virtual ground at its input, switches S_2 and S_3 have been added to each circuit such that the sampling point is defined by Φ_{1e} and S_2, and the acquisition time constant by the on-resistance of S_1 and S_2 and the sampling capacitor (C_S or $C_S/4$). Random mismatches between the two networks may still yield a sampling discrepancy of several LSBs, but the 1.5-bit/stage architecture accommodates such errors. Fig. 13 shows the cross section of the structure used for the capacitors. The capacitance is obtained primarily from the lateral field, and the "top plate" is shielded by the "bottom plate". Moreover, the bottom plate is shielded from adjacent geometries by a ground plate.

B. Bootstrapped Switch

The low supply voltage and high linearity required in the design necessitate bootstrapping for the front-end switches. Shown in Fig. 14, the bootstrap circuit is adapted from [18]. With $C_S = 4$ pF, the main sampling switch has a W/L of 128 μm/0.1 μm and C_B is chosen equal to 2 pF so as to minimize charge sharing between it and the sampling switches. A 5-Ω metal resistor is placed in series with the main sampling switch to further linearize it.[7] Simulations indicate that the sampling circuit (in differential form) exhibits distortion components about 90 dB below the full-scale at an input frequency of 97 MHz.

Bootstrapping is applied to a number of other switches in the design to increase their overdrive voltage though their linearity is not critical. For example, S_F and S_2 in Fig. 12 are tied to a common-mode voltage approximately equal to $V_{DD}/2$, thus suffering from a small overdrive voltage and high sensitivity to threshold and CM level variations. Bootstrapping allows the use of small, efficient switches here.

C. Calibration DAC

As described in Section III, the calibration proceeds by digitizing $V_{in,j}$, $V_{in,j} - \Delta V$, and ΔV as j goes from 1 to 128. Thus, $V_{in,j}$ must be produced by a DAC. While the INL of the DAC is not critical, its interface with the ADC must settle fast enough such that the ADC can sample $V_{in,j}$ in half a clock cycle (in both the foreground and background modes). With a 4-pF sampling capacitor, it is extremely difficult to utilize a resistor ladder for this purpose. Fortunately, it is possible to decompose the main sampling capacitor into 128 equal units and reconfigure them to form the calibration DAC. Fig. 15 shows the implementation of the front end. Capacitors $32C_{u1}$, $16C_{u1}$, etc., collectively form the 4-pF sampling capacitor and also operate as the reference DAC. To apply $V_{in,j}$, the switches connected to V_{in} are turned off and the left plates of the capacitors are switched to $+V_{REF}$ or $-V_{REF}$ according to the digital setting.

The minimum value of C_{u2} in Fig. 15 is determined by physical dimensions and matching requirements. The use of binary weighting simplifies the logic while potentially creating non-monotonicity if the unit capacitors do not match to a 7-bit level. However, the calibration still operates correctly even if the DAC characteristic is non-monotonic. This is because, as mentioned in Section III, the $V_{in,j}$ levels are selected randomly from the 128 possible values. In this design, C_{u2} is constructed as shown in Fig. 13 with $W = 2.5$ μm and a finger length of 7 μm, assuming a value of 15 fF.

D. Op Amp

The speed, noise, and dynamic range of the ADC greatly hinge upon the performance of the op amp used in the MDAC. The op amp topology shown in Fig. 16 is a candidate for high-speed, nearly rail-to-rail operation. The circuit avoids cascode devices, thus operating as a true two-pole system (before compensation) and lending itself more easily to compensation. Furthermore, simple common mode feedback (CMFB) provided by R_1–R_2 and R_3–R_4 allows fast settling of the CM levels, avoiding differential settling components that typically arise in nonlinear CMFB networks. Note that the current mirror action between M_3–M_4 and M_7–M_8 defines the output branch bias currents as an accurate multiple of I_{SS}. Current source I_1 creates a level shift of $R_3 I_1/2$ ($= R_4 I_1/2$) at the output, yielding an output CM level equal to $V_{GS5} + R_3 I_1/2$, which can be set to approximately $V_{DD}/2$.

Employing minimum channel length for all of the transistors in the signal path, the op amp of Fig. 16 offers an open-loop

[7]In order to reduce the variation of switch resistance by <5%, the switch had to be scaled up by 10%. Adding a 5-Ω metal resistor (which is part of metal routing) reduces the variation without increasing the switch size.

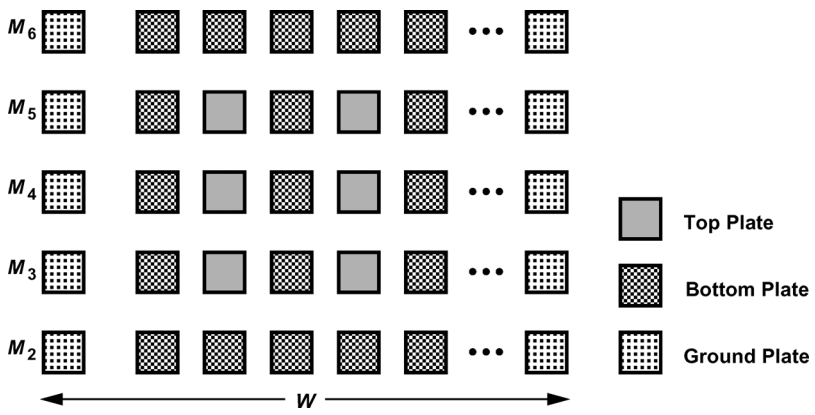

Fig. 13. Cross section of fringe capacitor structure.

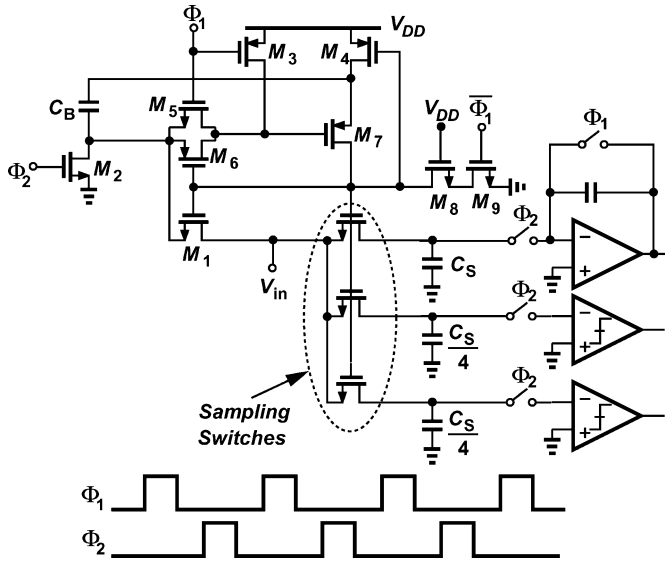

Fig. 14. Bootstrap circuit.

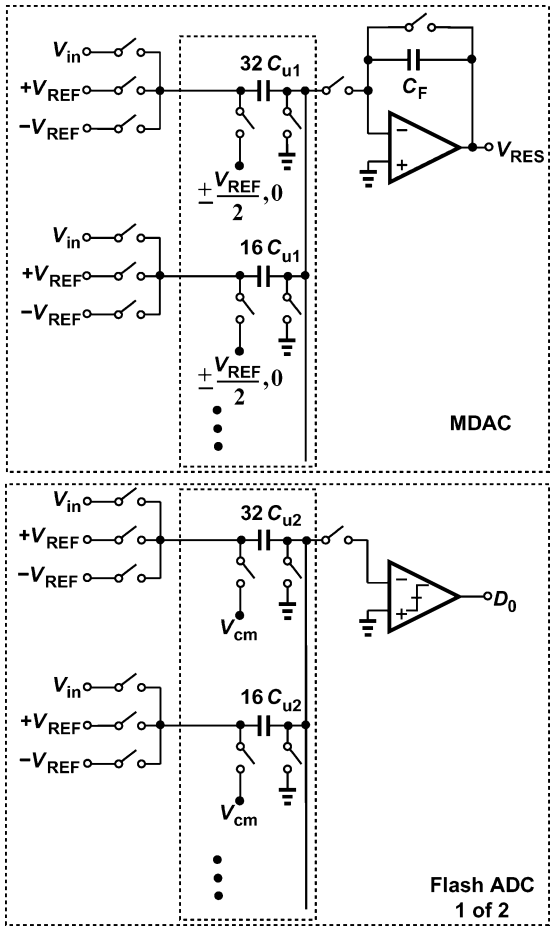

Fig. 15. Front-end sampling network.

gain of only 28 dB, creating substantial gain error and nonlinearity in the MDAC. The closed-loop gain amounts to 1.71. Fig. 17(a) and (b) respectively plot the open-loop nonlinearity error of the op amp and the closed-loop nonlinearity error of the MDAC in the amplification mode. The latter reaches 5 LSB. Shown in Fig. 18 is the simulated output spectrum of the MDAC if it senses a full-scale near-Nyquist sinusoid. The third harmonic is about 57 dB below the fundamental—calling for calibration—but higher harmonics are negligible.

Once designed for maximum output swings, maximum voltage gain, and proper compensation, the topology of Fig. 16 can simply be scaled so as to achieve (a) the fastest settling with given sampling, feedback, and load capacitors, and/or (b) an acceptably low integrated noise. In this work, the latter condition dominates, requiring a total bias current of 160 mA ($I_{SS} = 20$ mA, $I_{D7} = I_{D8} = 70$ mA) for the op amp in the first stage. (Under this condition, the MDAC settles to 13-bit accuracy in less than 1 ns.) The second stage components are scaled down by a factor of 4. The scaling continues by a factor of 2 to the fifth stage, with the remainder of the stages using identical op amps, each drawing 3 mA. This scaling of op amps and capacitors results in a total input-referred noise of 130 μV for the overall ADC,[8] yielding an SNR of 70 dB. That is, the

[8]Even with a 4-pF sampling capacitor, the ADC input-referred noise is relatively high due to contributions from op amps and subsequent stages (Appendix B).

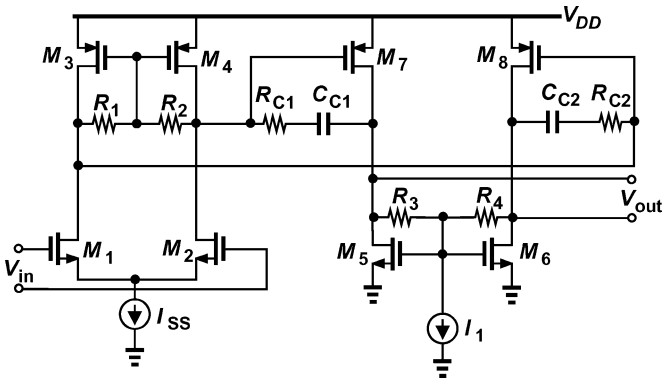

Fig. 16. Op amp circuit.

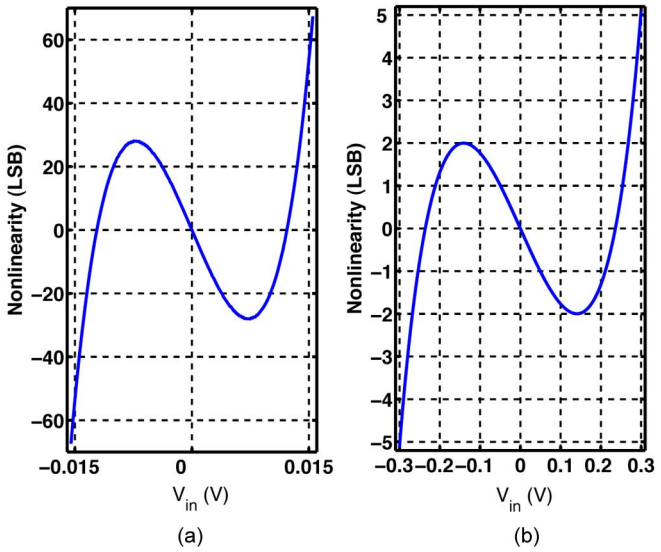

Fig. 17. (a) Open-loop nonlinearity of op amp. (b) Closed-loop nonlinearity of MDAC.

kT/C and op total amp noise of the pipeline is comparable with the quantization noise.

E. Comparator

The comparators in the first stage must sample the input signal in unison with the MDAC and respond rapidly so as to leave sufficient time for its settling. Fig. 19(a) redraws one of the comparators shown in Fig. 15 in the regular operation mode. Here, $C_1 = 128C_{u2}$, and the choice of $\alpha = +1$ or -1 sets the decision threshold to $+V_{\rm REF}/4$ or $-V_{\rm REF}/4$, respectively, if the attenuation due to $C_{\rm in}$ is negligible. Fig. 19(b) depicts the comparator implementation. A differential pair precedes the topology used in [19] so as to reduce the kickback noise.

F. Digital Back End

The ADC requires a digital back-end consisting of: 1) a combiner block realizing the inverse function in Fig. 3; 2) a 122-tap filter to implement nonlinear interpolation in the background mode; 3) a state machine carrying out the foreground and background calibrations; 4) 10 kbits of memory to store the 122 coefficients (C_k) for the interpolation filter and digital

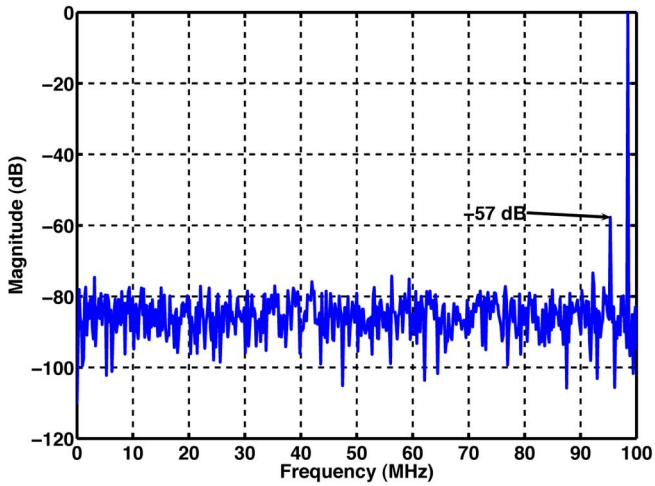

Fig. 18. Simulated MDAC output spectrum.

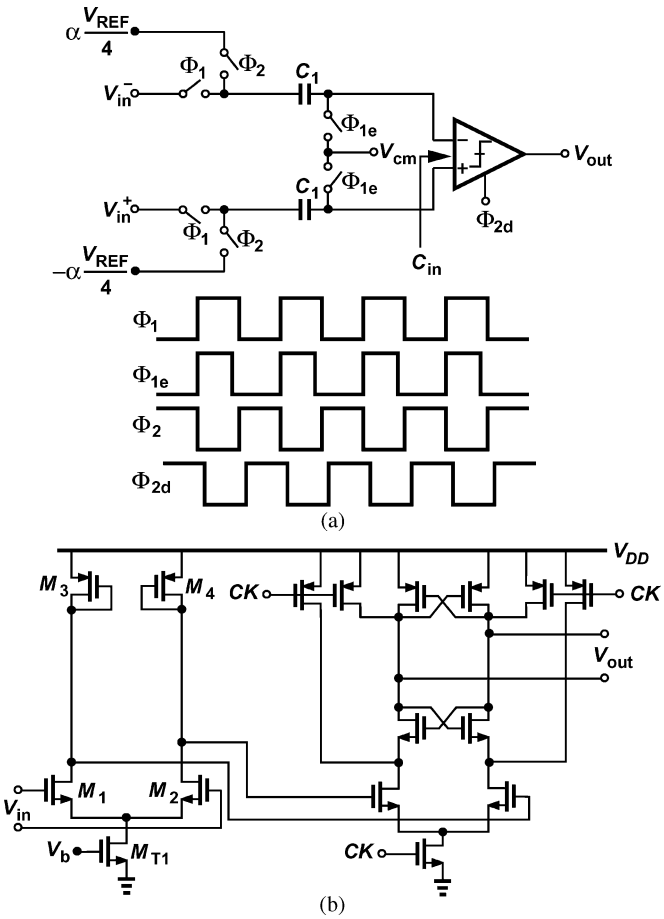

Fig. 19. (a) Comparator input network, and (b) comparator circuit.

bits for ΔV, V_{OS}, and 128 values of $V_{{\rm in},j}$ and $V_{{\rm in},j} + \Delta V$; and 5) the LMS machine that computes the coefficients. The prototype reported here contains the state machine but emulates the rest of the digital blocks in MATLAB using a 16-bit finite-precision implementation. Nonetheless, the complexity and power consumption of a hardware realization of the various blocks are estimated from synthesis and simulations. Gate-level synthesis of the logic for the combiner block, the nonlinear interpolation filter, and the calibration engine indicates a complexity of 17 K,

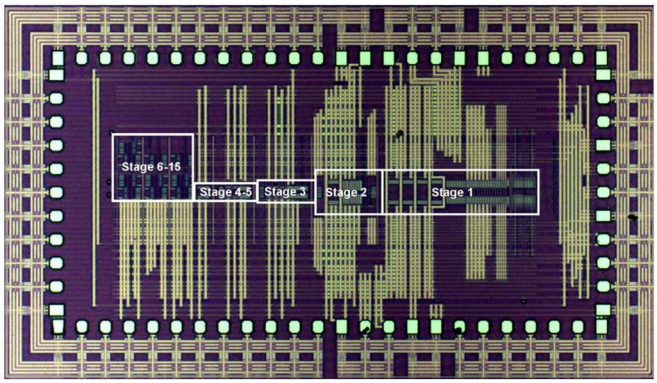

Fig. 20. Chip micrograph.

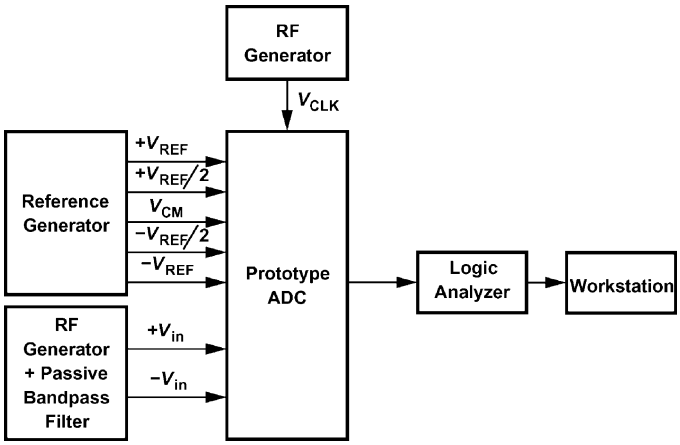

Fig. 21. Block diagram of the test setup.

2.3 K, and 53 K gates, respectively. In this study, the calibration engine is synthesized with a relaxed timing constraint but a strict area constraint whereas the remaining blocks are synthesized with a strict timing constraint. The power consumption of the synthesized logic at full speed is estimated to be 10 mW. The combiner block and interpolation filter consume 7.3 mW and 1.15 mW, respectively, at 200 MHz. Since a sample is skipped once every 16384 cycles, the calibration engine was synthesized with a relaxed timing constraint of 6.25 MHz, thus consuming 1.8 mW.

The prototype also includes a downsampling circuit to lower the output data rate by a factor of 16, thereby simplifying the design of the test environment.

V. Experimental Results

The prototype ADC has been fabricated in standard 90-nm CMOS technology. The die is shown in Fig. 20 and the active area measures 800 μm $\times$ 1700 μm. Operating from a 1.2-V supply, the ADC has been tested in a chip-on-board assembly. Fig. 21 shows the block diagram of the test setup. The analog input is derived from an RF generator, bandpass filtered, and converted to differential form. The clock is also obtained from an RF generator. The reference voltages are generated off-chip using precision resistors and low-noise op amps.

Figs. 22 and 23 plot the measured differential nonlinearity (DNL) and integral nonlinearity (INL) before and after calibration, respectively, at a sampling rate of 200 MHz. The uncalibrated ADC exhibits many missing codes and a peak INL of -70 LSB. After calibration, the peak DNL and INL fall to $+0.78$ LSB and -1.7 LSB, respectively.

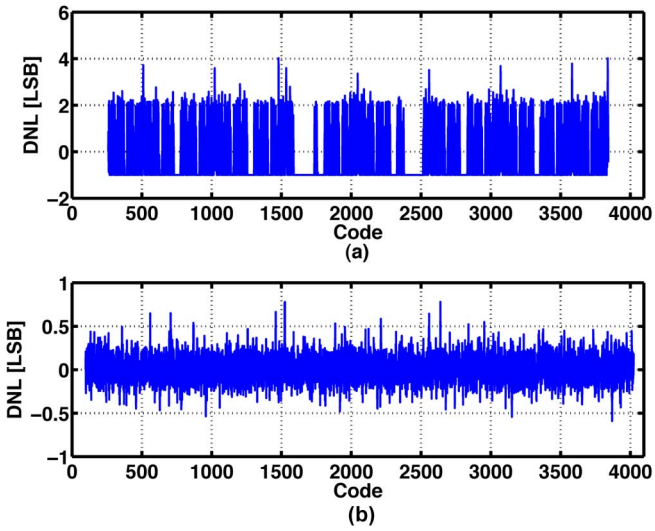

Fig. 22. Differential nonlinearity of pipelined ADC:(a) without calibration and (b) with calibration.

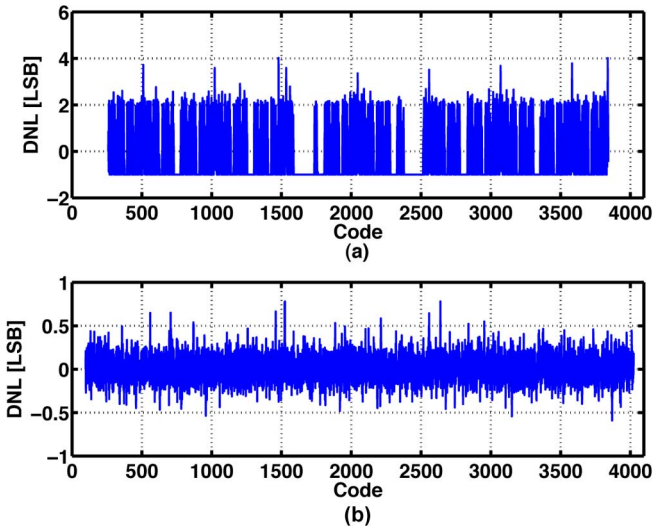

Fig. 23. Integral nonlinearity of pipelined ADC:(a) without calibration and (b) with calibration.

Fig. 24 shows the measured output spectrum for a 91 MHz, 1.2-$V_{\rm pp}$ analog input sampled at 200 MHz. Due to downsampling, the signal appears at 3.5 MHz. The SNDR is equal to 61.6 dB in this case, for an input frequency of 91 MHz.

Fig. 25 plots the measured SNDR as a function of the analog input frequency at a sampling rate of 200 MHz before and after foreground calibration. The average SNDR degrades by about 0.1 dB with background calibration and nonlinear interpolation to recover the sample skipped every 16,384 cycles.

Fig. 26 shows the convergence of the linear and the nonlinear coefficients of the different stages of the ADC. The algorithm converges in about 15,000 iterations.

Table III summarizes the measured performance of the ADC and compares it with that of recent work. The power consumed

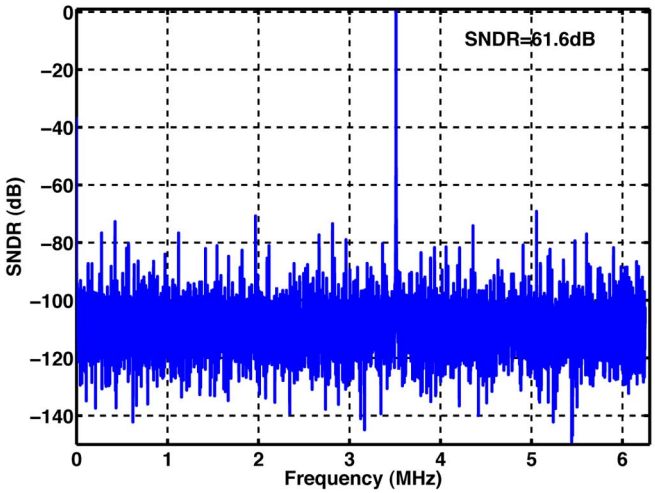

Fig. 24. Pipelined ADC output spectrum for $f_s = 200$ MHz (downsampled by a factor of 16), $V_{\rm in} = 1.2$ V and $f_{\rm in} = 91$ MHz.

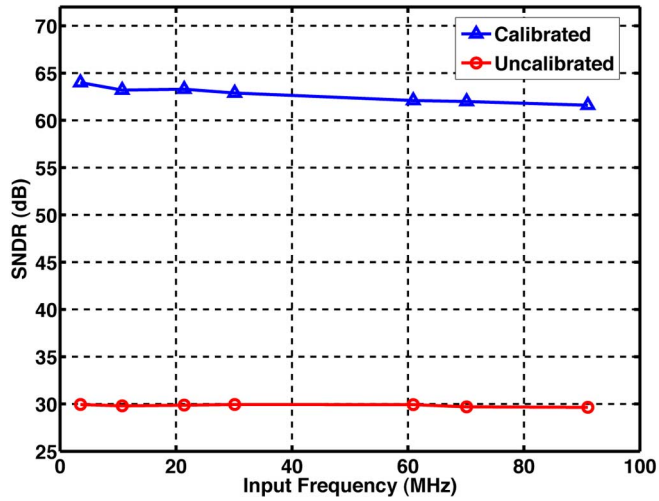

Fig. 25. Measured SNDR versus input frequency with and without calibration at $f_s = 200$ MHz.

by each op amp is shown in Table II in Appendix B. The comparators and flip-flops consume a total of 18 mW. The op amps can be placed in the two bias modes. In the low-bias mode (LBM), the power consumption drops to 186 mW and the high frequency SNDR degrades by about 2 dB, improving the figure of merit (FOM) by about 70%.

VI. Conclusion

With the scaling of supplies and transistor dimensions, high-gain high-speed op amps are approaching extinction, pointing to the need for calibration of gain error and nonlinearity in ADCs. A 12-bit pipelined ADC incorporating a new calibration algorithm is reported that corrects for capacitor mismatch, residue gain error, and op amp nonlinearity. A prototype realized in 90-nm CMOS technology achieves an SNDR of 62 dB while digitizing an input frequency of 91 MHz.

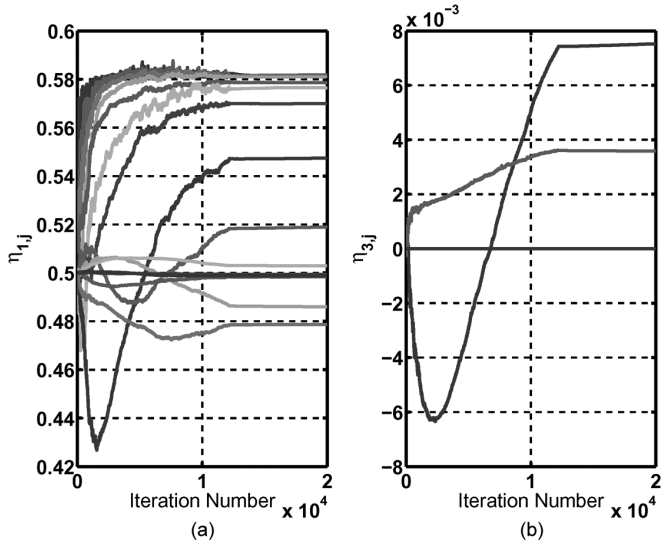

Fig. 26. Convergence plots of (a) linear ($\eta_{1,j}$, $j = 1$–15) and (b) nonlinear ($\eta_{3,1}$ and $\eta_{3,2}$) coefficients.

Appendix A

In this Appendix, the convergence of the proposed algorithm is proved for the case wherein the first stage contains gain error and nonlinearity but the subsequent stages are ideal. With our notation in (16)–(18), the error to be minimized is given by

$$\epsilon = D_{{\rm out},j} - D_{{\rm out},j,\Delta} - D_{{\rm out},\Delta} \tag{22}$$

From (22), ϵ can be written as

$$\epsilon = [D_{0\Delta} - (D_{01} - D_{02})] + \eta_1 [D_{B\Delta} - (D_{B1} - D_{B2})] + \eta_3 \left[D^3_{B\Delta} - \left(D^3_{B1} - D^3_{B2}\right)\right] \tag{23}$$

where the subscripts 0 and B refer to the first stage and the back-end, respectively. Thus, at discrete-time index n, the error is equal to

$$\epsilon(n) = c(n) + \boldsymbol{\eta}(\boldsymbol{n})\boldsymbol{x^T}(\boldsymbol{n}) \tag{24}$$

where

$$c(n) = D_{0\Delta}(n) - [D_{01}(n) - D_{02}(n)] \tag{25}$$
$$\boldsymbol{\eta}(\boldsymbol{n}) = [\eta_1(n)\eta_3(n)] \tag{26}$$
$$\boldsymbol{x}(\boldsymbol{n}) = [x_1(n)x_2(n)] \tag{27}$$
$$x_1(n) = D_{B\Delta}(n) - [D_{B1}(n) - D_{B2}(n)] \tag{28}$$
$$x_2(n) = D^3_{B\Delta}(n) - \left[D^3_{B1}(n) - D^3_{B2}(n)\right]. \tag{29}$$

The LMS update equation is therefore given by

$$\boldsymbol{\eta}(\boldsymbol{n}+\boldsymbol{1}) = \boldsymbol{\eta}(\boldsymbol{n}) + 2\mu\epsilon(n)\boldsymbol{x^T}(\boldsymbol{n}). \tag{30}$$

Let $\boldsymbol{\eta_{\rm opt}}$ be the coefficient vector that yields the minimum error. At time index n, $\boldsymbol{\eta}(\boldsymbol{n}) - \boldsymbol{\eta_{\rm opt}}$ represents the instantaneous deviation of the weight vector from the ideal value. Denoting this

TABLE II
SUMMARY OF CAPACITOR, OP AMP, AND NOISE SCALING

Stage	Sampling Capacitor (pF)	Op amp Current (mA)	Noise on Sampling Capacitor N_C (μV)	Total Output Noise $N_{OUT-TOT}$(μV)	Gain (G)	Output Noise of each Stage N_{OUTPUT}(μV)	Input−Referred Noise N_{INPUT} (μV)
1	4	160	45.5	136	1.73	110.91	64.11
2	2	40	64.34	228	1.73	198.98	66.48
3	1	20	90.99	290	1.73	243.55	47.04
4	0.5	8	128.69	382	1.73	310.42	34.66
5	0.25	4	181.99	636	1.73	552.6	35.66
6	0.1	3	287.75	984	1.73	848.79	31.66
7	0.1	3	287.75	984	1.73	848.79	18.30
8	0.1	3	287.75	984	1.73	848.79	10.58
9	0.1	3	287.75	984	1.73	848.79	6.11
10	0.1	3	287.75	984	1.73	848.79	3.53
11	0.1	3	287.75	984	1.73	848.79	2.04
12	0.1	3	287.75	984	1.73	848.79	1.18
13	0.1	3	287.75	984	1.73	848.79	0.68
14	0.1	3	287.75	984	1.73	848.79	0.39
15	0.1	3	287.75	984	1.73	848.79	0.23
Total Input−Referred Noise							129.6

quantity by $\xi(n)$ and subtracting $\eta_{\rm opt}$ from both sides of (30) we have

$$\boldsymbol{\xi(n+1)} = \boldsymbol{\xi(n)} + 2\mu\epsilon(n)\boldsymbol{x_T(n)}. \tag{31}$$

Also, (24) can be written as follows:

$$\epsilon(n) = c(n) + \boldsymbol{\eta(n)x^T(n)} - \boldsymbol{\eta^0 x^T(n)} + \boldsymbol{\eta^0 x^T(n)} \tag{32}$$

$$\epsilon(n) = \epsilon_{\rm opt}(n) + \boldsymbol{\xi(n)x^T(n)} \tag{33}$$

where $\epsilon_{\rm opt}(n)$ is the error when the coefficient is optimum. Taking the mean square of the error given by (33) gives, after some manipulation,

$$\begin{aligned} J_\epsilon &= E\left\{\epsilon^2(n)\right\} \\ &= E\left\{\left[\epsilon_{\rm opt}(n) - \boldsymbol{\xi(n)x^T(n)}\right] \right. \\ &\qquad \left. \times \left[\epsilon_{\rm opt}(n) - \boldsymbol{x(n)\xi^T(n)}\right]\right\} \qquad (34) \\ &= E\left\{\epsilon_{\rm opt}^2(n)\right\} + E\left\{\boldsymbol{\xi(n)x^T(n)x(n)\xi^T(n)}\right\} \\ &\quad - 2E\left\{\epsilon_{\rm opt}(n)\boldsymbol{\xi(n)x^T(n)}\right\}. \qquad (35) \end{aligned}$$

For independent random variables, we have

$$E\{xy\} = E\{x\}E\{y\} = E\left\{xE\{y\}\right\} \tag{36}$$

$$\begin{aligned} E\{x^2y^2\} &= E\{x^2\}\{y^2\} = E\left\{x^2E\{y^2\}\right\} \\ &= E\left\{xE\{y^2\}x\right\}. \end{aligned} \tag{37}$$

The second term in (35) thus reduces to

$$\begin{aligned} E\left\{\left[\boldsymbol{\xi(n)x^T(n)}\right]^{\boldsymbol{2}}\right\} &= E\left\{\boldsymbol{\xi^T(n)R_x\xi(n)}\right\} \\ &= tr\left\{E\left\{\boldsymbol{\xi^T(n)R_x\xi(n)}\right\}\right\} \\ &= tr\left\{\boldsymbol{K(n)R_x}\right\} \end{aligned} \tag{38}$$

where $\boldsymbol{R_x}$ is the autocorrelation of $\boldsymbol{x(n)}$, $tr\{\ \}$ the trace of a matrix (the sum of diagonal elements), and $\boldsymbol{K(n)}$ the weight error correlation matrix. Also, the third term in (35) is zero due to the independence assumption and the fact that $\epsilon_{\rm opt}(n)$ is a constant. Thus, (35) reduces to

$$J_\epsilon = J_{\min} + tr\left\{\boldsymbol{K(n)R_x}\right\} \tag{39}$$

where $J_{\min} = E[\epsilon_{\rm opt}(n)^2]$ is the minimum mean square error. From Fig. 8(b), (39) is a paraboloid, thereby converging if driven by an LMS update algorithm [20].

In the absence of nonlinearity, this equation represents a parabola and converges if $1/\lambda_{\max} > \mu > 0$, where $\lambda_{\max}$ is the maximum of the eigenvalues of the autocorrelation matrix $\boldsymbol{R_x}$. The above derivation can be extended to incorporate N non-ideal stages. Since the inputs are uniformly distributed and independent, the autocorrelation matrix becomes a diagonal matrix. The autocorrelation matrix obtained from simulations is then used to obtain appropriate step size, μ.

APPENDIX B

This Appendix summarizes the capacitor, op amp, and noise scaling in the prototype pipelined ADC. The noise analysis is done for each stage of the pipeline by running periodic steady state analysis followed by periodic noise analysis in Cadence Spectre.

The total output noise, $N_{\rm OUT-TOT}$, and the gain are obtained from Cadence. The output noise of each stage is given by

$$N_{\rm OUTPUT_I} = \sqrt{N_{\rm OUT-TOT_I}^2 - N_{C_I}^2 G_I^2} \tag{40}$$

TABLE III
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ART

		This Work	[16]	[23]	[24][12]
Resolution		12 bits	14 bits	11 bits	14 bits
Conversion Rate		200 MHz	100 MHz	200 MHz	100 MHz
Supply Voltage		1.2 V	1.5 V	1 V	3 V
Input Voltage		1.2 V_{PP}	1.5 V_{PP}	1 V_{PP}	
Input Capacitance		6 pF (Single Ended)			
Power	HBM[10]	348 mW	224 mW	180 mW	230 mW
	LBM[11]	186 mW			
SNDR	HBM	64 dB (f_{in}=3.5 MHz)	71.4dB (f_{in}=15 MHz)	62.2dB (f_{in}=4 MHz)	70.2dB (f_{in}=39 MHz)
		61.6 dB (f_{in}=91 MHz)			
	LBM	61.5 dB (f_{in}=3.5 MHz)	66.5dB (f_{in}=39 MHz)	59.9dB (f_{in}=60 MHz)	70.5dB (f_{in}=145 MHz)
		59.4 dB (f_{in}=91 MHz)			
INL	HBM	$+1.3/-1.7$ LSB	$+2/-2$ LSB	0.87 LSB	$+2/-2.11$ LSB
	LBM	$+1.55/-1.9$ LSB			
DNL	HBM	$+0.78/-0.59$ LSB	$+1.1/-1.1$ LSB	0.53 LSB	$+0.6/-0.8$ LSB
	LBM	$+0.91/-0.76$ LSB			
FOM	HBM	1.34 pJ/conv (f_{in}=3.5 MHz)	1.12 pJ/conv	1.86 pJ/conv	0.7 pJ/conv
		1.77 pJ/conv (f_{in}=91 MHz)			
	LBM	0.96 pJ/conv (f_{in}=3.5 MHz)			
		1.22 pJ/conv (f_{in}=91 MHz)			
Technology		90 nm CMOS 1P8M	0.13μm CMOS	65 nm CMOS	0.18μm DGO CMOS
Active ADC Area		800 μm $\times$ 1700 μm	1.02 mm^2	1.1 mm^2	7.28 mm^2

[10]High Bias Mode.

[11]Low Bias Mode.

[12]This work assumes sufficient uncalibrated capacitor matching for 14-bit resolution [25].

where subscript "I" denotes the stage number. The input-referred noise of each stage is thus equal to

$$N_{\mathrm{INPUT_I}} = \frac{N_{\mathrm{OUTPUT_I}}}{\prod_{j=1}^{I} G_j}. \tag{41}$$

This quantity includes the noise sampled on to the sampling capacitor of stage $(I+1)$ [21]. The total input-referred noise is given by

$$N_{\mathrm{IN-TOTAL}} = \sqrt{\sum_{j=1}^{15} N_{\mathrm{INPUT_I}}^2 + N_{C_1}^2}. \tag{42}$$

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