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In-situ mask removal in selective area epitaxy using metal organic chemical vapor deposition

S. Birudavolu, S.Q. Luong, N. Nuntawong, Y.C. Xin, C.P. Hains, D.L. Huffaker*

Center for High Technology Materials, University of New Mexico, 1313 Goddard SE, Albuquerque, NM 87106, USA

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Abstract

We demonstrate an in situ mask removal technique for use in selective area epitaxy (SAE) by metal organic chemical vapor deposition (MOCVD). The mask material is native aluminum oxide (Al_xO_y) formed by wet thermal oxidation of a thin AlGaAs layer. The Al_xO_y layer is patterned using standard photolithography and wet chemistry outside of chamber. The Al_xO_y layer forms a high-quality, pin-hole- free SAE mask that can be removed within the MOCVD chamber using an in situ HCl etch process. After in situ mask removal, subsequent growth processes produce an atomically smooth and uniform surface. Scanning electron microscopy and atomic force microscopy are used to characterize surface features and measure RMS roughness after each processing step. Using this processing scheme, we form a buried InGaAs quantum well stripe that emits room-temperature photoluminescence. The in situ mask removal may have significant applications in nanopatterned growth processes, where protection of the growth surface from atmospheric exposure reduces surface contamination to improve electrical and radiative interface characteristics.

Keywords: A3. Metalorganic chemical vapor deposition; A3. Selective epitaxy; B1. Halides; A1. Etching; A3. Quantum wells; B1. Oxides

1. Introduction

There have been many demonstrations of selective area epitaxy (SAE) for purposes ranging from buried heterostructure lasers [1,2] to patterned nanostructures [3,4]. Common dielectric mask materials for SAE are SiO_2 [5] or SiN_x [6] that require an ex situ hydrofluoric acid etch for mask removal. Such processing schemes typically involve several sample transfer steps to accommodate oxide layer deposition and patterning outside the chamber, an SAE in the chamber, followed by mask removal outside the chamber and finally, an overgrowth process.

*Corresponding author. Tel.: +1 505 272 7845; fax. +1 505 272 7801.
E-mail address: huffaker@chtm.unm.edu (D.L. Huffaker).

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Each exposure of the growth surface to atmosphere can result in contamination that leads to surface degradation, traps and nonradiative recombination centers.

To minimize both the atmospheric exposure of the growth surface and the number of sample transfers, we have developed an SAE process based on a mask material that can be removed using an in situ etch step. The mask material is Al_xO_y formed by wet thermal oxidation of AlGaAs as described by Dallasassee et al. [7] in 1990. This Al_xO_y material has been highly characterized for its interface properties [8,9], crystallinity [10], and thermal stability [11,12]. While the oxidation process and mask patterning are performed in the clean room, the growth surface can be completely protected since the mask is removed in the metalorganic chemical vapor deposition (MOCVD) chamber during the process flow. Use of the Al_xO_y layers as a high-quality mask for selective lateral overgrowth of GaN in MOCVD has already been demonstrated by Dapkus and co-workers [13]. Using different growth parameters, the same group has also demonstrated growth of GaN on Al_xO_y [14].

While no mention of in situ Al_xO_y processes have been mentioned in the literature, previous work has identified Ga_2O_3 [15,16] as a possible mask for SAE with in situ removal using thermal processing and hydrogen treatment. In Ref. [15], the Ga_2O_3 is deposited using a sputtering method that results in a significant pin-hole density in the Ga_2O_3 material. However, initial results in GaAs and AlGaAs SAE using the Ga_2O_3 mask along with in situ mask removal are demonstrated. In the present manuscript, we describe the growth and processing sequence used to form and remove an Al_xO_y mask. We demonstrate a very high-quality Al_xO_y mask, atomically smooth GaAs/InGaAs SAE, in situ mask removal and GaAs overgrowth. The sample surface is characterized after each processing step using atomic force microscopy (AFM), scanning electron microscopy (SEM) and optical microscopy. Using this processing scheme, we demonstrate room-temperature photoluminescence (RTPL) from buried InGaAs stripe quantum wells (QWs).

2. Process flow—description and analysis

The samples are grown on a GaAs (1 0 0) substrate. After deoxidation, a GaAs buffer is grown followed by a 300 Å thick $Al_{0.95}Ga_{0.05}As$ layer and a thin GaAs cap. The sample is processed according to the outline in Fig. 1(a)–(f). Processes (a)–(c) are performed in the cleanroom and (d)–(f) in the growth chamber. We refer to two regions on the sample surface, Region A and Region B, to delineate location. In the cleanroom, the GaAs cap layer is removed using $NH_4OH:H_2O_2:H_2O$ (1:1:400) to expose the AlGaAs surface (Fig. 1(a)) for oxidation. The AlGaAs is converted to Al_xO_y in a standard oxidation furnace at 425 °C (Fig. 1(b)) as described in Ref. [7]. The newly formed oxide layer is patterned using a standard photolithographic technique to form 10 μm photoresist (PR) stripes on a 20 μm pitch followed by a wet-chemical etch of undiluted HCl to remove the exposed oxide. An optimized wet-etch process only partially removes the oxide layer in Region A, thus protecting the growth surface from atmospheric exposure (Fig. 1(c)). The PR is removed and the sample is loaded into the MOCVD system for steps (d)–(f).

Prior to SAE, the Al_xO_y-patterned GaAs sample is treated at 900 °C for 5 min under a hydrogen flow to remove carbon, residual oxygen and other contamination from the sample surface prior to regrowth. The SAE material quality is sensitive to V/III ratio and growth rate. We find that a slow

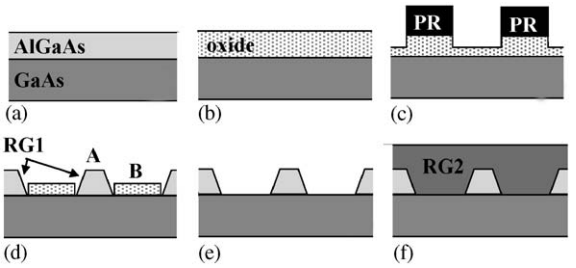

Fig. 1. Schematic diagram of the process flow showing (a) AlGaAs/GaAs heterostructure, (b) Al_xO_y mask/GaAs, (c) Photoresist/Al_xO_y mask/GaAs, (d) SAE on Al_xO_y mask/GaAs, (e) Al_xO_y mask etched using HCL (f) overgrowth. Processes (a)–(c) are conducted in the cleanroom and (d)–(f) are in the MOCVD chamber.

growth rate along with a low V/III ratio is necessary to prevent GaAs islanding on the Al_xO_y layer. For our system configuration, the optimized growth parameters are AsH_3 flow rate = 15 sccm/s, TMG flow rate = 2.1 sccm/s, V/III = 7.5, growth rate = 4 Å/s, which is similar to selective area growth of GaAs on SiO_2 masks [17]. The SAE process results in a 600 nm GaAs layer grown in Region A (Fig. 1(d)).

3. Surface characterization and processing feedback

Figs. 2(a)–(c) show images of the sample surface in Regions A and B after SAE. Fig. 2(a) shows a Nomarski microscope image and an SEM inset of the masked sample. The SEM inset of Fig. 2(a) images the edge of the GaAs stripe/oxide mask interface and confirms a highly selective growth in the open mask regions with no evidence of GaAs islanding or growth on the Al_xO_y surface. Fig. 2(b) is an AFM image of Region A that shows step flow regrowth of GaAs with an RMS roughness of 0.0246 nm. Fig. 2(c) is an AFM image of Region B that shows a terraced, but fairly smooth oxide surface with an RMS roughness of 3.157 nm.The oxide surface chosen for this figure is marked by islands (Ga or GaAs) with size and density of 20–50 nm and $3 \times 10^9\,cm^{-2}$, respectively.

After the SAE step, the oxide mask is removed in situ using HCl in a H_2 carrier gas. In preparation for mask removal, the reactor temperature is reduced and stabilized at 300 °C under AsH_3 overpressure. The arsine valve is closed and the valved HCl line is opened. An HCl flow rate of 250 sccm/s provides an etch rate = 1.6 Å/s at this temperature. The mask removal by HCl gas can be explained by the following equation:

$$Al_xO_y + 6Hcl(g) = 2AlCl_x(g) + y(H_2O)(g). \quad (1)$$

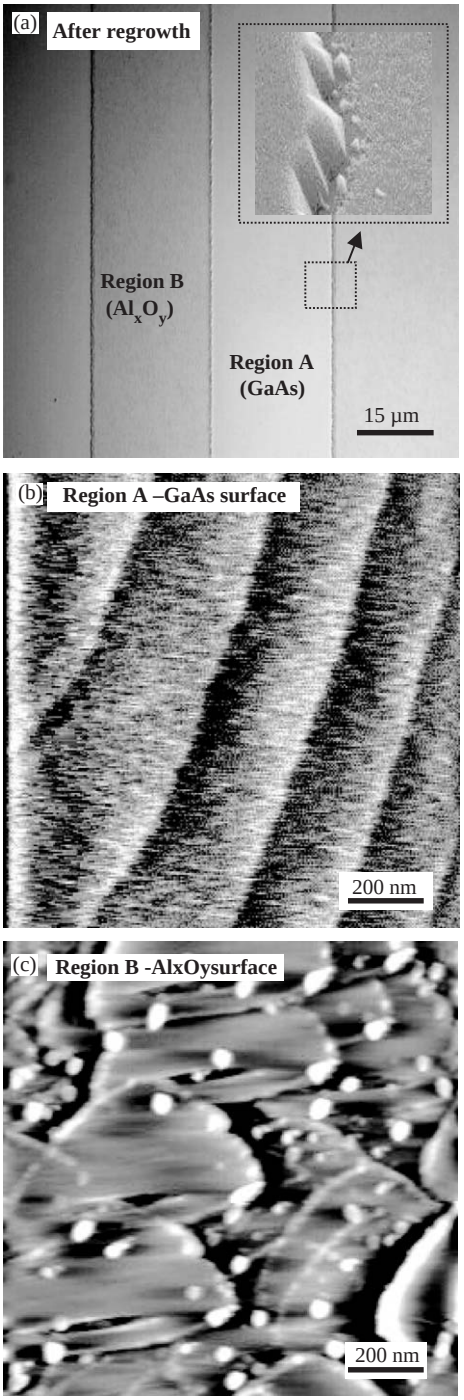

Fig. 2. (a) Nomarski microscope image and a scanning electron microscope (SEM) inset of a masked sample after GaAs SAE (600 nm), (b) AFM image of Region A shows step flow growth of GaAs that results in an RMS roughness of 0.0246 nm, (c) AFM image of Region B shows a terraced but fairly smooth surface with scattered islands that result in an RMS roughness of 3.157 nm.

The negative free energy change, $\Delta G = -118.8$ kJ, of this reaction suggests etching of the Al_xO_y by the HCl gas. Fig. 3(a) shows an SEM image of both Regions A and B after in situ mask removal. Figs. 3(b) and (c) show higher-resolution AFM images of both regions. While the GaAs layer of Region A, Fig. 3(b), is slightly roughened by the etch compared to Fig. 2(b), it is still atomically flat with an RMS roughness of 0.0968 nm. Region B, Fig. 3(c), previously covered with oxide, is a pock-marked GaAs surface with an RMS roughness of 1.4908 nm. At this point, the source of the surface roughening is unclear. It may result from the oxide/GaAs interface at the time of oxidation and it may be due to a slight etch of the GaAs during the oxide removal process. However, the following paragraph describes a higher-temperature mask removal process that results in a smoother surface and shorter etch time.

The in situ etch process has been characterized as a function of temperature. We find that both the etch rate and the surface of Region B are significantly improved if the in situ etch is performed at higher temperatures. This trend is due to the increased molecular decomposition of HCl at $T > 550\,^{\circ}$C. The entire oxide layer (300 Å) is completely removed in 10 s at 550 °C compared to the 500 s required at 300 °C. Fig. 4(a)–(c) shows AFM images of the etched surface at three flow times, 2, 5 and 10 s. The etch process is incomplete after 2 and 5 s as shown in Fig. 4(a) and (b), which indicates the anisotropic nature of the in situ HCl etch process. Fig. 4(c) shows a relatively smooth surface that results when the oxide is completely removed. We note that the surface of Fig. 4(c) has an RMS roughness (0.2903 nm) that is decreased compared to Fig. 3(c) etched at 300 °C. The explanation for the smoother surface may be reduced oxide/GaAs selectivity at higher temperatures that results in a partially etched GaAs surface immediately after the oxide is removed. We are conducting experiments, presently, to determine the etch rate of the GaAs at 550 °C.

After the in situ etch step, the reactor temperature is increased to 600 °C in preparation for the overgrowth process (Fig. 1(f)). The GaAs overgrowth (100 nm) uses gas flows similar to the SAE step. Fig. 5(a)–(c) shows several images of the

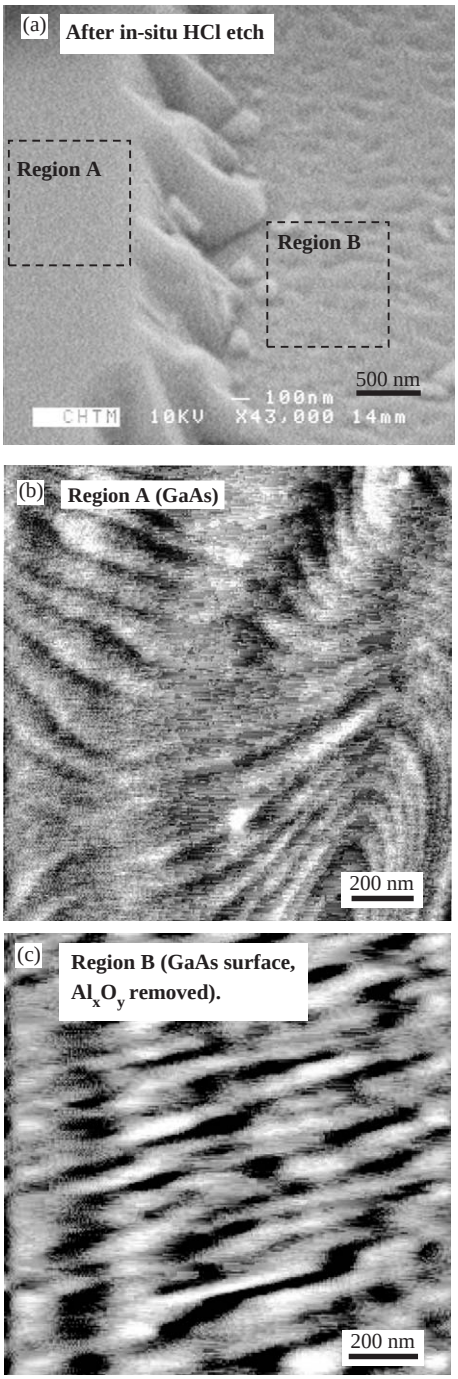

Fig. 3. (a) SEM image of the sample after both GaAs SAE and in-situ mask removal, (b) AFM image of Region A shows step flow growth of GaAs, (c) AFM image of Region B shows GaAs surface with an RMS roughness of 1.4908 nm.

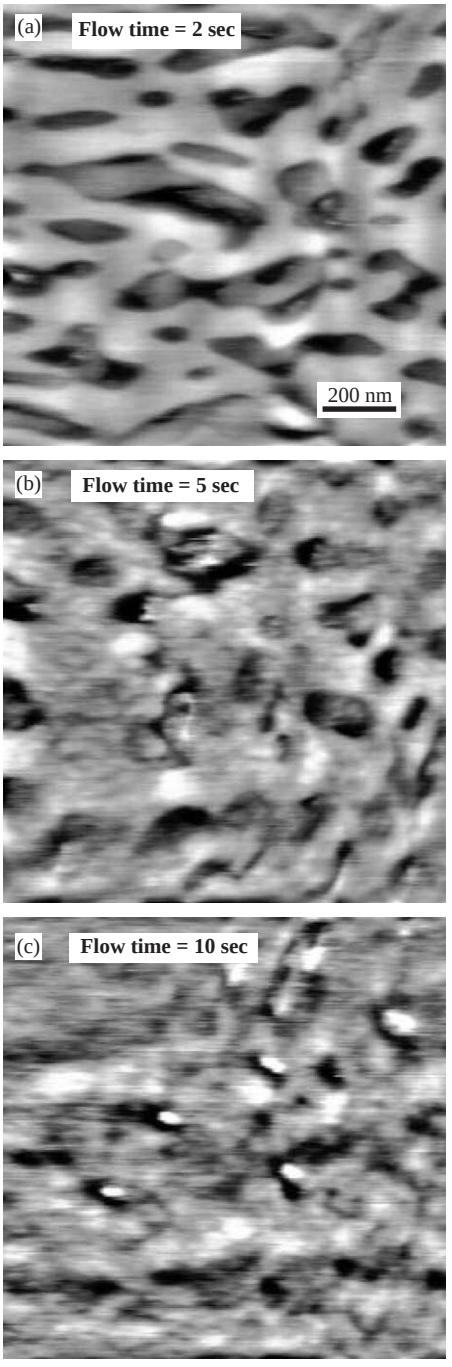

Fig. 4. Region B after in situ HCl etch at 550 °C for (a) 2 s flow time, (b) 5 s flow time and (c) 10 s flow time.

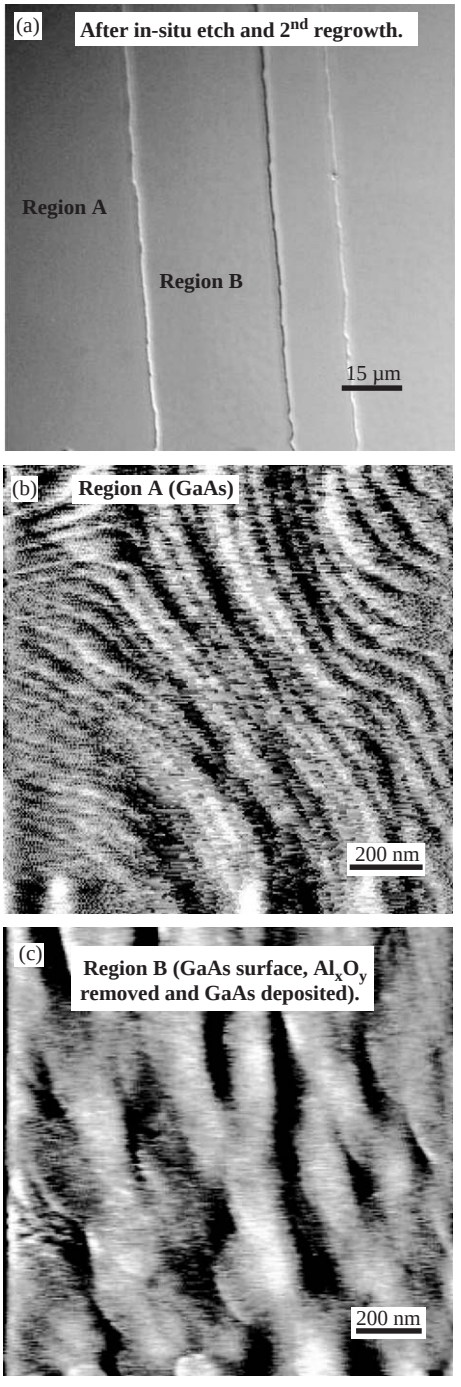

Fig. 5. (a) The Nomarski images of both Regions A and B after GaAs overgrowth (100 nm), (b) AFM of Region A (GaAs stripe) with RMS roughness of 0.0714 nm, (c) AFM image of the GaAs surface in Region B, once masked with Al_xO_y, with RMS roughness of 0.249 nm.

surface after overgrowth. We note that this particular sample was processed with the 300 °C in situ etch process. The Nomarski image in Fig. 5(a) shows very clean surfaces in both Regions A and B. Fig. 5(b) shows an AFM image of the GaAs stripe in Region A and indicates an RMS roughness of 0.0714 nm. Fig. 5(c) shows an AFM image of the GaAs surface in Region B—the area that was once masked with Al_xO_y—with an RMS roughness of 0.249 nm that indicates a markedly smoother surface compared to Fig. 3(c). With continued regrowth of another 300 nm GaAs, the RMS roughness continues to improve to a value of 0.1425 nm.

4. Quantum well SAE

An important application of this in situ mask removal is in the growth of buried nanopatterned heterostructures as described in Ref. [17]. Toward this application, we have successfully demonstrated growth of a buried single $In_{0.20}Ga_{0.80}As$ (120 Å) QW within Region A. The QW is grown under the conditions described above and emits RTPL at 1.075 μm as shown in Fig. 6(a) and (b). Fig. 6(a) shows RTPL from the InGaAs QW grown by SAE using the Al_xO_y mask and capped by a 20 nm GaAs layer. Fig. 6(b) shows RTPL from the same sample, but after the oxide mask removal process. The data suggests that the etch (at 300 °C) process does not significantly affect the optical properties of the capped active region. It also indicates that the etch process at 300 °C is quite selective in that 30 nm of oxide is removed from Region B without significantly affecting the 20 nm GaAs cap layer in Region A.

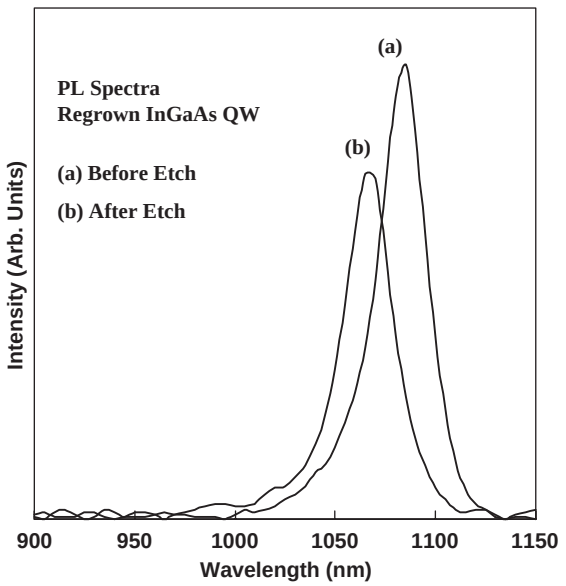

Fig. 6. (a) RTPL from the InGaAs QW grown by SAE on Region A and capped by a 20 nm GaAs layer, (b) RTPL from the same sample after the oxide mask removal process.

5. Conclusion

We have demonstrated a process by which a dielectric mask for selective growth can be removed in situ. The mask material, Al_xO_y, is formed by wet-thermal oxidation of AlGaAs in a cleanroom environment. The Al_xO_y layer serves as a very effective mask for SAE, but is also removable within the MOCVD chamber, thus protecting the growth surface from environment exposure. To date, we have demonstrated RTPL from a buried InGaAs QW stripe. The next stage of this project is to utilize the in situ mask removal process in the patterning of nanostructures in which the in situ etch will prevent the growth surface from atmospheric exposure.

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