

UCLA Electrical Engineering ARR 2011

Session 5. Next-Generation CAD for Circuit Design West Coast Room

11:00-11:25

"Defect-Aware Floorplanning for EUV Masks"

Abde Ali and Puneet Gupta

Abstract:

Extreme ultraviolet (EUV) lithography is the most promising technology solution replace to 193nm lithography. Apart from source and resist issues, fabricating defect-free mask blanks remains a major "show-stopper" for the adoption of EUV lithography. One promising approach to alleviate this problem is smart reticle floorplanning to minimizing the design impact of buried defects. We propose a simulated annealing based gridded floorplanner for single project reticles that minimizes the design impact of these buried defects. Our simulation results show a substantial improvement in mask yield: for a mask with 40 defects, our approach can improve mask yield from 53% to 94%.

11:25-11:50

"Stochastic Simulation for Analog Circuit and Stochastic Yield for Memory"

Fang Gong and Lei He

Abstract:

Two research threads related to stochastic modeling and simulation are presented. Considering device mismatch, thermal noise and flick noise, we develop a transient noise analysis over 100X faster than the existing work and apply it to high precision analog circuits. Considering rare event failure rate for memory, we introduce several methods including cross-entropy minimization within the framework of importance sampling and apply them for memory yield optimization.

11:50-12:15

"DRE: A Framework for Efficient and Systematic Co-Evaluation of Design Rules, Technology Choices, and Layout Methodologies"

Rani S. Ghaida and Puneet Gupta

Abstract:

Design rules have been the primary contract between technology developers and designers. While current approaches for defining design rules are largely empirical, this talk offers a framework for fast and systematic evaluation of design rules in terms of area, yield, and variability. The framework essentially creates a virtual cell library and performs the evaluation based on the virtual layouts. Due to the focus on exploration of rules at an early stage of technology development, we use first order models of variability/yield and topology/congestion-based area estimates. The framework can be used to co-evaluate and co-optimize rules, patterning technologies, and layout methodologies.