

UCLA Electrical Engineering ARR 2011

Session 6. Novel Circuits for Cognitive Radios South Bay Room

11:00-11:25

"A Single-LC-Tank 5-10GHz Quadrature Local Oscillator for Cognitive Radio Applications"

Jianhua Lu, Ning-Yi Wang and Mau-Chung Frank Chang

Abstract:

This talk presents a local oscillator (LO) that converts oscillation frequencies of 13.3-20GHz from a single-LC-tank VCO to the intended 5-10GHz with continuous frequency coverage. A 4-stage differential injection-locked ring oscillator (ILRO) is used after the latch-based divider to produce quadrature output phases without requiring 50% duty cycle of input signals as those of conventional divide-by-2 approaches. When implemented in 65nm CMOS, the prototype LO consumes 22mA at 1V supply and is able to exhibit a worst-case phase noise of -102dBc/Hz at 1MHz offset across the entire 5-10GHz band.

11:25-11:50

"Low-Power Broadband Frequency Synthesis for Cognitive Radios"

Marco Zanusso and Behzad Razavi

Abstract:

Cognitive radios communicate on any standard across two or three frequency decades. A key challenge in the design of such radios is the synthesis of the carrier frequency for a broad range. A new frequency synthesizer architecture is proposed that leverages the low phase noise of LC oscillators and the wide tuning range of ring oscillators. The synthesizer generates a carrier frequency from 10 MHz to 10 GHz and its phase noise satisfies mobile communication standards. The power consumption is lower than 20 mW.

11:50-12:15

"A 7.4mW 120MS/s Wideband Spectrum Sensing Digital Baseband Processor for Cognitive Radios"

Tsung-Han Yu, Danijela Cabric and Dejan Markovic

Abstract:

A digital baseband cognitive radio spectrum sensing processor with channel-specific threshold and sensing time is integrated in 1.64mm² in 65nm CMOS. The processor achieves detection probability .9 and false-alarm probability .1 for 5dB within a 50ms sensing time. The power and area of are minimized by jointly considering algorithm, architecture, and circuit parameters. The chip dissipates 7.4mW for a 200MHz sensing bandwidth. A 22x reduction in power per sensing bandwidth is achieved compared to prior work.