Design-Aware Mask Inspection

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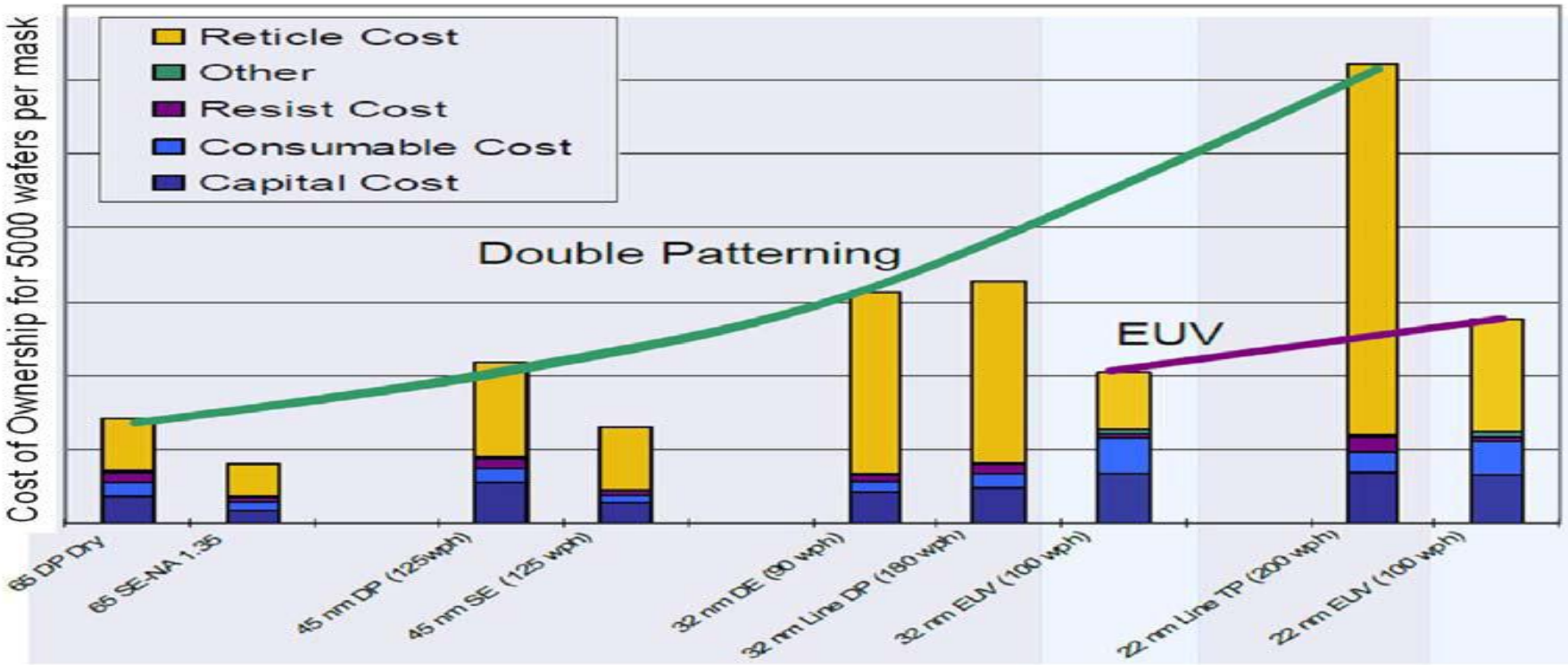
Annual Research Review, 2012

Semiconductor Manufacturing Cost Explosion



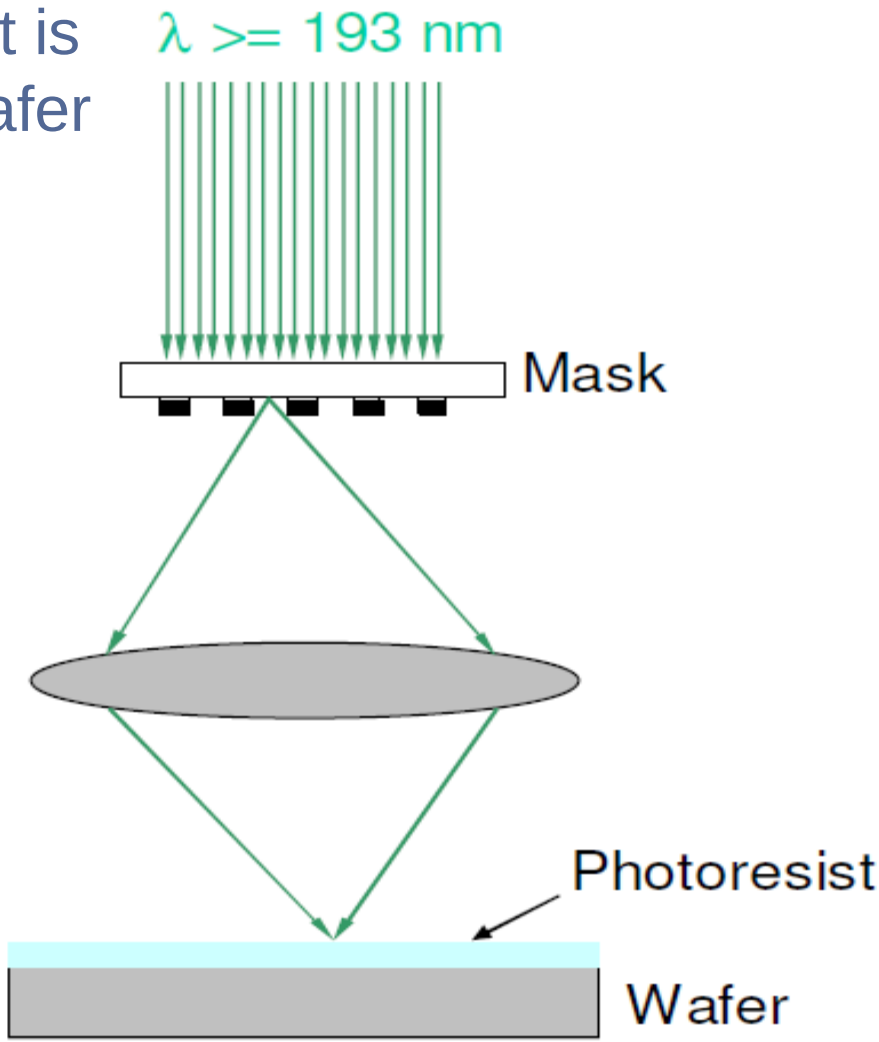
Source: ITRS 2009

- **Mask/reticle cost the most significant contributor to this problem**

Mask Manufacturing Challenges

- Masks contain circuit layout that is reproduced several times on wafer
  - Need defect free masks

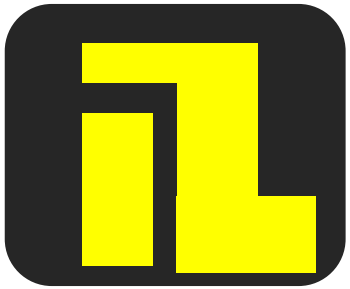
- 193nm light even for < 90nm features → diffraction
  - Optical proximity correction (OPC) to compensate diffraction



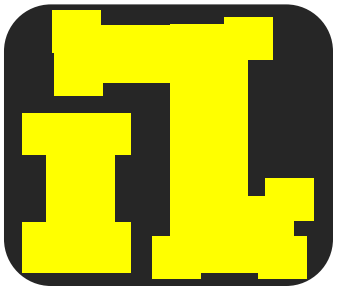
Source: Naulleau, SPIE tutorial, 2011

Mask Manufacturing

Circuit Layout



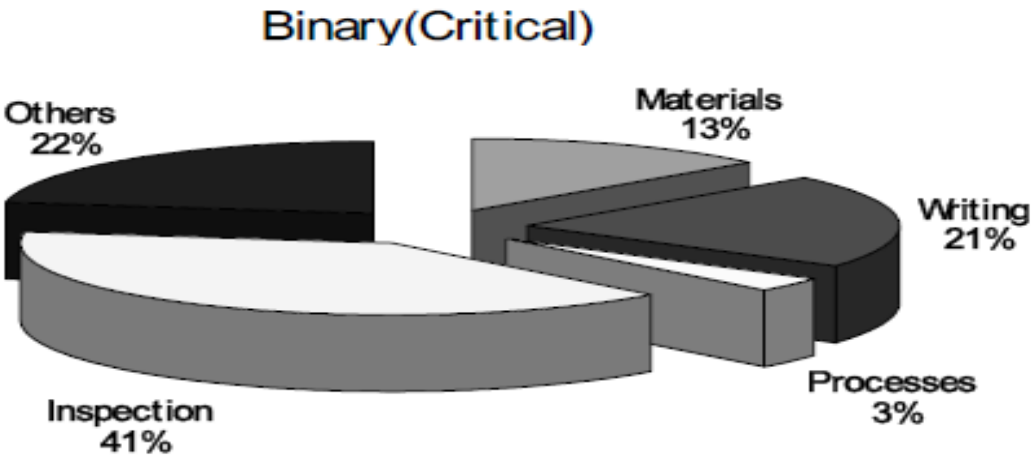
OPC



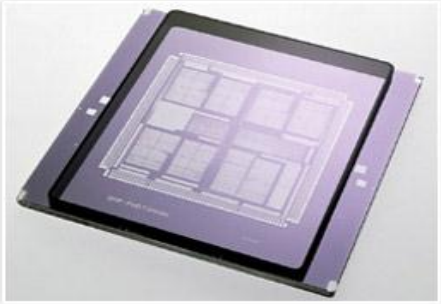
Mask Write (E-beam Tool)

Mask Inspection

Mask manufacturing cost dominated by inspection

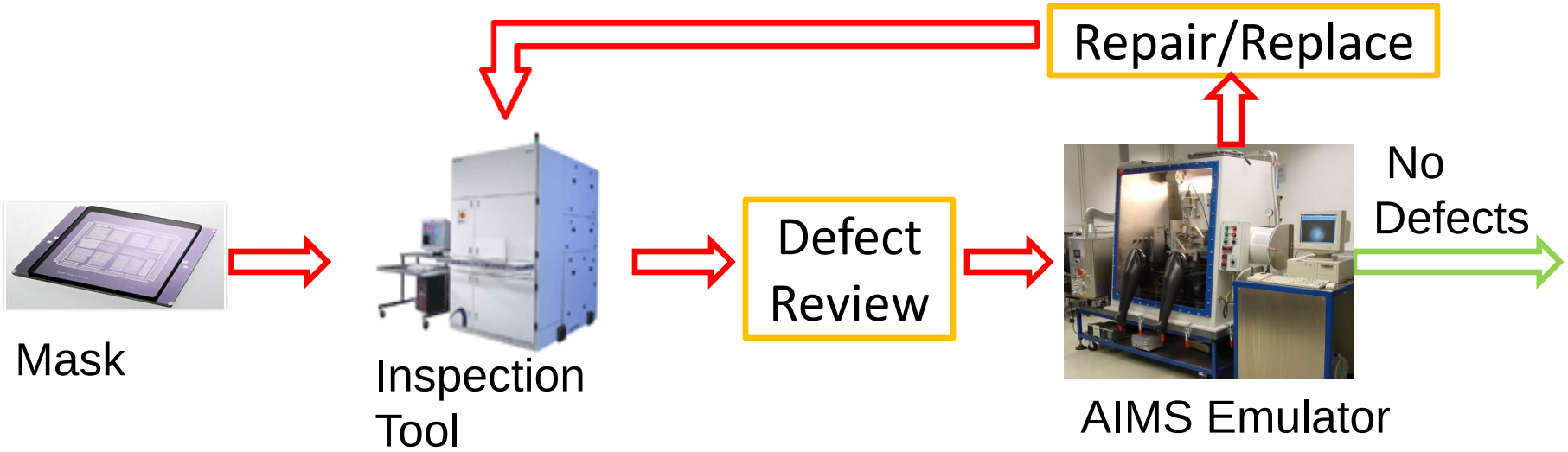


Source: Dai Nippon Photomask at SPIE 2008



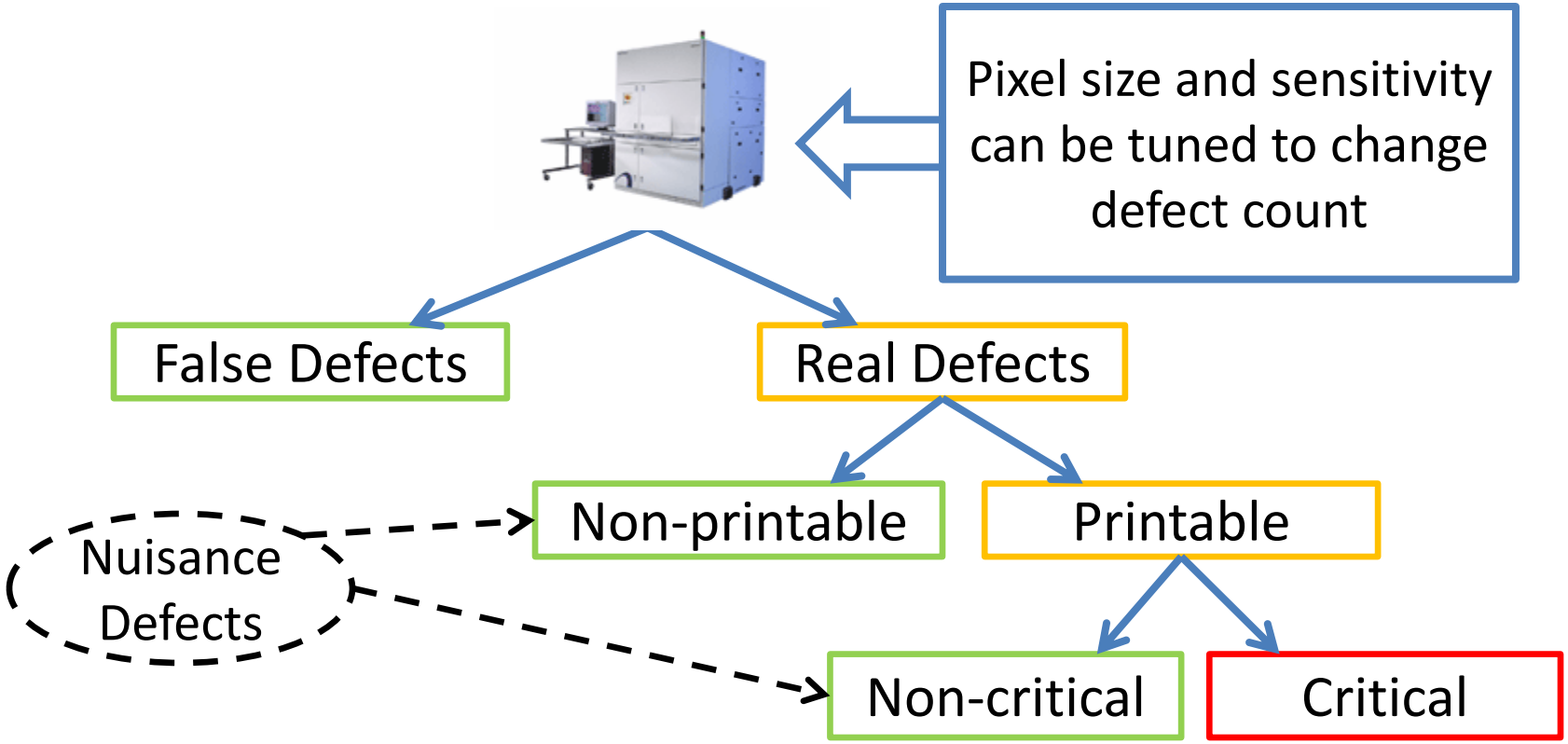
Mask

Conventional Mask Inspection



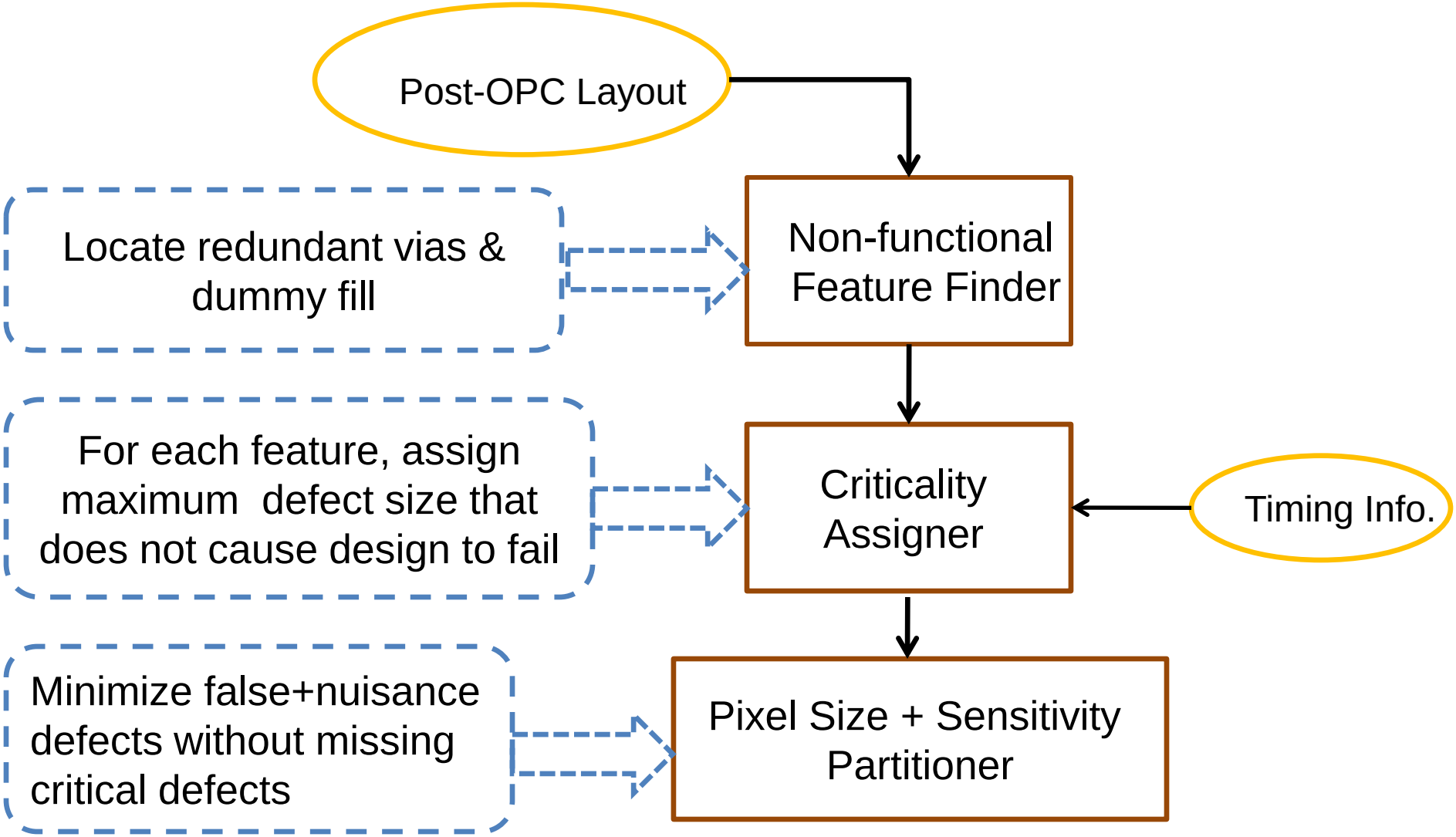
- Inspection tool → compare mask images, report difference as defect
- Defect Review → prune out noise and non-printable defects.
- AIMS → accurate test of defect printability. But slow and tedious

Why Design-Awareness ?



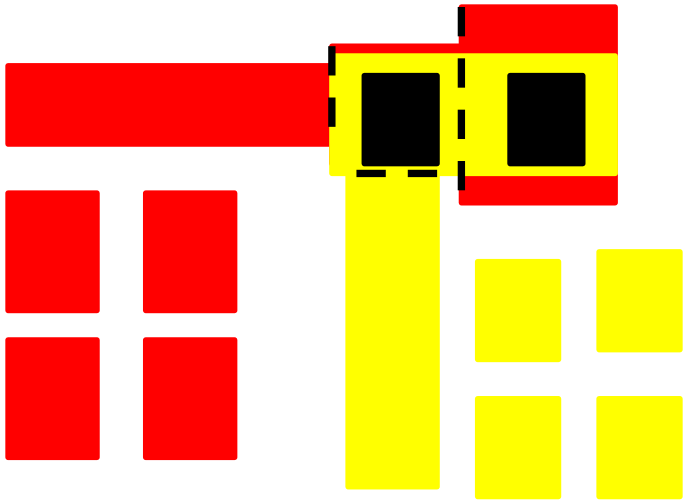
- Design information helps predict defect criticality
- Inspection resolution can be adjusted for less critical regions up front

Overview of Our Approach

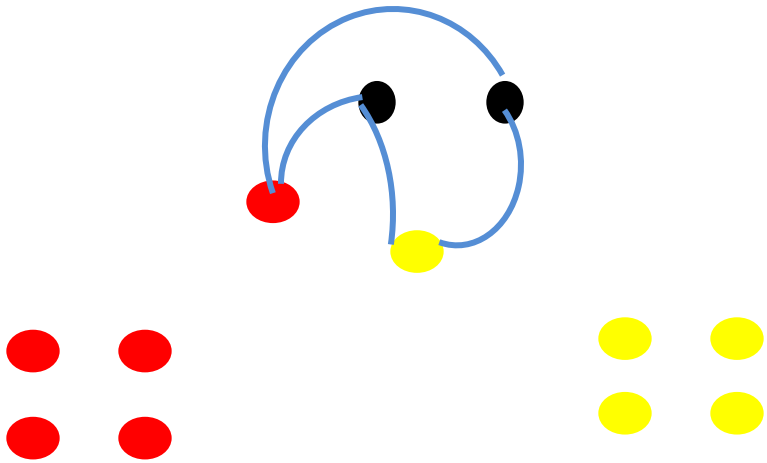


Non-Functional Feature Finder

Sample Layout



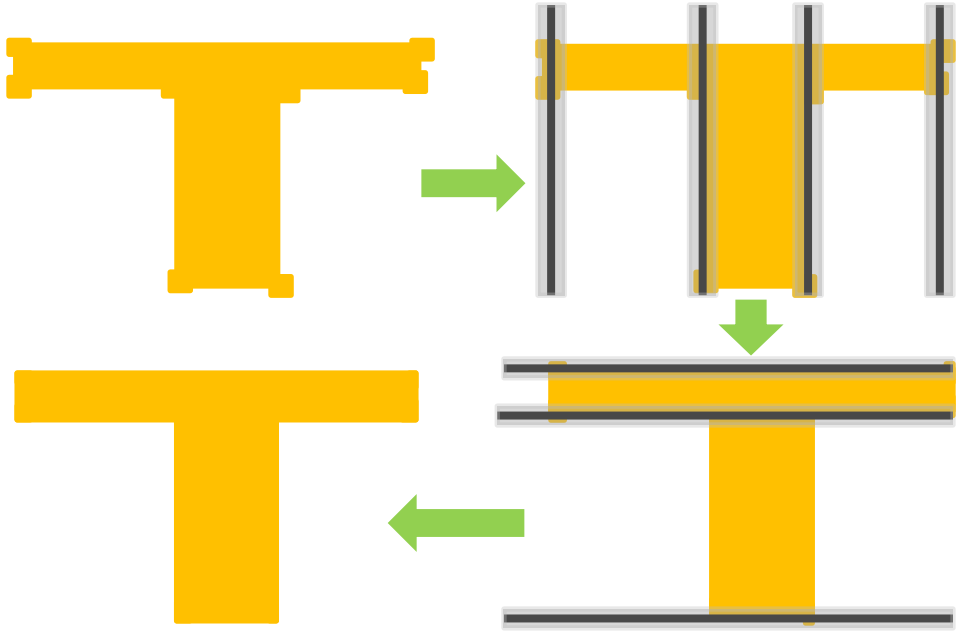
Reduced neighborhood graph

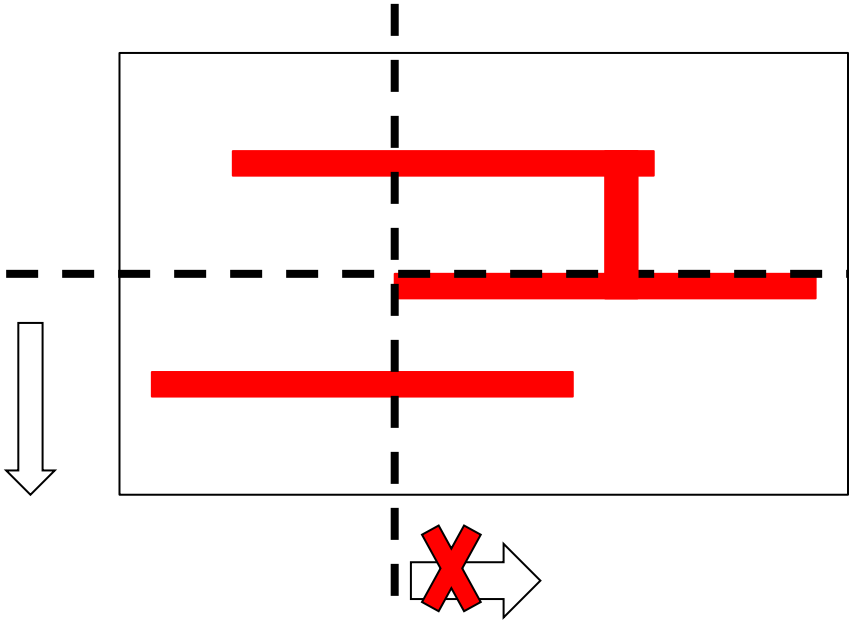


- Fracturing, scan-line based graph construction and edge contraction
- Cycles → Redundant vias; Isolated nodes → Dummy Fill
- Large design layouts and complex post-OPC shapes makes graph construction step very slow

Runtime Reduction Techniques

- Runtime O(R*logR* + *E*) for scan-line using dynamic trees
  - R → number of rectangles, E → Number of intersections
- Shape simplification to reduce R
- Smart scan-line direction to reduce average tree size



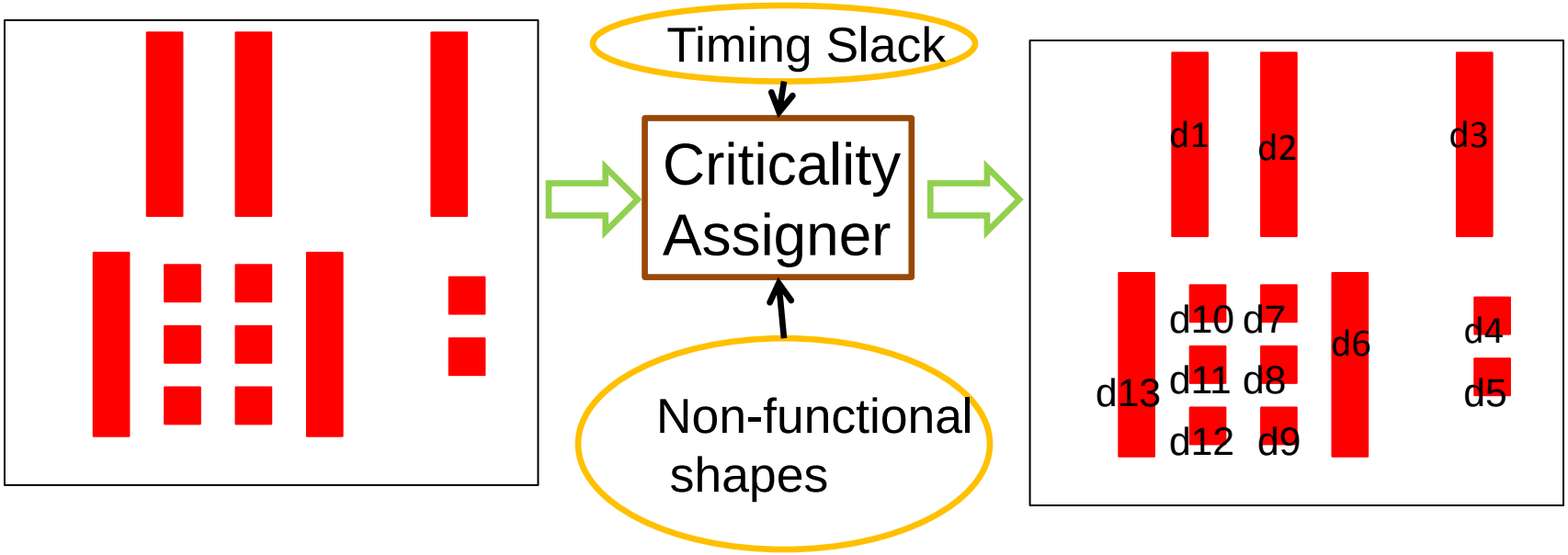


Experimental Results

- Implemented in C++ using OpenAccess API
- Results validated using a post routing output file
  - Double via detection fully accurate
  - 1% error in dummy fill detection

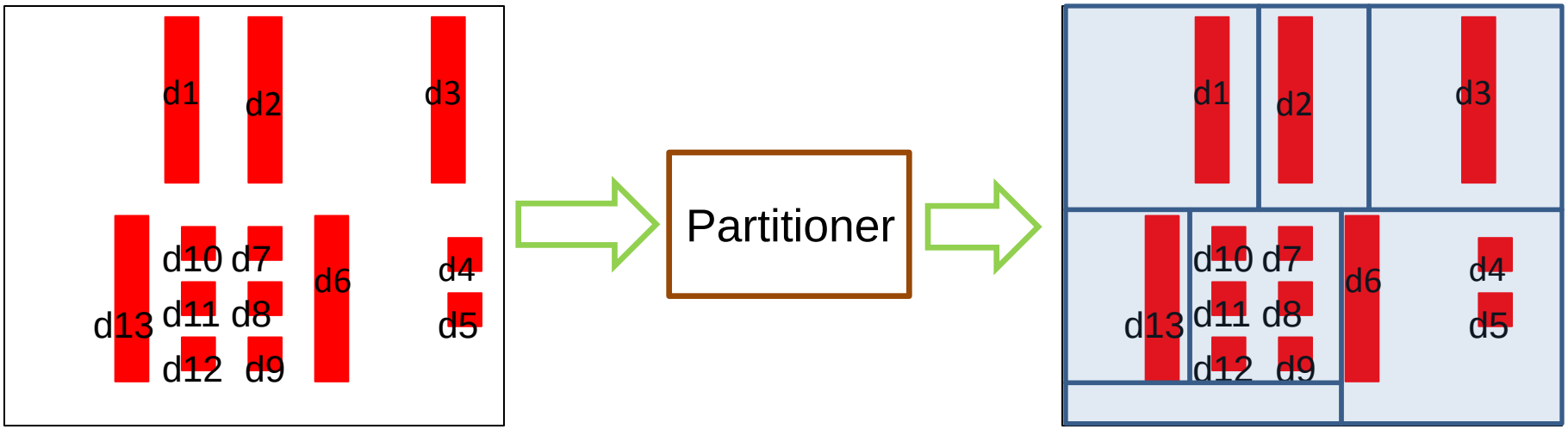
Design	#Gates	#Rectangles	# Double Vias	# Dummy Fill	Runtime (min.)
Mips	19983	2582260	23562	20040	3
AesCipher	11395	2893906	24267	5308	683
Nova	62800	20621302	156774	144727	135

Criticality Assignment



- Needs to be done for different layer reticles
  - Poly and active → timing slack and first order transistor models
  - Metal → dummy fill
  - Via → redundant vias

Partitioning Problem Formulation



- Minimize (#False Defects + γ*#Nuisance Defects) by finding partitions that are assigned different pixel size and sensitivity
- Constraints:
  - No critical defect missed → Each partition limited by smallest tolerance
  - Partition size not too small → Inspection tool limitation

Modeling Defect Count

- Adjustable inspection tool parameters: pix → pixel size & S → sensitivity

$$FalseDefects = K_a \times \frac{A}{pix^2} \times \mathrm{erfc}\left(K_m \frac{pix}{S}\right)$$

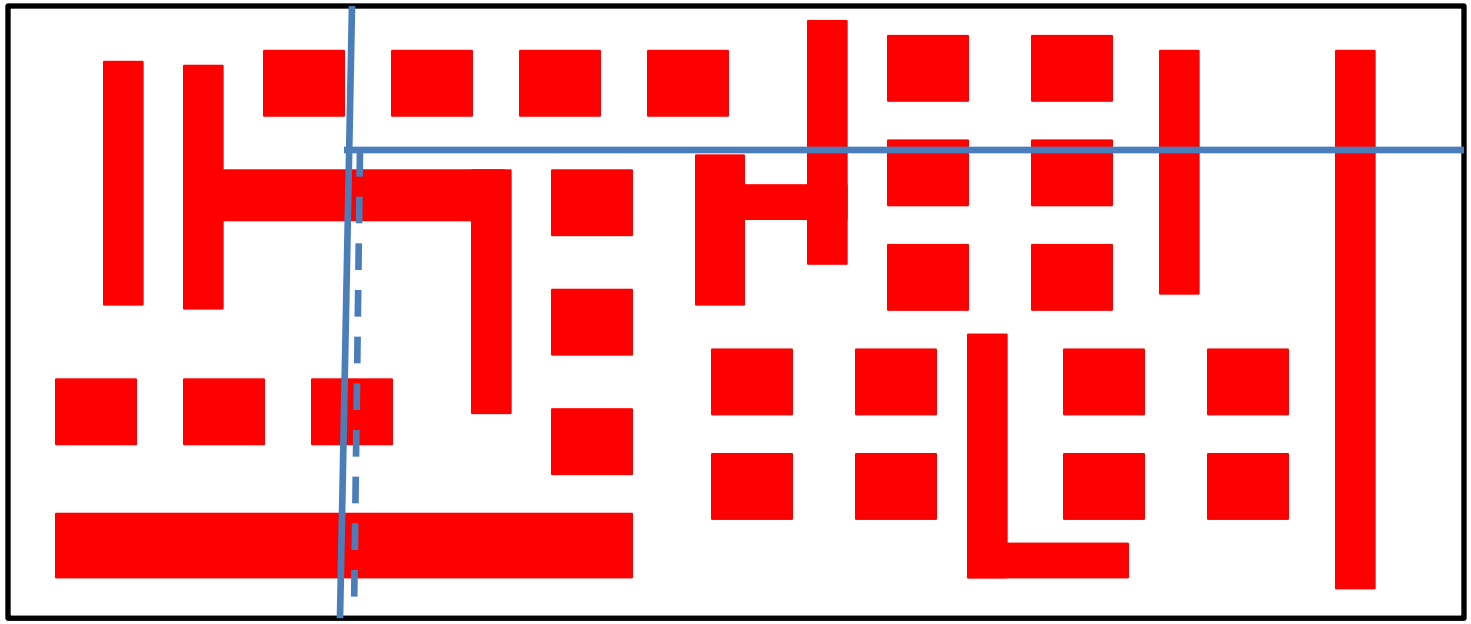
Number of pixels

Probability of pixel being labeled as defect (Gaussian noise)

$$NuisanceDefects = T \times A \times \left(\frac{pix}{S}\right)^{\beta}$$

Negative binomial defect distribution

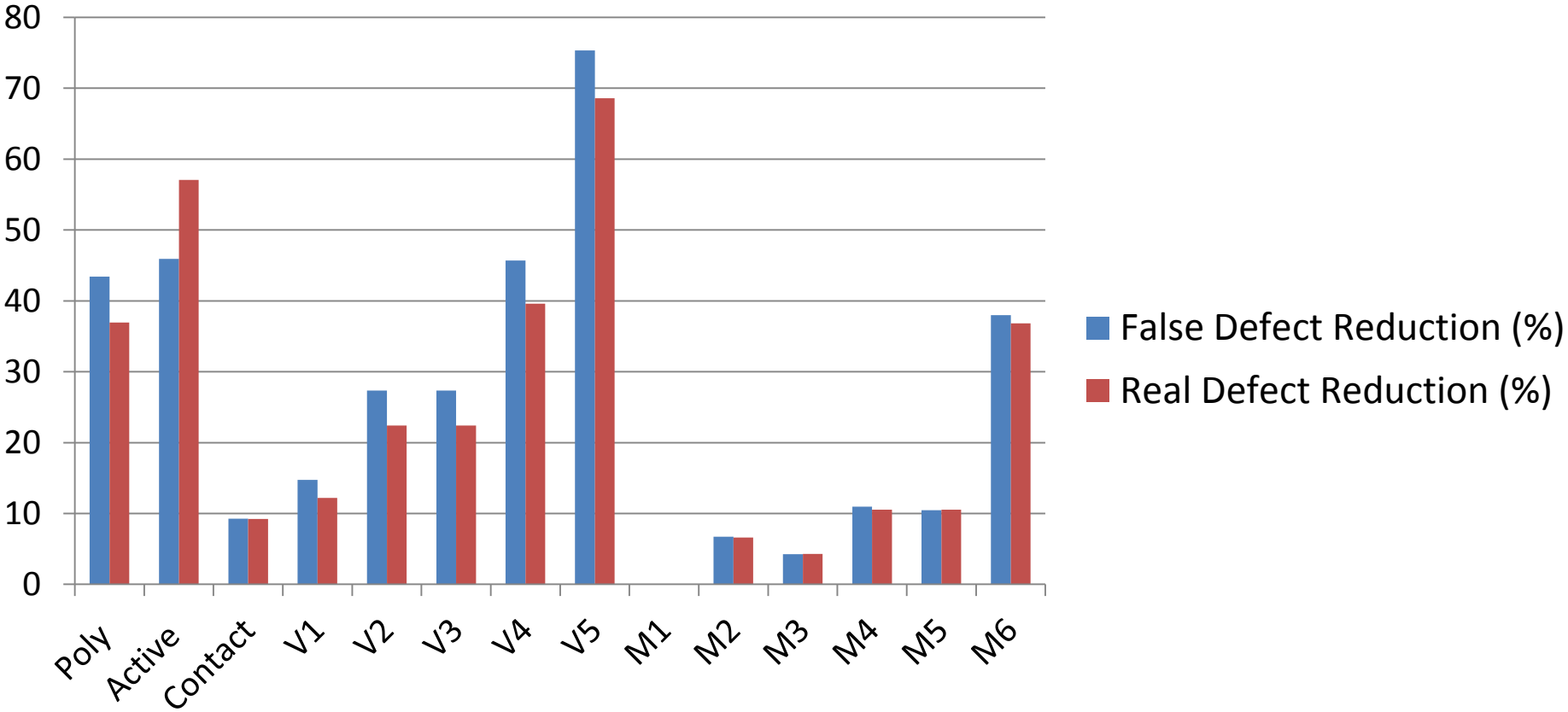
Partitioning Heuristic



- Recursive, greedy approach
  - Split existing partition
  - Pick best pixel size & sensitivity option for each split
  - Stop when partition minimum size or no cost improvement

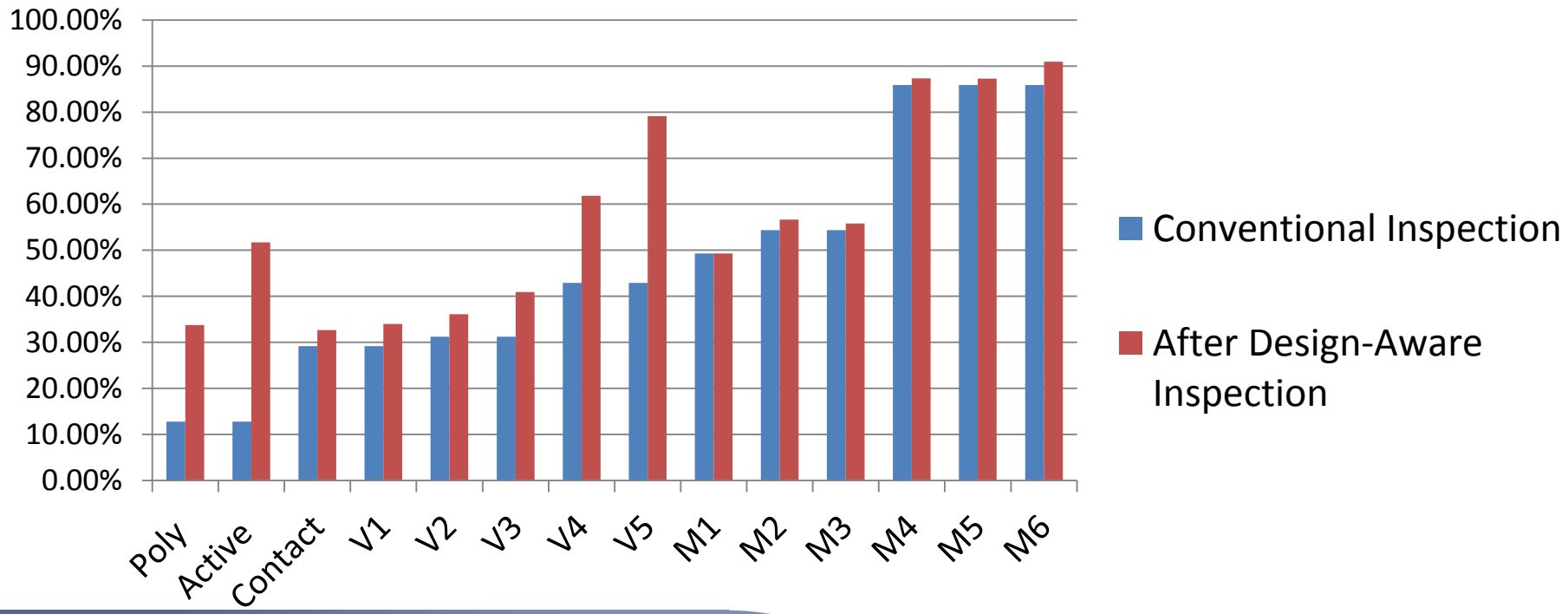
Experimental Results: Reduction in Defect Count

- Front-end layers (poly and active) and higher metal/via layers show most improvement



Improvement in First Pass Yield

- Fraction of masks that can be shipped out without repair
  - $P_i = e^{-(P_{dd} \times D_{avg} A_i)}$ yield per partition (Poisson distribution)
- Improvement in line with reduction in defect count → significant reduction for expensive poly/active masks



Conclusion

- Proposed and implemented a comprehensive design-aware mask inspection
  - Graph based algorithm that finds redundant vias and dummy fill with almost 100% accuracy
  - Systematic method to assign maximum tolerable defect size to each layout feature
  - Recursive partitioning method to inspect different layout regions at different pixel size/sensitivity which achieves 39% reduction in defect count
  - 19%-point improvement in first pass yield for critical polysilicon mask as a result of design-aware inspection