# Unparalleled Power Performance **FNFL**



## Challenges & Trends for 28 nm and below in SOC Analog/Mixed Signal Design

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#### **Abstract**

In this presentation, we review current and future trends and challenges for system on chip analog/mixed signal design for CMOS nodes in 28 nm and below. We review our recent developments in clocking, phased locked loop, higher performance I/O and SerDes designs. In addition, we will give real world examples of Analog Bit solutions, which have shipped in billions of units in a variety of today's highest performance consumer platforms.

Specifically, we discuss development of industry leading and industry firsts including: (1) development of a CMOS 20nm mixed signal design kit, (2) successful design of high-performance PLL at very low dissipated power levels for 100GB applications including implementation of a 14GHz SerDes PLL in TSMC 28nm technology which produces quadrature outputs and a measured output clock jitter < 0.3ps rms in under 12mW of power and (3) development of a PLL used in 100GBASE-LR4 and Optical Transport Lane 4.4 SerDes applications incorporating an LC-VCO running at 12.5-14.5GHz and generates quadrature outputs at 6.25-7.25 GHz. Fabricated in 40nm GP CMOS technology, the PLL operates on two supplies: 1.25V for the VCO and 1V for the rest of the circuitry with a measured output clock jitter at the transmitter output at 7 GHz output frequency of 174fs<sub>rms</sub> while consuming 12mW.

# **Biographies**



# Alan Rogers, President and CTO

Alan Rogers is the President and CTO of Analog Bits, Inc. He has grown Analog Bits into the premier supplier of custom transistor-level IP solutions for both fabless and IDM companies and continues to oversee technology development for customer applications. Mr. Rogers' technical background includes server-class microprocessors, volume consumer semiconductors and high reliability aerospace and defense applications, and he holds numerous patents. Mr. Rogers holds a BSc degree in engineering from Imperial College, London



### Mahesh Tirupattur, EVP

Mahesh Tirupattur is the Executive Vice President at Analog Bits responsible for business partnerships, IP licensing, and joint venture development. He has helped lead Analog Bits to its position as the leader in integrated timing and interface IP. Prior to Analog Bits, Mr. Tirupattur held executive level positions leading IP and library companies. He earned his MSEE from Arizona State and a business degree from the University of California, Berkeley.