Paper 9.6

A 60-GHz CMOS Receiver Using a 30-GHz LO

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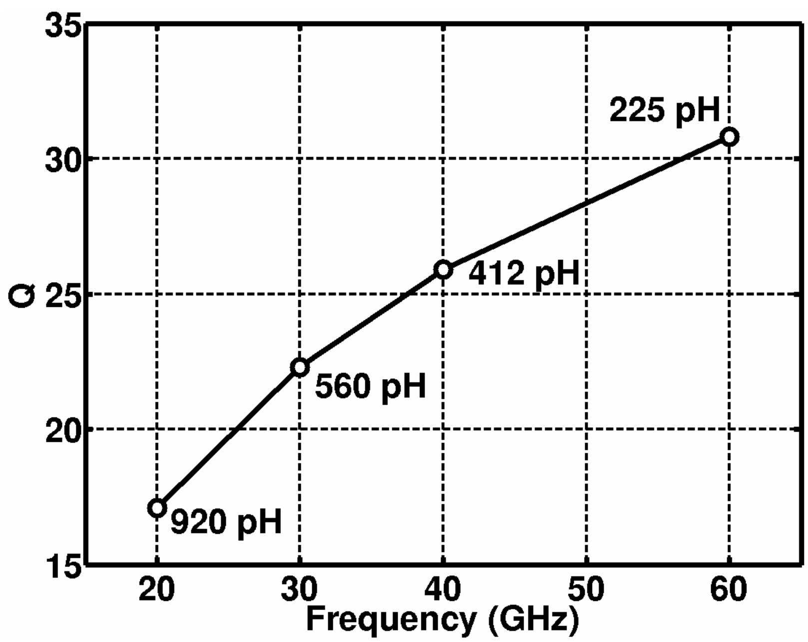
Outline

- Introduction
- Architecture Comparison
- Proposed Architecture
- Building Blocks
- Experimental Results
- Conclusion

Design Challenges: LO

- LO Generation
- LO Distribution
- LO Division

Inductor Q's at mm-Wave Frequencies

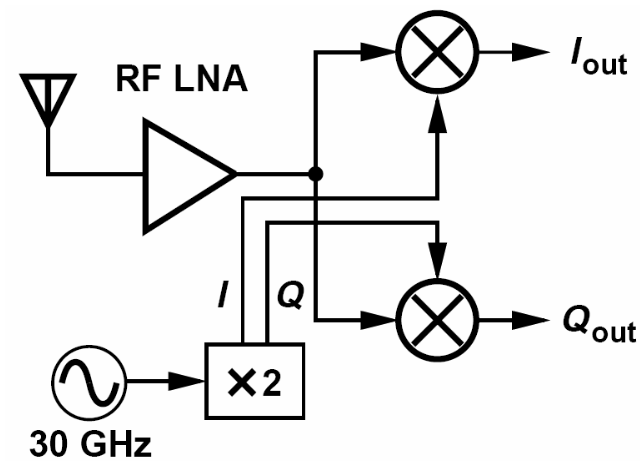


Phase Noise

$$\propto \frac{1}{4Q^2}\frac{\omega_0^2}{\Delta\omega^2}$$

- Also, varactor Q falls with frequency.

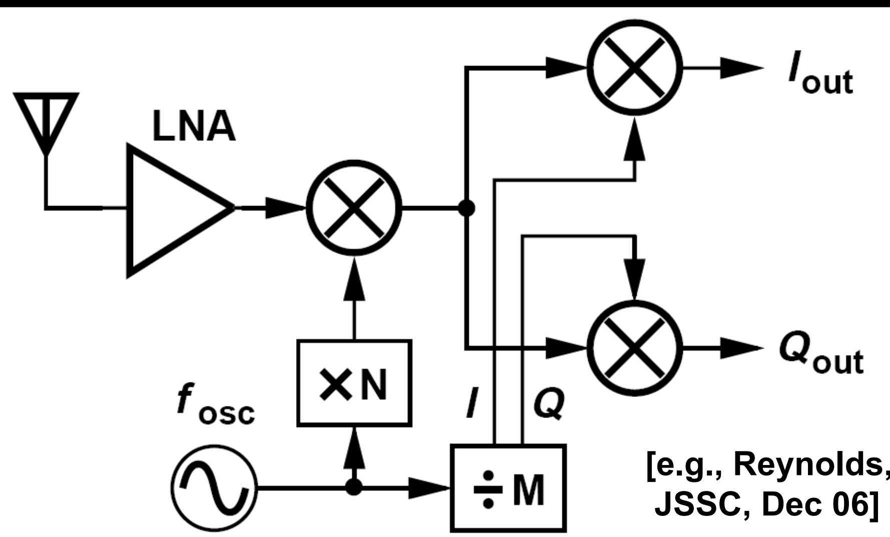
Direct-Conversion RX with 30-GHz LO



- **Quadrature generation is difficult.**
- **Distribution is difficult.**

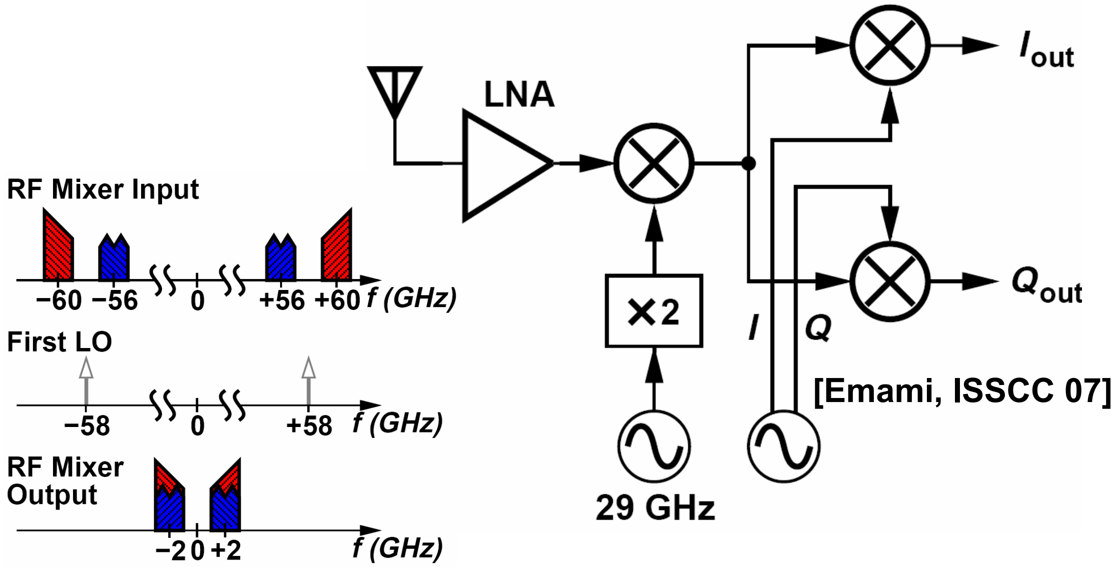
→Need "synthesizer-friendly" transceiver.

Heterodyne Receiver



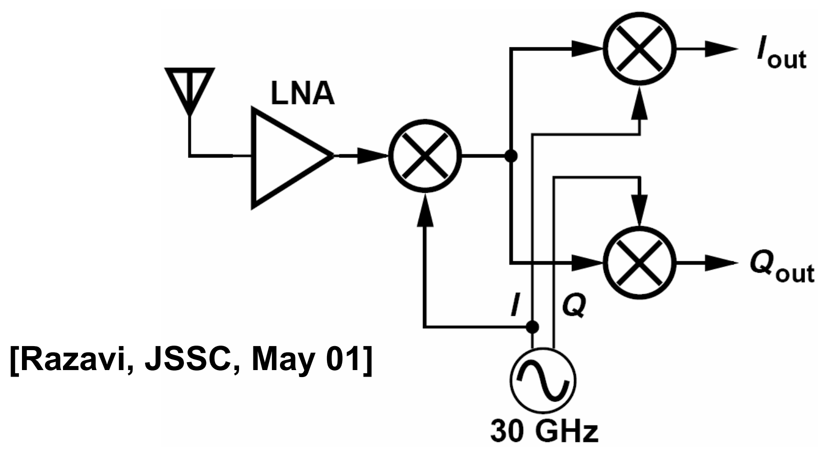
- **Multiplier has high loss and needs its own inductor.**

Problem of Low-IF Heterodyne



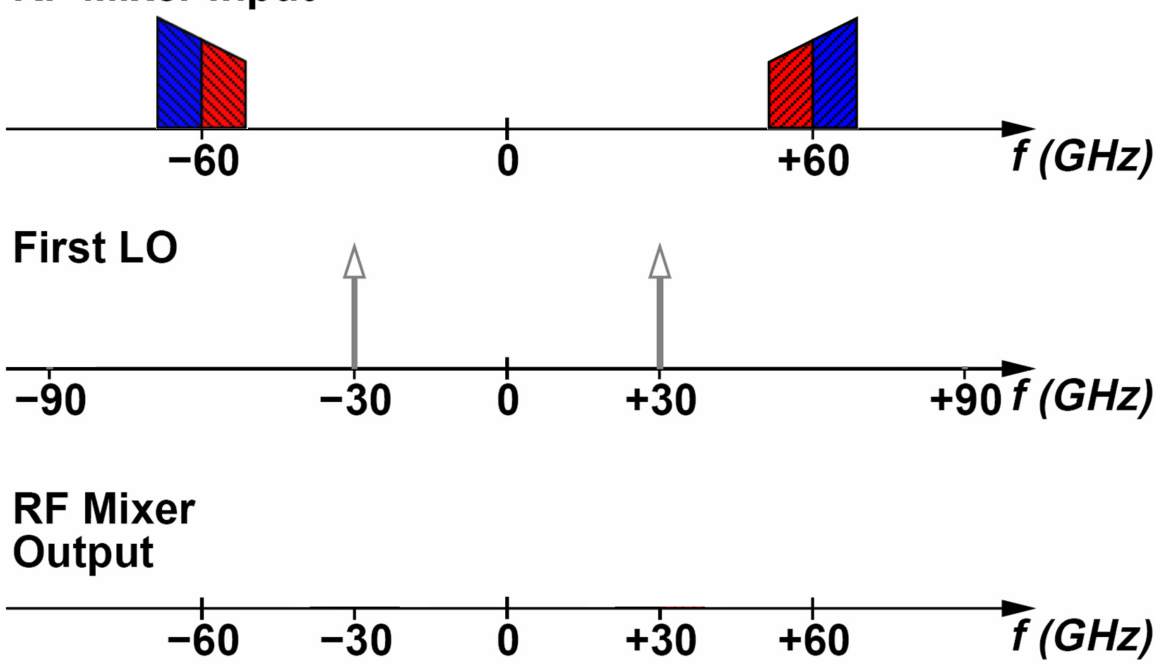
- Image of the first mixer is in the band.
- Receiver NF is increased by ~3 dB.

Example of Synthesizer-Friendly Receiver



- No extra divider/multiplier needed.
- Image is at DC.
- But,
  - Third harmonic of LO causes corruption.
  - LO-IF feedthrough may desensitize the IF mixers.
  - 1/f noise is upconverted in RF mixer.

Problem of LO Third Harmonic



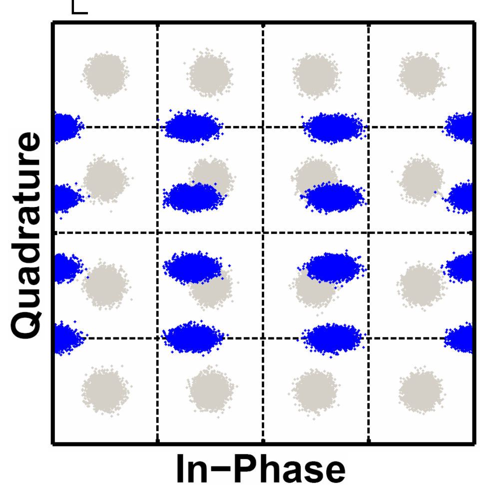
Analysis

$$x_{BP}(t) = \Re\left[x_{BB}(t)e^{+j2\pi f_{RF}t}\right]$$

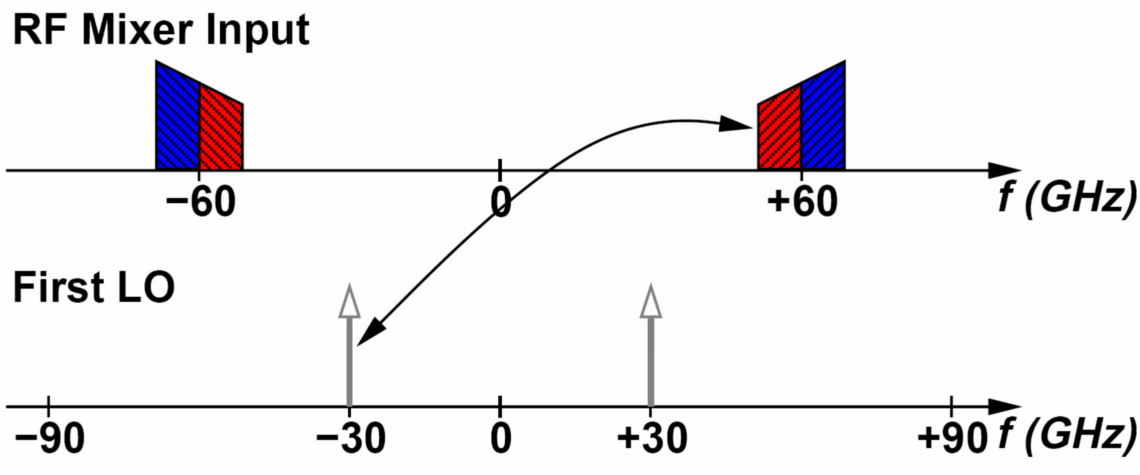
$$LO = \cos\omega_{LO}t + \alpha\cos 3\omega_{LO}t \quad \alpha \approx 1/3$$

$$x_{IF}(t) = \Re\left[\frac{x_{BB}(t) + \alpha x_{BB}^{*}(t)}{2} e^{+j2\pi f_{IF}t}\right]$$

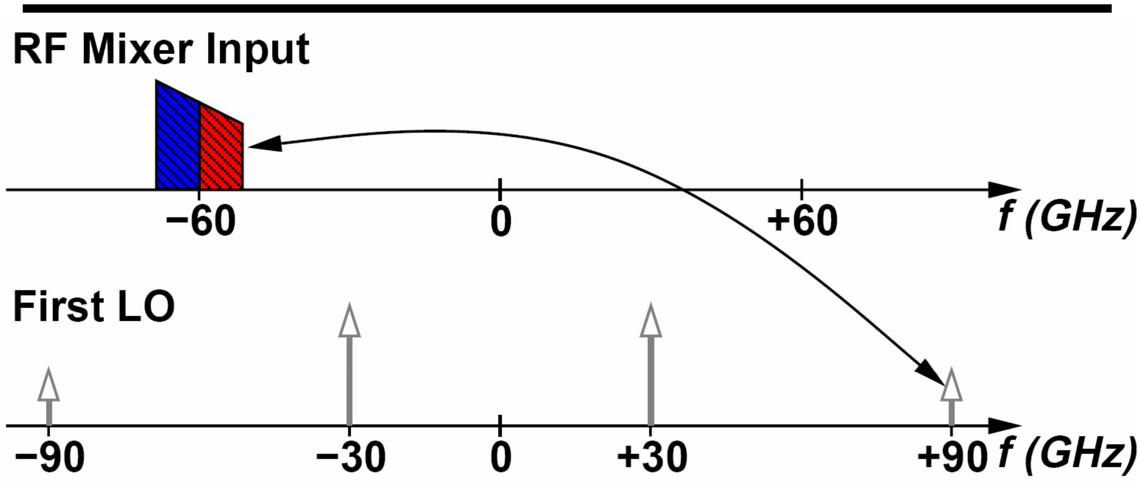
SNR = 25 dB



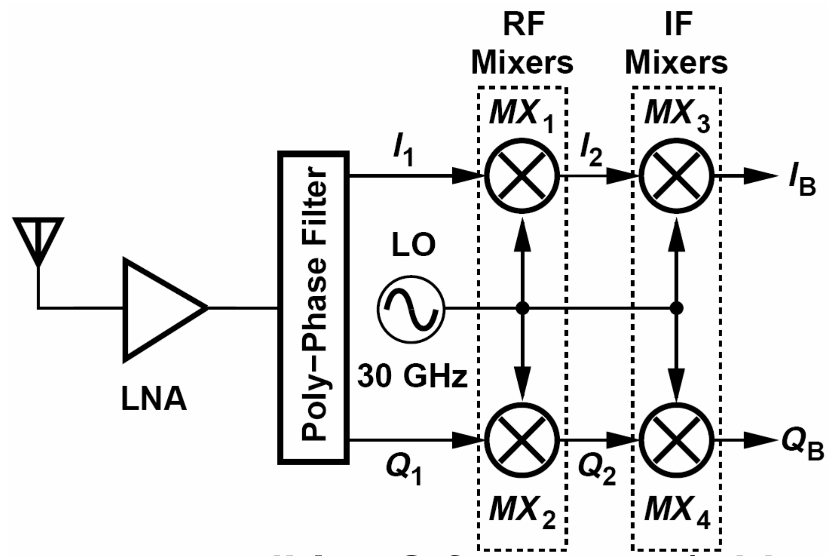
Linearize LO Port?



Alternative Solution

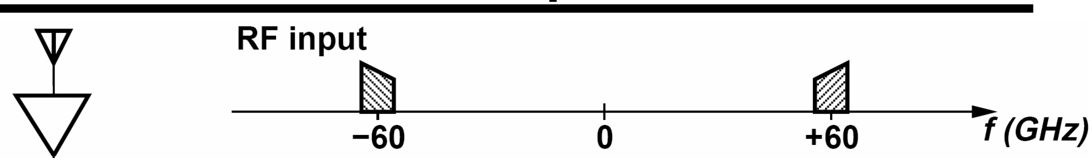


Proposed Architecture

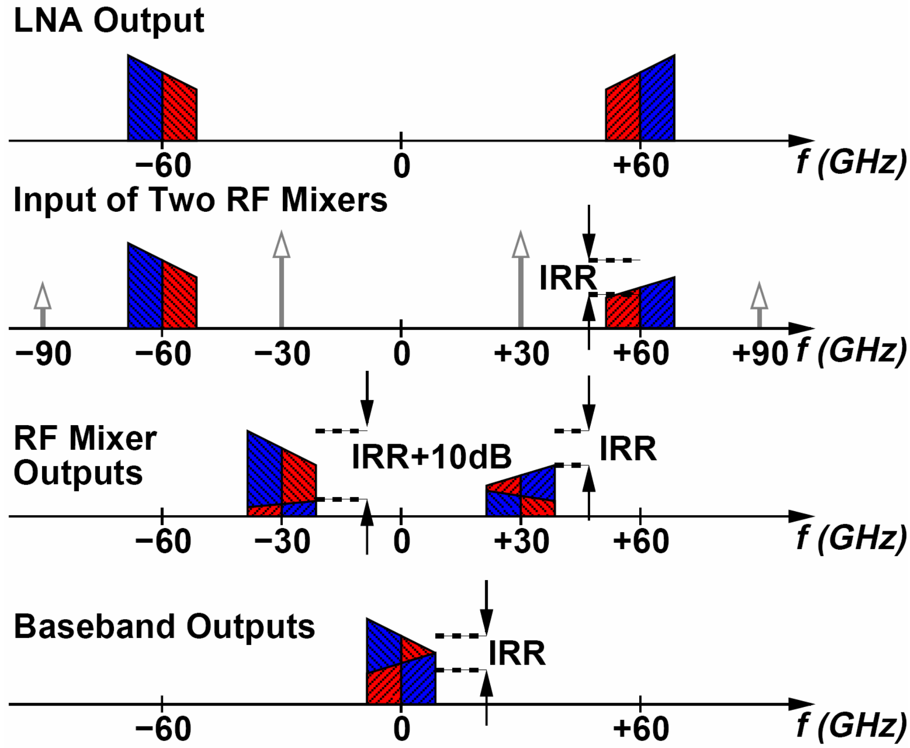


- Lowest possible LO frequency (without multiplication).
- No quadrature LO phases required.

Receiver Spectra

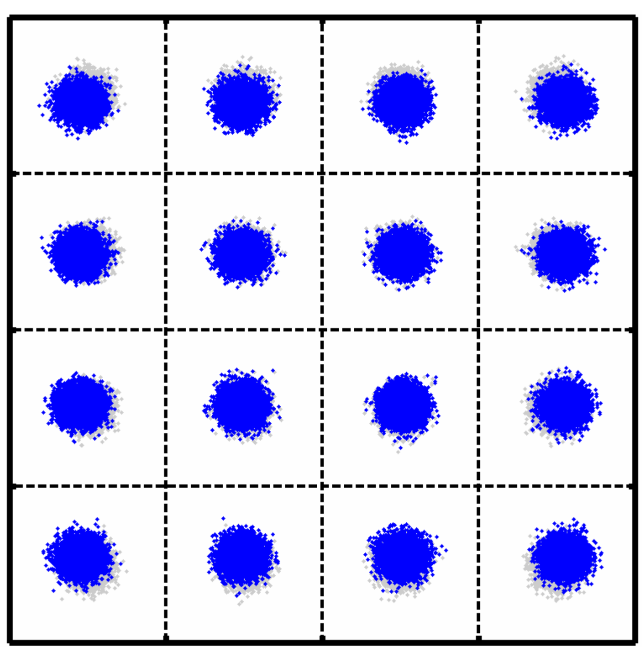


Effect of Mismatches



16-QAM Constellation

SNR=25 dB
IRR=30 dB

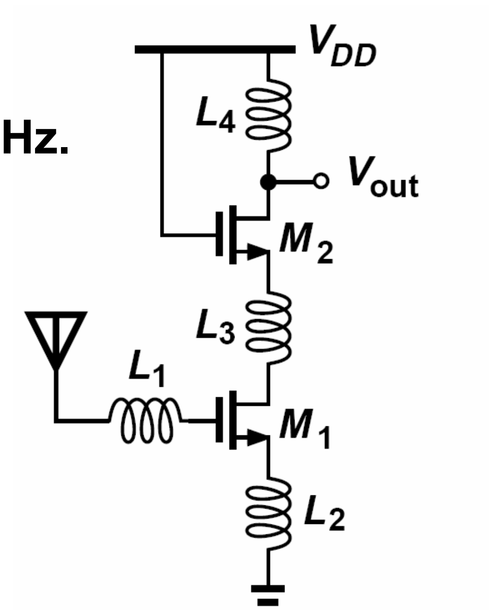


Building Blocks

- LNA
- Polyphase Filter
  - LNA interface
- Mixers

LNA

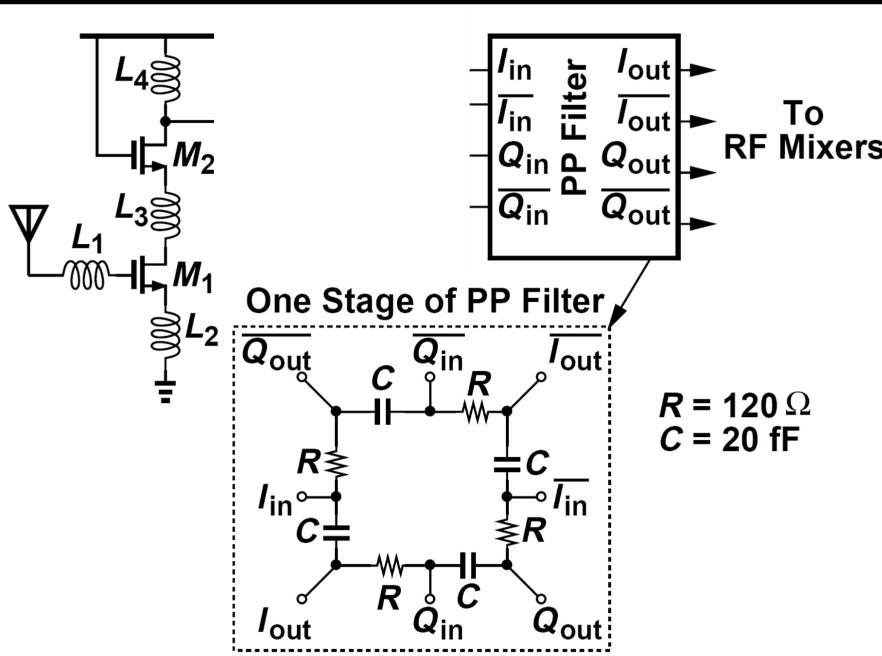
- Pole at node *X* in 90-nm CMOS is around 60-70 GHz.
- Parallel resonance.
- Series resonance.
  - Wider bandwidth
  - No need for large bypass capacitor



Polyphase Filter

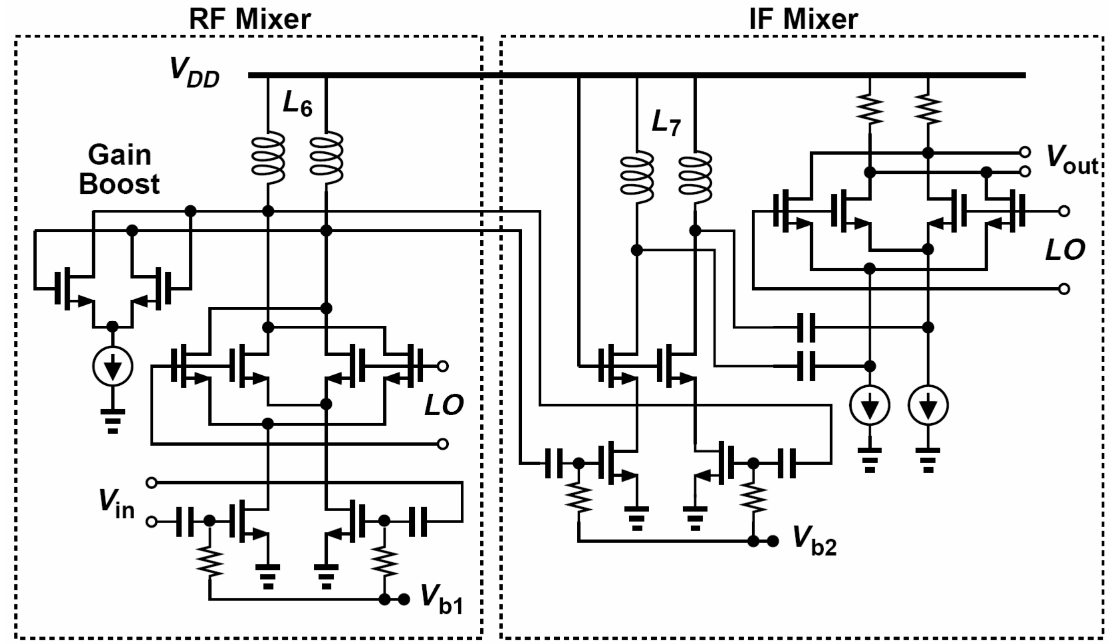
- **Microwave Hybrid [Wang, ISSCC 07]**
  - Large area
  - High loss
  - Low impedance
- **Current-Mode Quadrature Seperation [Razavi, ISSCC '07]**
  - Does not convert single-ended to differential.
  - Component values too small at 60 GHz.

LNA Polyphase Buffer



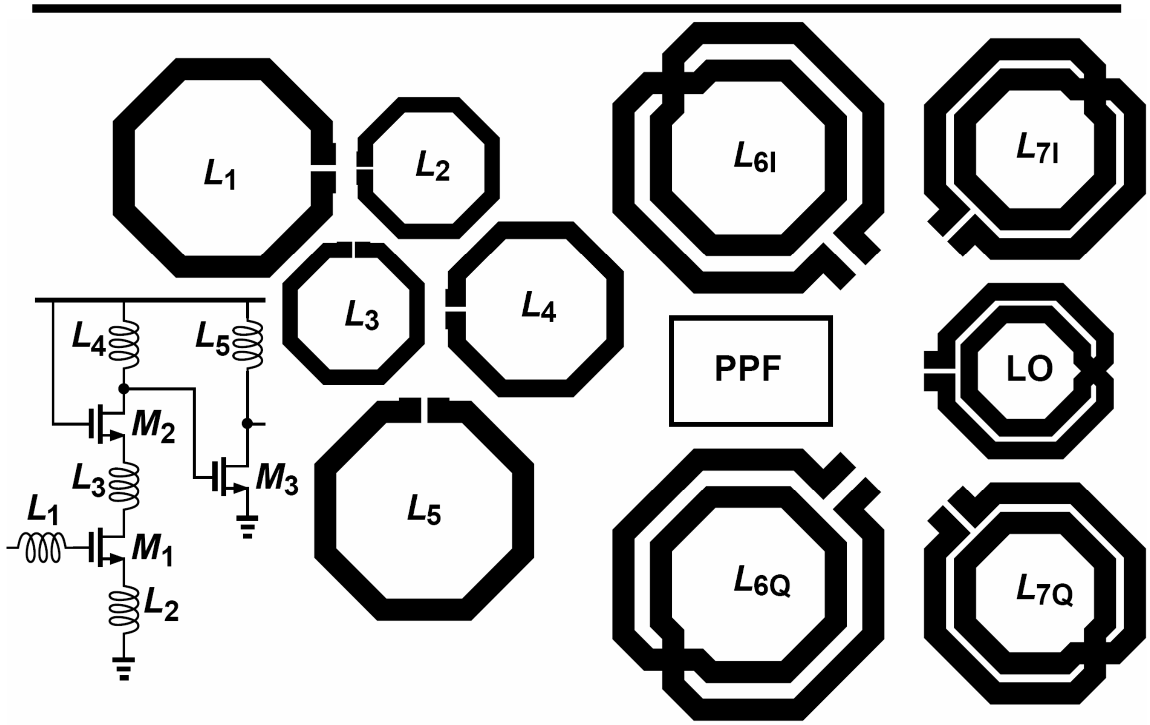
- NF of polyphase + LNA is around 15 dB.
- Polyphase allows double-balanced RF mixers →No desensitization of IF mixers.

RF and IF mixers

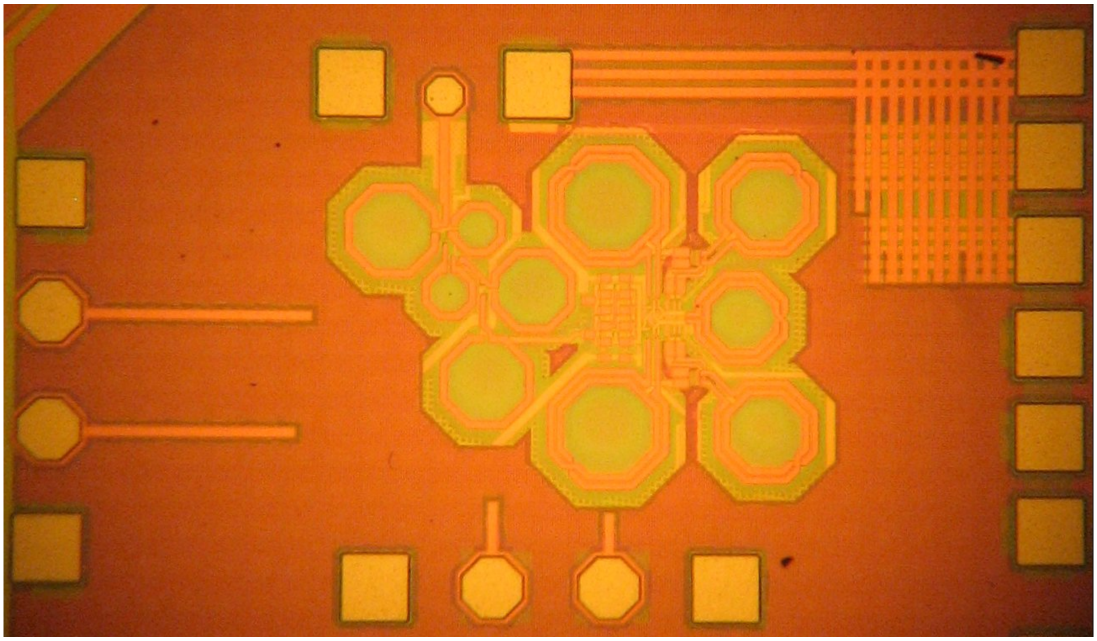


Gain boost stage to provide more gain

Floor Plan

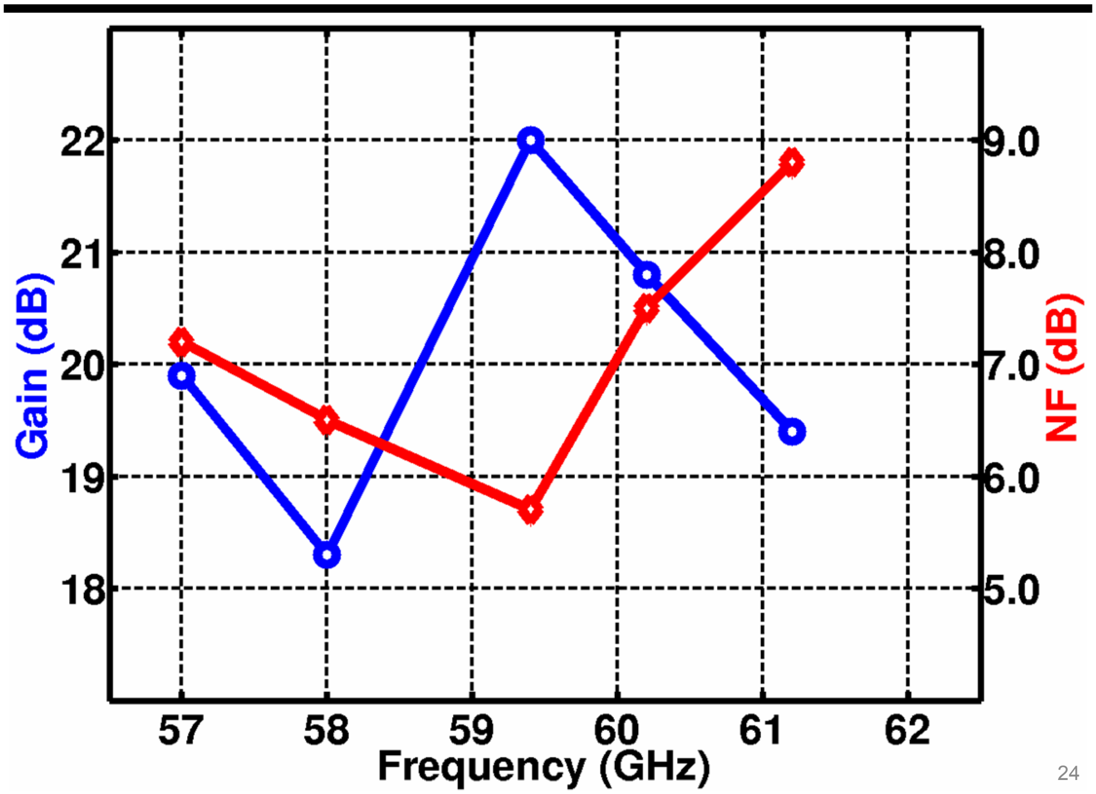


Die Photograph

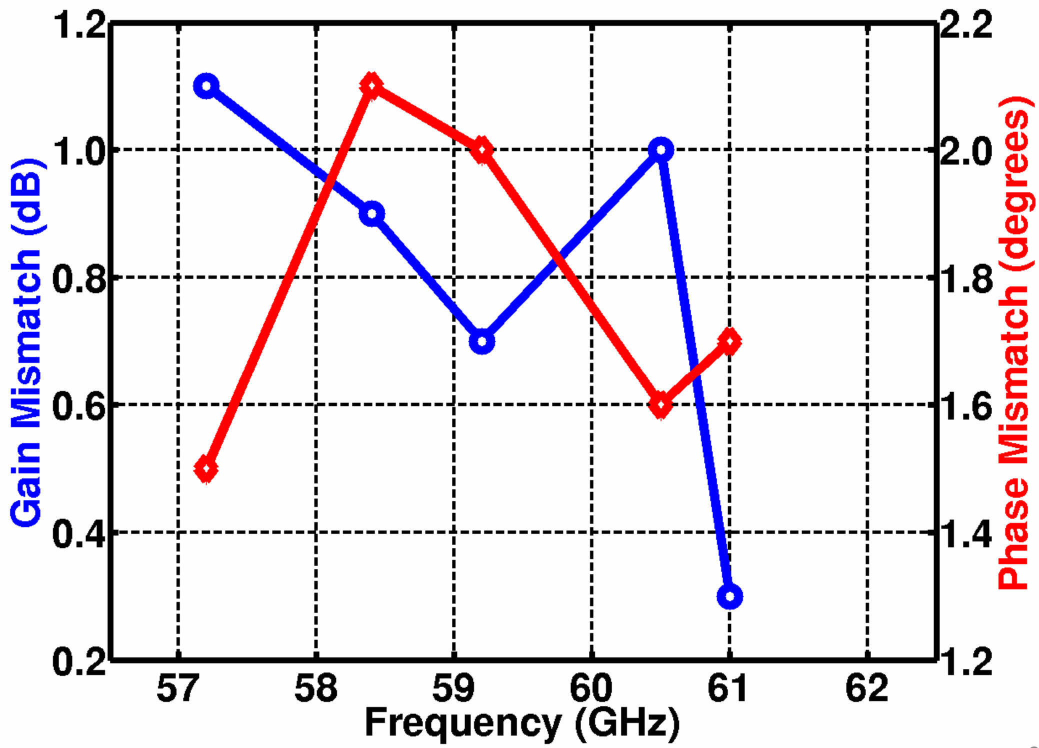


Fabricated in TSMC's 90-nm CMOS technology.
Active area: 500 µm x 370 µm

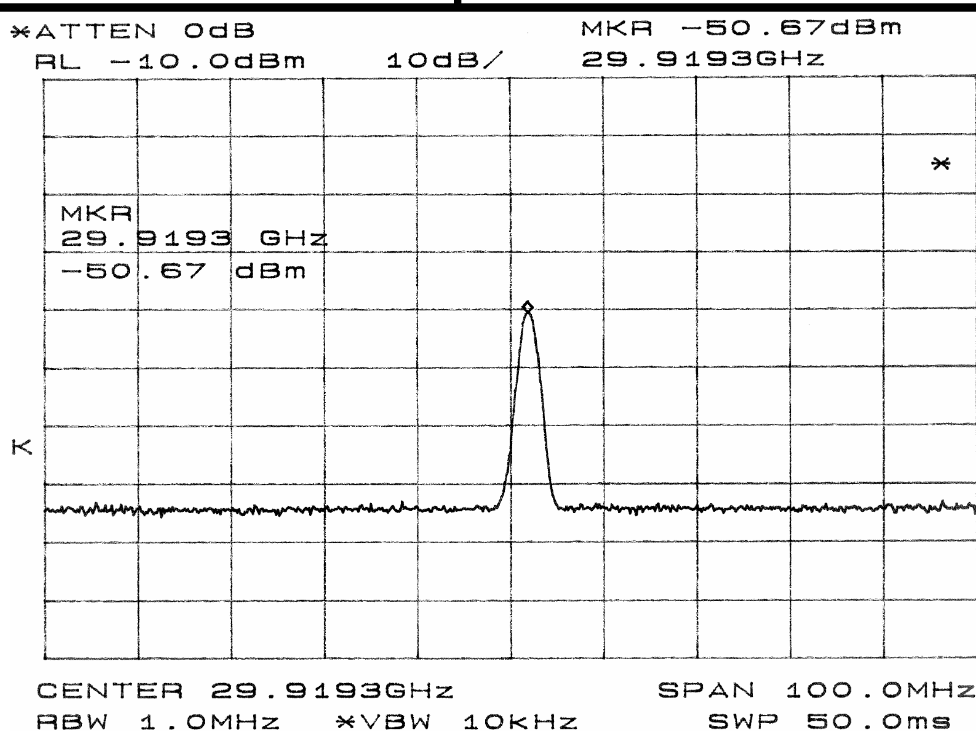
Measured NF and Gain



Measured Quadrature Mismatch



LO Spectrum



Comparison

	Receiver in [3]	Receiver in [1]	This work
Noise Figure (dB)	10.4-11	6.9-8.3	5.7-8.8
Gain (dB)	9.5-12	26-31.5	18.3-22
P_{1dB} (dBm)	-15.8	-25.5	-27.5
LO Leakage to Input (dBm)	N/A	-47	-65
I/Q Mismatch	N/A	6.5°/ 1.5dB	2.1°/ 1.1dB
LO Phase Noise (dBc/Hz @ 1-MHz offset)	-86	-95	-87
Power Dissipation (mW)	77	80	36
LNA			9
Mixers			23
Oscillator			4
Supply Voltage (V)	1.2	1.8	1.2
CMOS Technology	0.13-µm	90-nm	90-nm

[1] B. Razavi, ISSCC '07
[3] S. Emami et al, ISSCC '07

Conclusion

- Choice of architecture plays a great role in the level of integration.
- A new architecture incorporates a single 30-GHz oscillator, making it a "synthesizer-friendly" architecture.
- The receiver achieves the lowest power consumption at 60 GHz.

Acknowledgement

- We are indebted to TSMC for chip fabrication.
- This work was supported by Realtek Semiconductor and Skyworks, Inc.