
Robust Synthesis for Defective Nano Devices

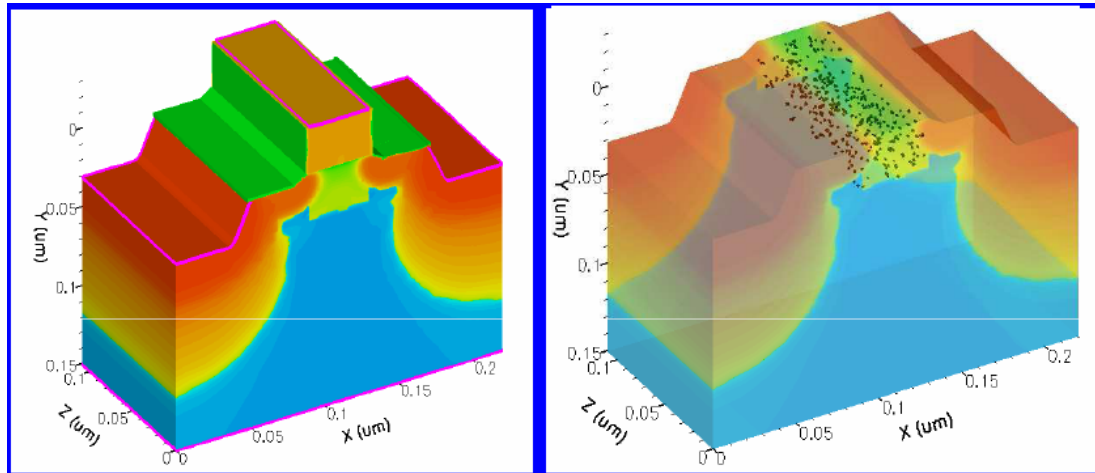
Lei He

Electrical Engineering Department
University of California Los Angeles

Outline

- Introduction
- Existing results for FPGA in scaled CMOS
- Ongoing work for defective nano devices
- Other research in my group

Process Variations for Scaled CMOS



- Example [Intel, IEDM'07]
 - Decreased channel area means that MOS threshold voltage variation due to random dopant fluctuations (RDF) is an increasingly significant effect

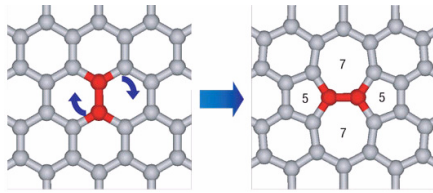
Defects for Scaled CMOS

Yield Model and Defect Budget in IRTS'05

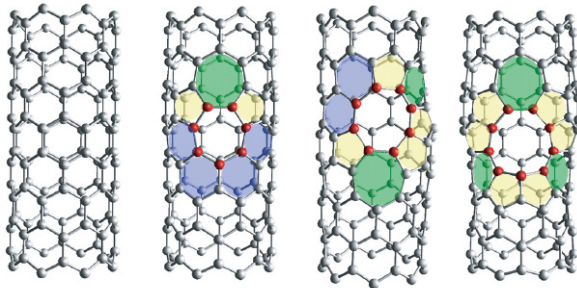
Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted) [A]	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
Critical Defect Size (nm)	40	35	32.5	28.5	25	22.5	20	17.5	16
Chip Size (mm ²) [B]	88	139	110	74	117	93	74	117	93
Cell Array Area (%) at Production [B]	63%	63%	63%	56%	56%	56%	56%	56%	56%
Non-core Area (mm ²)	32	51	41	32	51	41	32	51	41
Overall Electrical D_0 (faults/m ²) at critical defect size or greater [C]	5220	3288	4143	5219	3288	4143	5219	3288	4143
Random D_0 (faults/m ²) [D]	3517	2216	2791	3516	2215	2791	3516	2215	2791
Number of Mask Levels [E]	24	24	24	24	24	26	26	26	26
Random Faults/Mask	147	92	116	147	92	107	135	85	107

- Chip level defect rate rises over generations due to the increasing area
- Soft errors increases due to both area and more-vulnerable devices

Defects in Nano Technologies



Suenaga, Nature Nanotechnology 2007



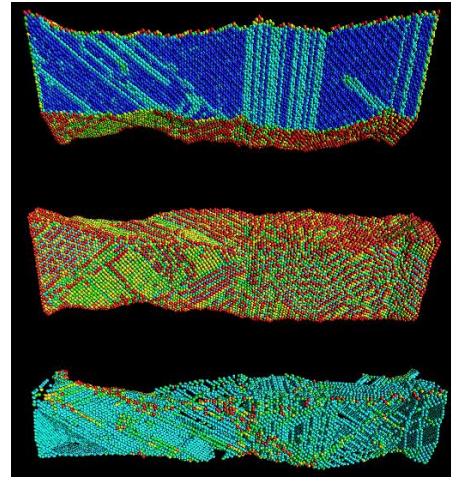
(8,0)

$n=7$

$n=8$

$n=9$

Nishidate, ISSS 2005



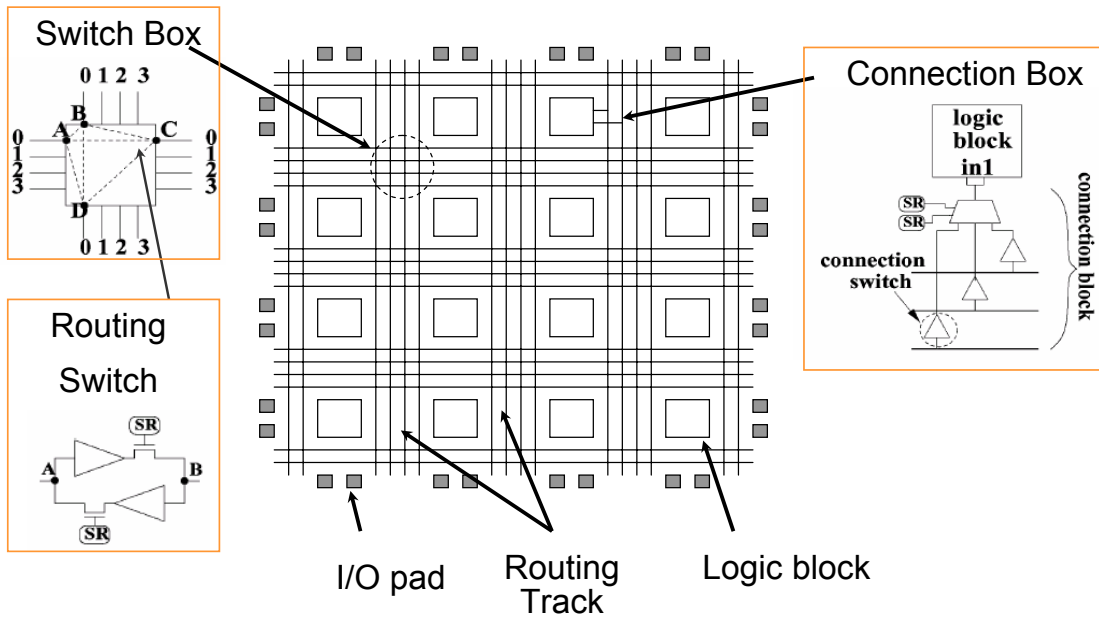
Zhou, Nano Letters 2005

- Defect rate could be up to 20%

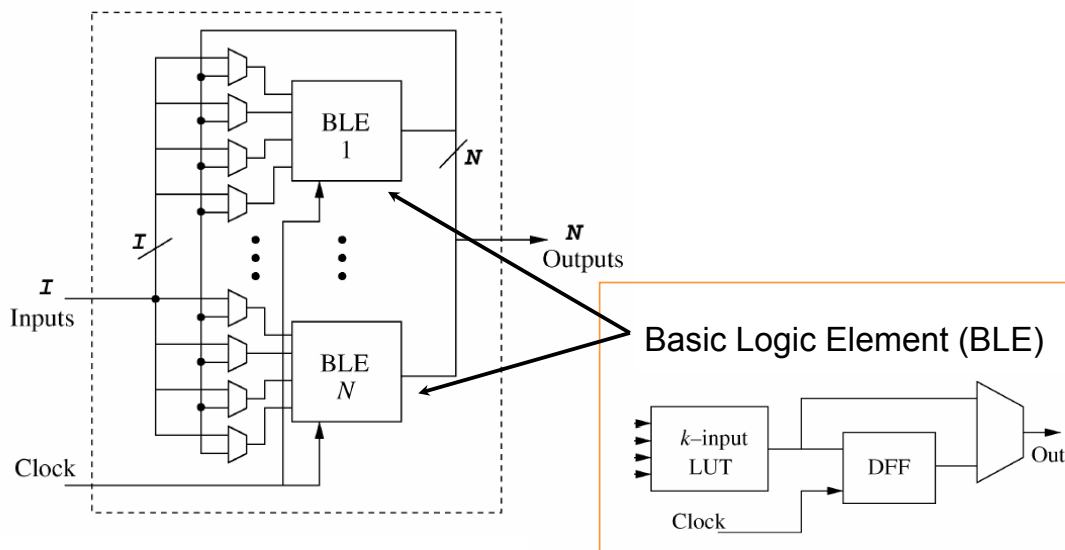
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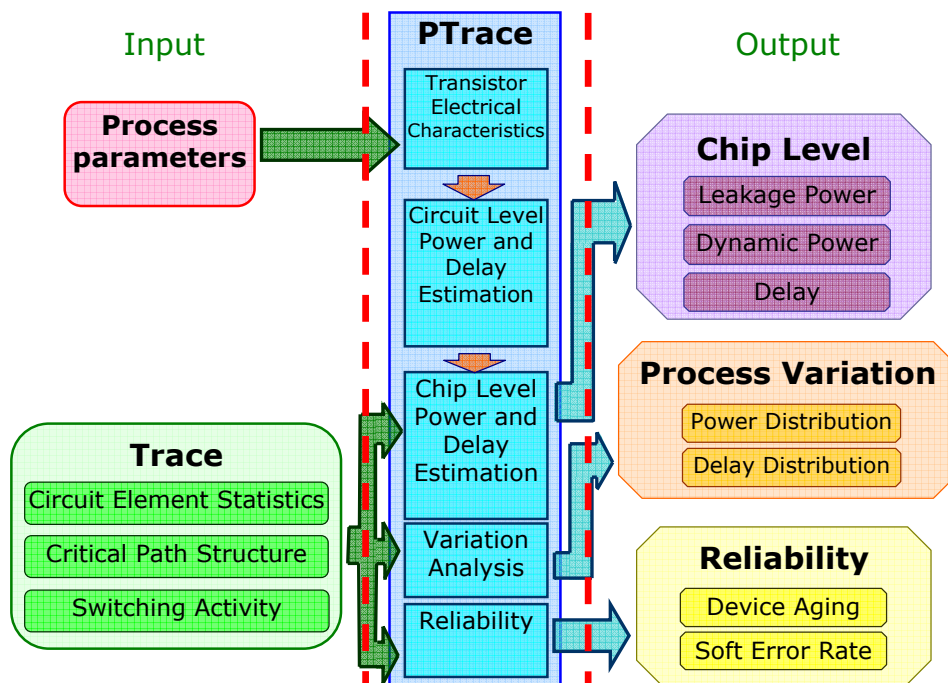
Island Style FPGA Architecture



Cluster-Based Logic Block

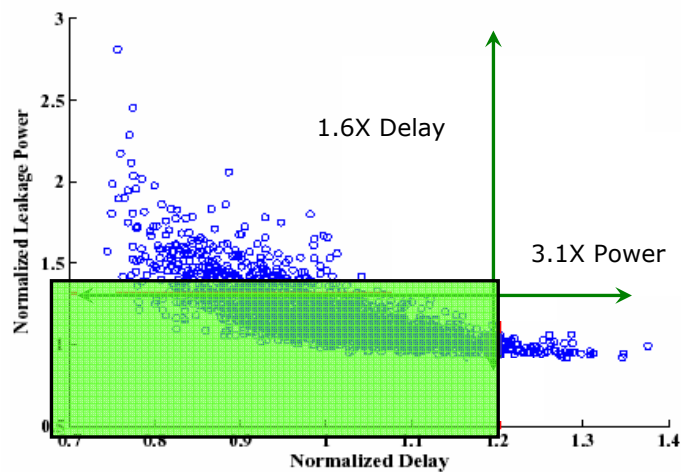


Con-current Process and Circuit Optimization



Process Variation in 100nm Technology

- Delay and leakage power are significantly affected by process variation
 - 1.6X delay variation
 - 3.1X leakage power variation



Process and Circuit Co-Optimization

- ITRS 32nm technology

	LUT size	L_{gate}	Delay Yield %	Power Yield %	Combine Yield %
Baseline	4	32	89.2	72.5	62.5
Min Delay Yield	7	31	95.2 (+6.0%)	52.1	55.7
Min Power Yield	4	33	81.4	83.2 (+10.7%)	61.5
Min combine Yield	5	33	87.2	81.6	70.1 (+7.5%)

Stochastic Synthesis

- Motivation
 - Variations
 - Pre-routing interconnect uncertainty
 - Process variation
 - Impact
 - Any near-critical paths → statistically timing critical
 - Static time analysis (STA) ignores near-criticality
- Stochastic static timing analysis (SSTA) to replace STA
 - For packing, placement, and routing

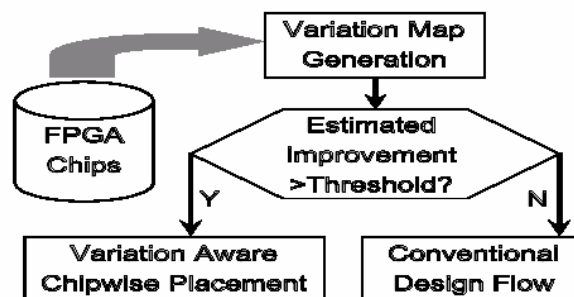
Stochastic vs Deterministic

- Hybrid of stochastic and deterministic is able to reduce delay, delay variation, and design time

	Nominal (nm)	Mean (nm)	Sigma (nm)	Run time
Deterministic	21.2	22.9	2.4	1X
Stochastic	-6.3%	-6.2%	-7.5%	3X
Hybrid	-3.7%	-5.0%	-6.4%	0.99X

Chip-Wise Placement

- FPGA can be programmed to obtain variation map
 - Either chip-wise testing or binning
- Placement can be customized for each chip/bin to improve delay



Delay Reduction by Chip-Wise Placement

- 60 variation maps in ITRS 65nm technology

Benchmark	Average Reduction %
clma	6.91
s298	7.32
diffeq	7.89
spla	12.10
Average	8.56

Multi-Configuration [Matsumoto, Sedcole, ISFPGA'07]

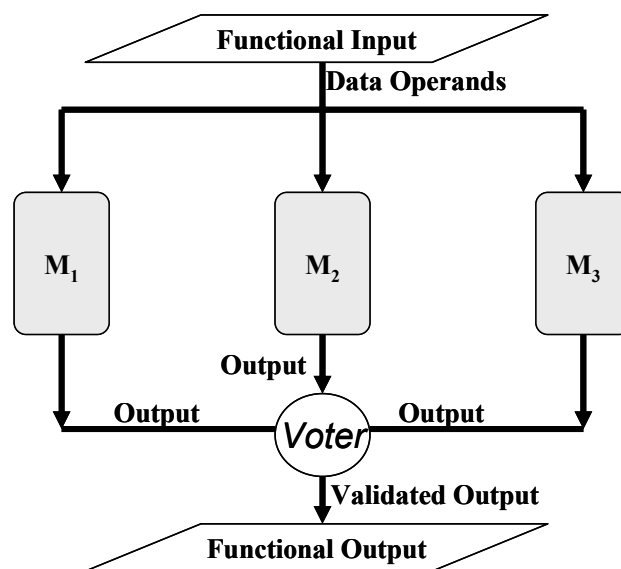
- Perform several configuration (placement and route) for each chip, and then choose the best one
- Average 3.3% delay reduction
 - STARC 90nm technology
 - 10 candidate configurations

Benchmark	Average Reduction %
alu4	2.8
apex2	2.5
apex4	4.6
bigkey	3.5
Average	3.3

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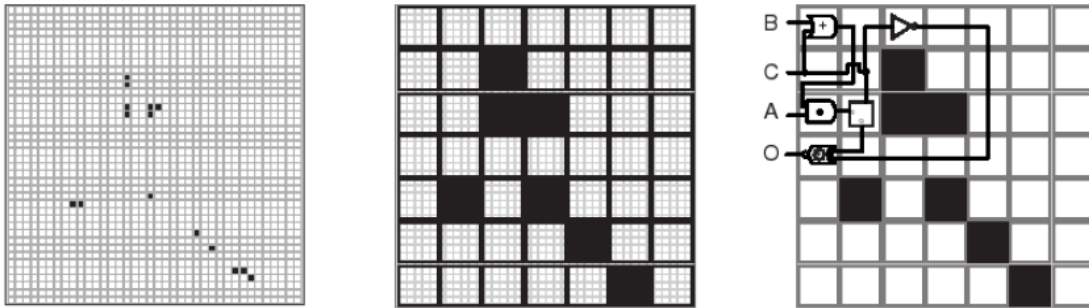
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Existing Robust Synthesis



- Triple module redundancy (TMR) has extremely high circuit overhead

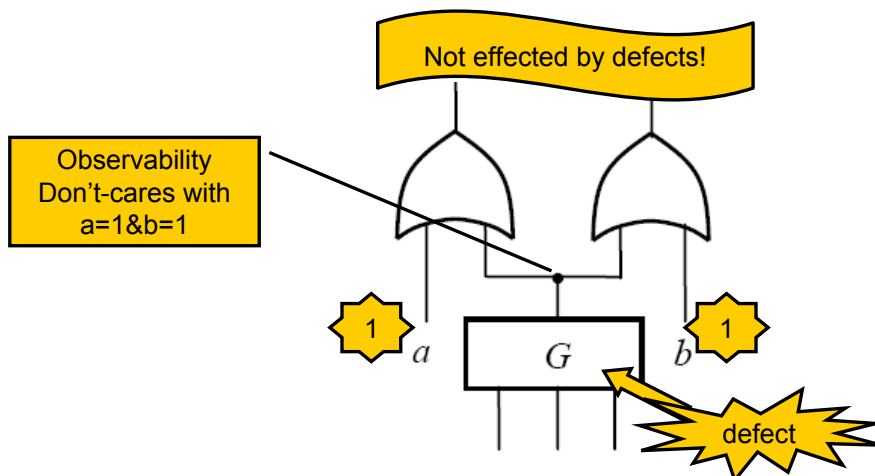
Exciting Robust Synthesis



- Chip-wise synthesis has extremely high testing and design cost
 - Strictly chip-wise, not possible to bin chips to reduce cost

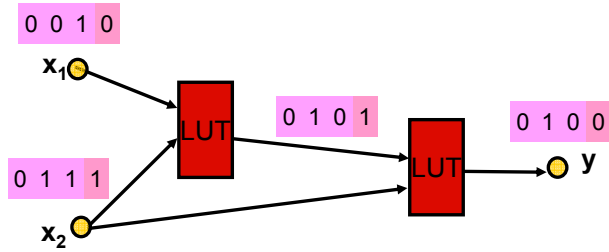
Alternative: Logic Masking

- Defects are created equally but not propagated equally
- Logic don't-cares may mask the propagation of defects

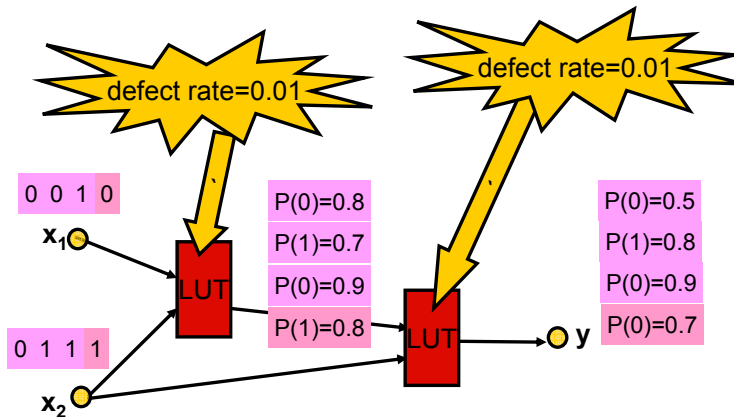


Deterministic vs. Stochastic

Deterministic Boolean space



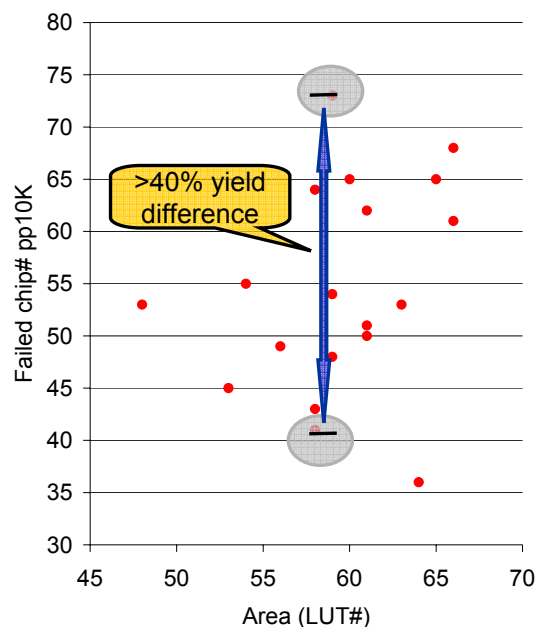
Stochastic Boolean space



There is a lot room for improvement

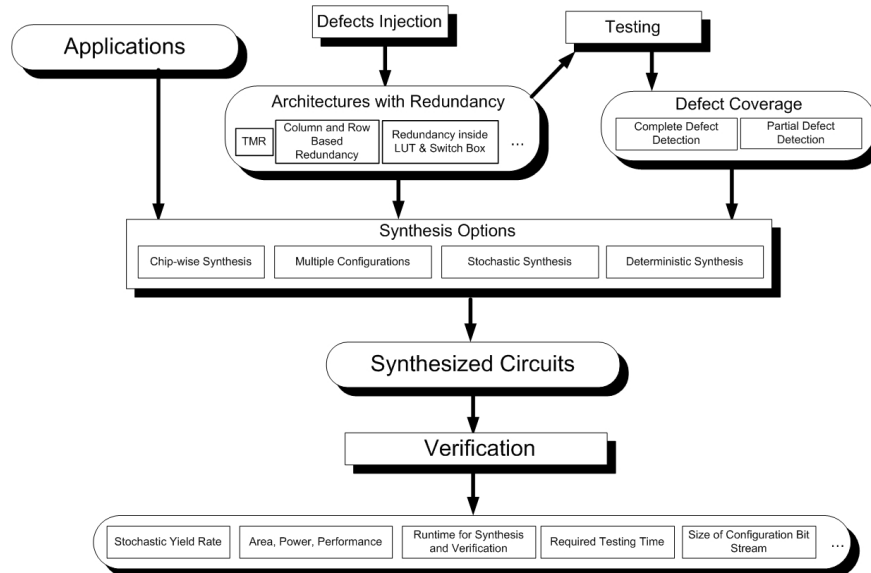
- Test bench
 - MCNC benchmarks
 - LUT-4 based FPGAs
 - Configuration bits are vulnerable to defects (0.01% defect per LUT)
- Evaluation method
 - Multiple implementations with same function
 - Monte Carlo simulations to calculate yield
- Key Observation
 - **Significant yield difference exists for synthesis results with similar area**

Yield loss for "ttt2" over different defect rates and area (defect rate: 0.01% per LUT)



Research Overview of Robust Synthesis

- Theoretical foundation for stochastic synthesis using stochastic satisfiability
- Combining chip-wise and multi-configuration synthesis with stochastic synthesis
- Defect-tolerant FPGA architecture co-designed with defect-tolerant synthesis



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FPGA and Multi-Core

- **Power, variation and reliability in FPGA**
 - Modeling and architecture evaluation
 - Processing and architecture co-optimization
 - FPGA using mixed LUT and macro-gate (i.e., how to select cell library)
 - FPGA in emerging technology (non-CMOS memory)

- **Multi-core power management for multi-media communication**
 - E.g., video conference with real-time constraint on desktop
 - Video on mobile phone
 - FPGA emulator with re-cognitive radio and multi-core

Interconnect Modeling and Optimization

- **RC and RLC extraction and reduction**
 - First published work on library based capacitance and inductance extraction

- **Interconnect optimization**
 - Low power, dual-Vdd and CMP-aware buffering and routing
 - Optimal tree generation and noise aware routing

- **P/G optimization with power gating**
 - Distributed sleep transistor network (used widely in industry)

SiP (System-in-Package) and 3D Integration

- **Chip-Package Co-Design**
 - I/O planning and placement [ASPDAC'06]
 - Package routing
 - Capacitive-coupled transmission lines with branches [TCAD'06]
- **Power and Thermal Integrity in SiP and 3D IC**
 - Efficient modeling and prediction [best paper nominations, DAC'06 and ICCAD'07]
 - Off-chip decap insertion and planning [ISPD'06, DAC'07]
 - Thermal via insertion in 3D stacking [ISLPED'06]
 - 3D via planning for power resonance and heat removal in 3D stacking [ICCAD'06] (best paper nomination)

Modeling and Optimization for Variations

- Extraction and prediction of variation with correlation and nonlinear/non-Gaussian SSTA
 - Best Paper at ISPD'06
- Clock and floorplanning optimization considering workload dependent temperature gradient
 - [ISPD'07] and [ICCAD'07]
- P/G optimization considering both operational and processing variations
 - Best paper nomination at ICCAD'07
- Pro-active P/G resonance control for loops of inductance

Mixed-Signal Circuits

- **On-chip DC-DC converter**
- **High-speed signaling**
 - Wirelined CDMA for programmable system-level interconnects
 - CDMA for noise-immune signaling
- **Design and run-time tuning to minimize digital switching noise and P/G resonance**
- **Mixed-signal SPICE**
 - Speedup with no loss of accuracy

Acknowledgement of Research Sponsors

