A MIMO DECODER ACCELERATOR FOR NEXT GENERATION WIRELESS COMMUNICATIONS

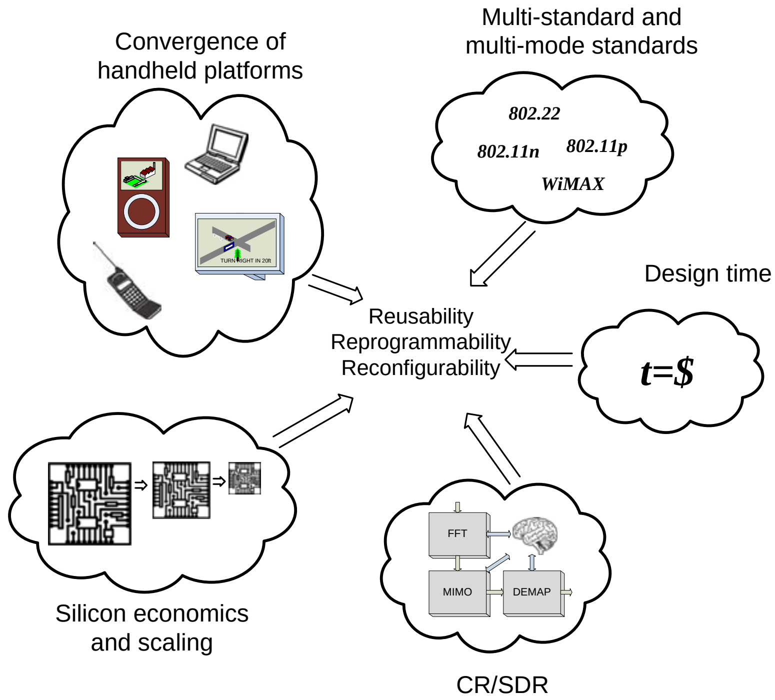
Karim Abbas, Mohammed Ali

Advisor: Babak Daneshrad

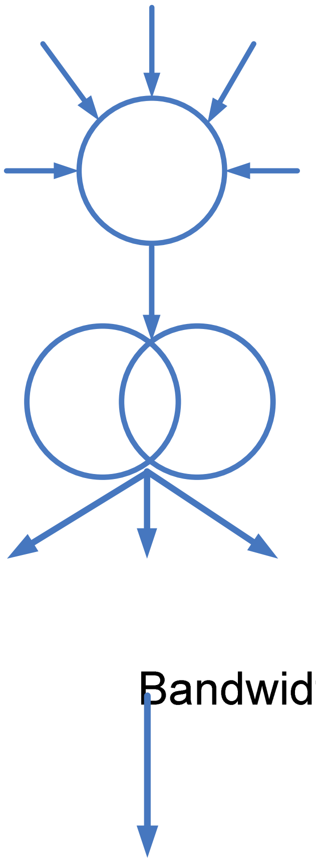
Wireless Integrated Systems Research Lab (WISR)

MIMO-OFDM: Complexity and flexibility

- MIMO-OFDM a feature of emerging wireless standards. Standards have multiple modes and will converge on a single platform
- The need for reconfigurability increased in SDR and CR platforms
- Complex subsystems must be designed and changed quickly
- Trends favor an accelerator-like approach to the design of complex subsystems (e.g. Viterbi decoder or FFT). In MIMO the most dominant subsystem is the MIMO decoder



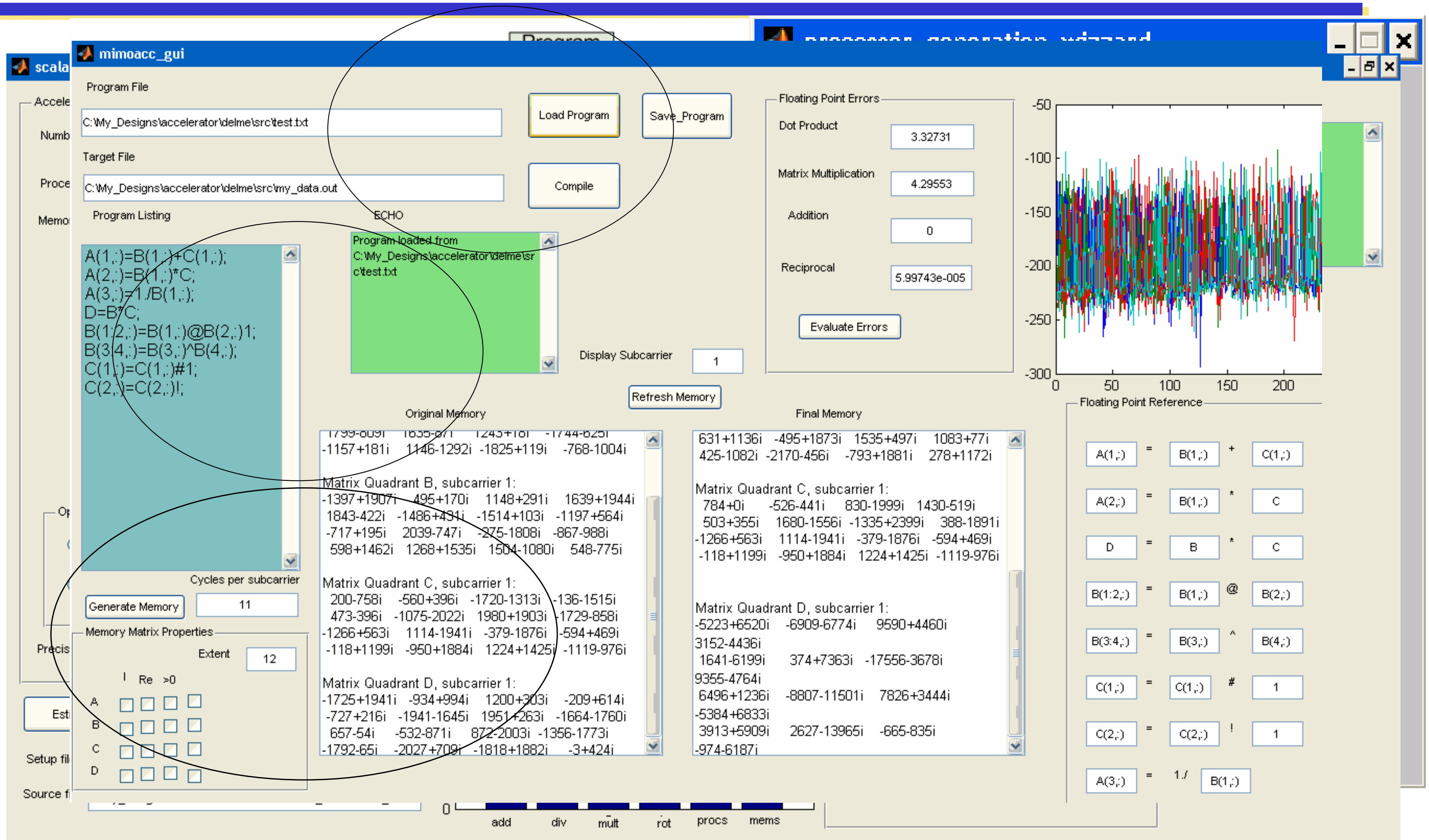
Approach and challenges



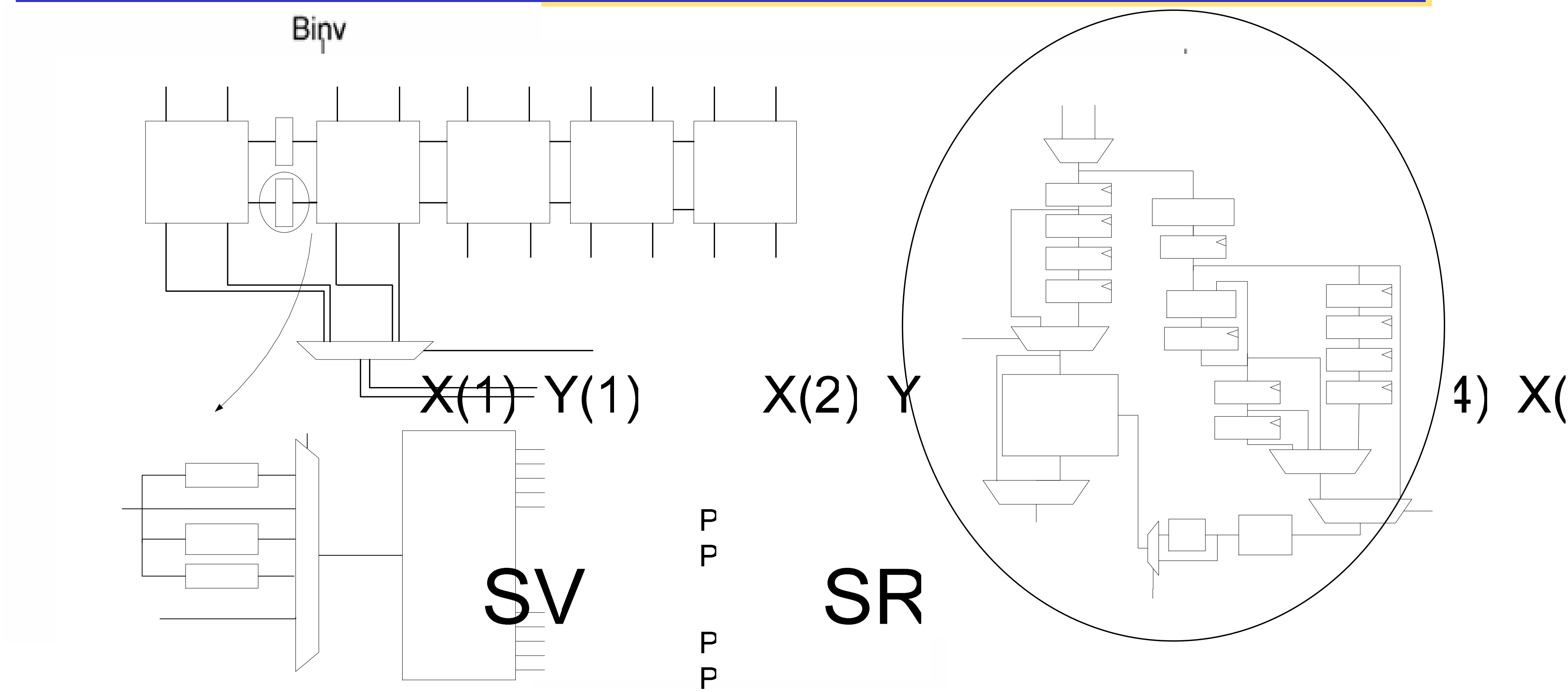
- Accelerator allows high degree of control over design tradeoffs through programming
- Combines features of dedicated architectures and processors (separate data, program, processor)
- Which introduces unique challenges
- Addressed through the domain of target applications

- Leading to DSP-like programmability for the operations of interest. Performance orders of magnitude higher than a DSP and within the order of magnitude of dedicated architectures

User's perspective

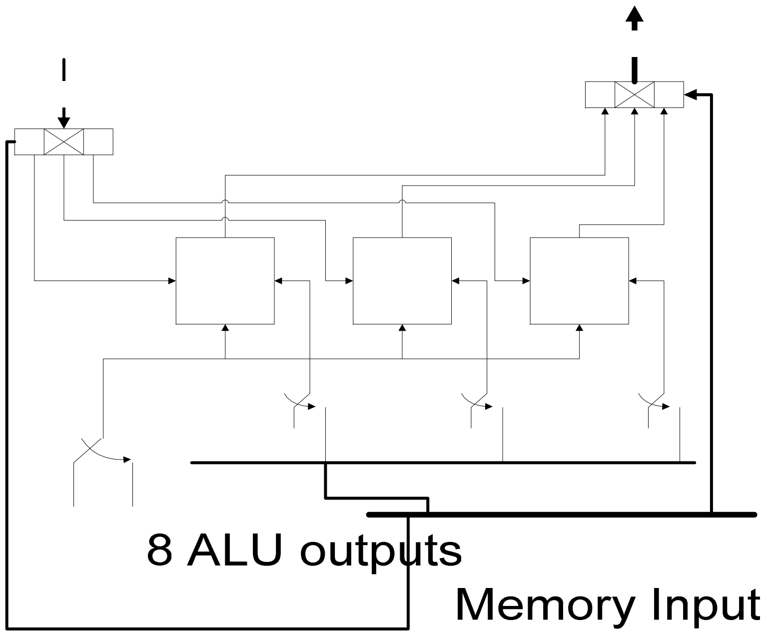


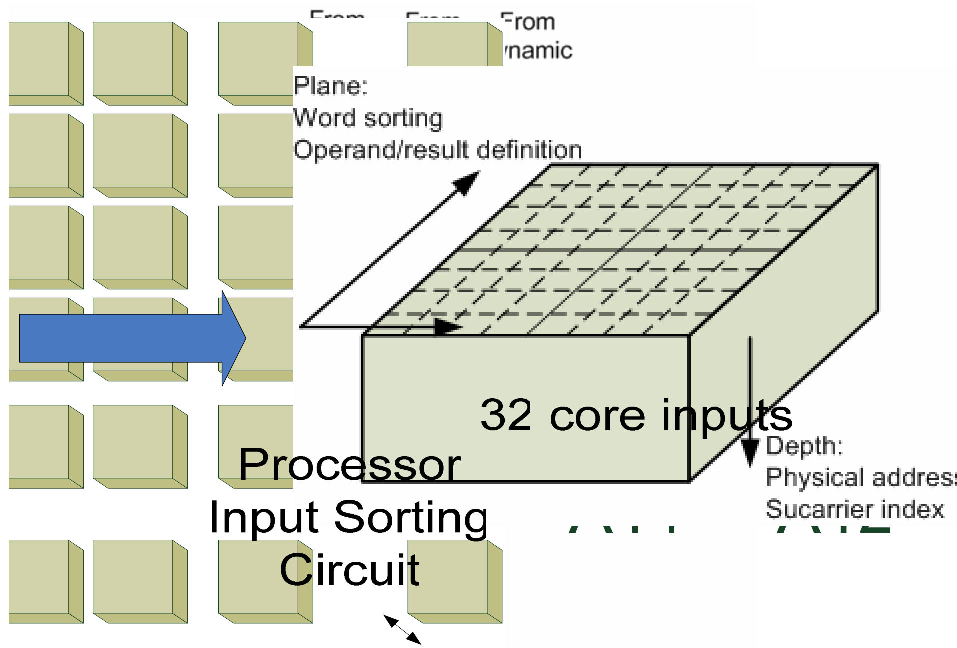
Linear decoding processing core



- Processing core supports operations derived from a minimum operating set of linear MIMO decoders. Core versatility preserves performance but allows breaking down of algorithms while reducing resources
- Programmable two-phase CORDIC units scale to fit (multi) vector transformations necessary for different decompositions with negligible additional cost
- Unitary transformation ... flexibility ... control ...

Matrix-OFDM memory access scheme





A11 A12 A13
A21 A22 A23
A31 A32 A33
A41 A42 A43

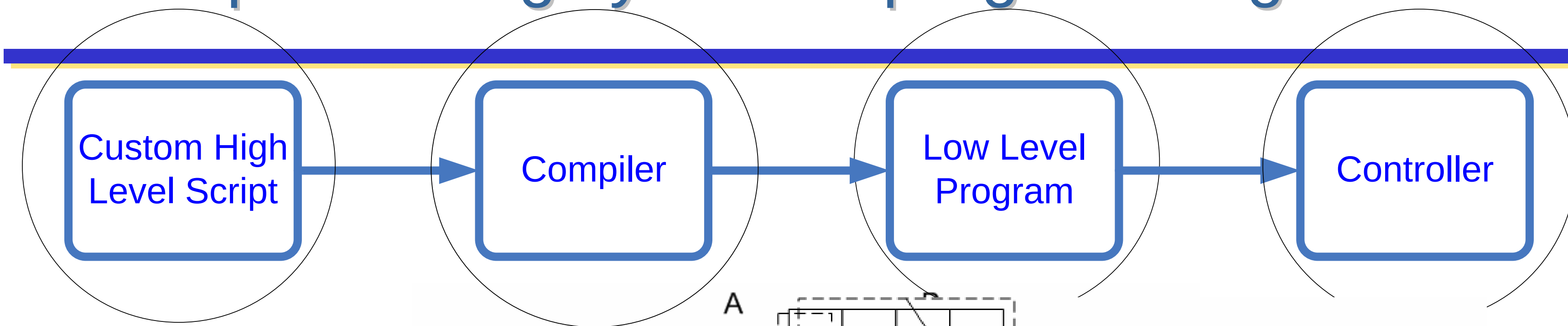
Control
Sorter
Core

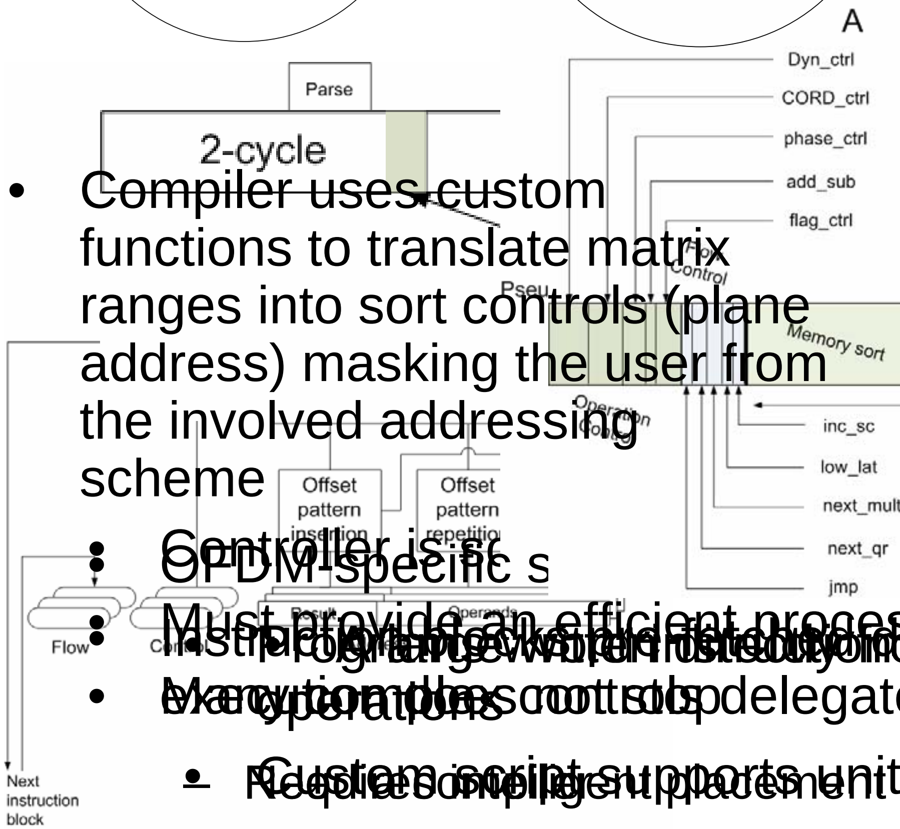
- By realizing the properties of data as complex matrices belonging to different subcarriers:
- Memory organization problem: How to provide 32 inputs from 64 memory elements in 1 cycle?
- Plane addressing reduced to resorting of data between processor and memory ports
- Immediate inputs are stored at different in an independent register
- Address bus is shared between all elements
- Using properties of data I/O at the processor two-level sorting significantly reduces resources allows scalability, while maintaining flexibility of access
  - Memory is transformed into two-dimensional structure with operand addressing moved to the plane
  - Addressing becomes a problem

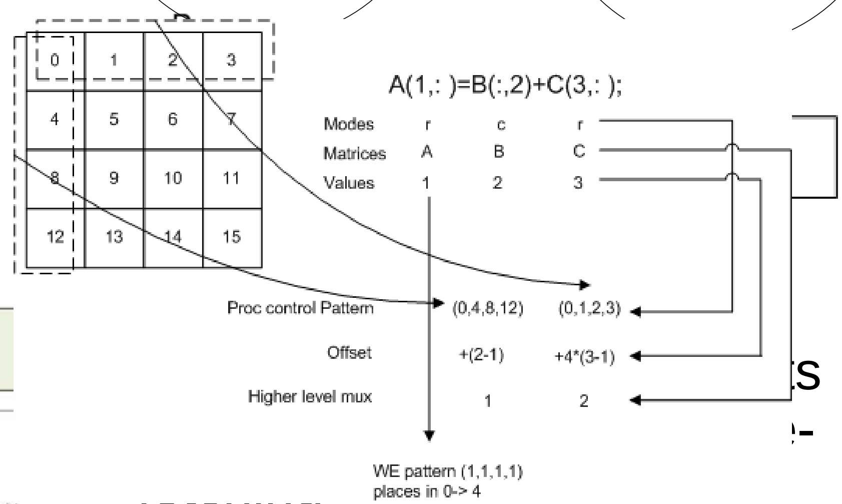
Din A11 WE add
Din A12 WE add
Din A13 WE add
Dout

Address Bus
WE Bus
0 0 0
Nsc

OFDM processing cycle and programming

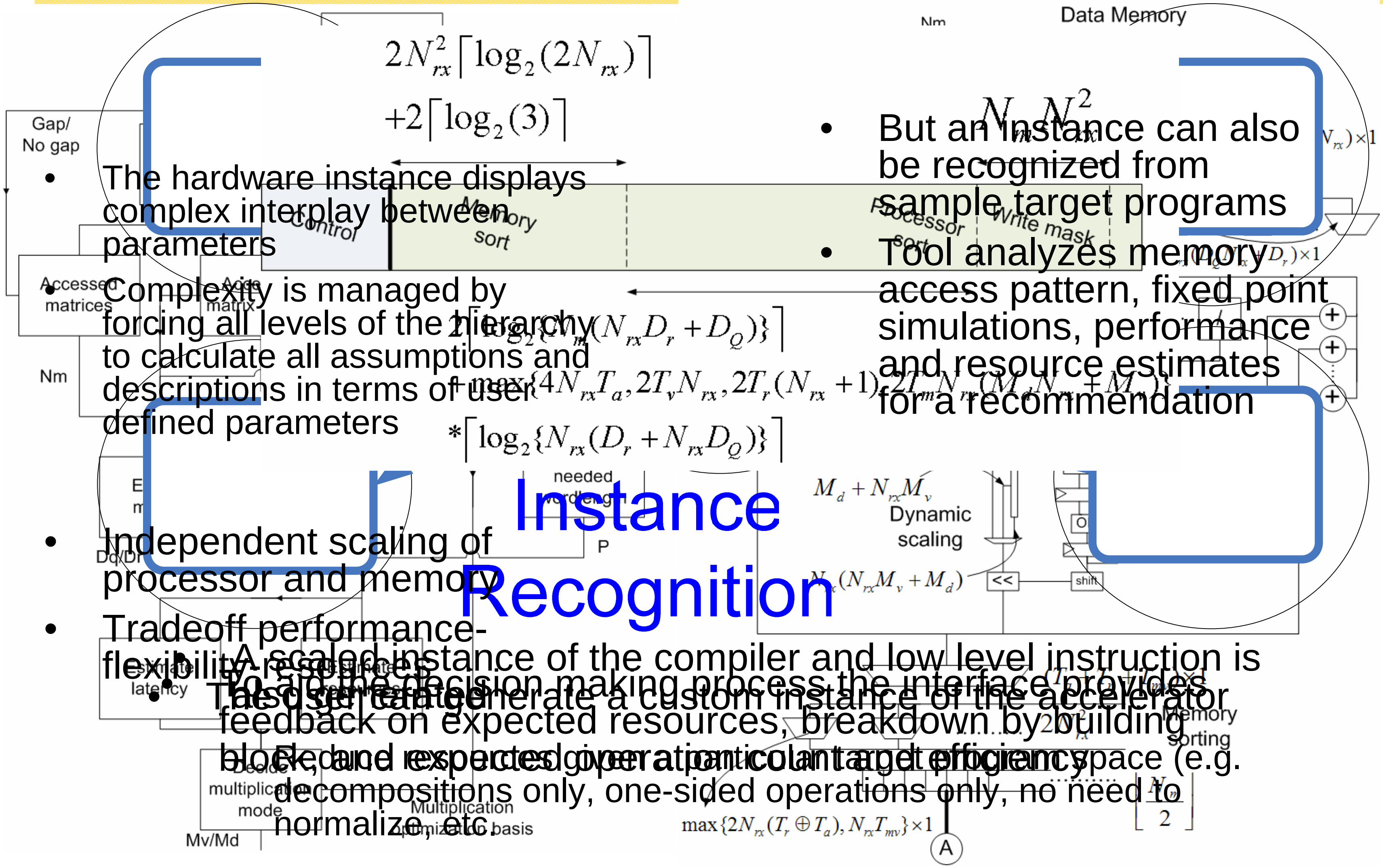






- Compiler uses custom functions to translate matrix ranges into sort controls (plane address) masking the user from the involved addressing scheme
  - Controller is sc... OFDM-specific s... ...rse controls
  - Must provide an efficient processing cycle
  - Instruction ... extended execute cycle,
  - Programs written ... algorithms as vector/matrix operations
  - Many of the controls delegated from hardware to programming
    - Custom script supports unitary operations
    - Requires intelligent placement of state mode control signals

Parameterized scaling and instance recognition



- The hardware instance displays complex interplay between parameters
- Complexity is managed by forcing all levels of the hierarchy to calculate all assumptions and descriptions in terms of user defined parameters
- Independent scaling of processor and memory
- Tradeoff performance-flexibility-resources

- But an instance can also be recognized from sample target programs
- Tool analyzes memory access pattern, fixed point simulations, performance and resource estimates for a recommendation

Instance Recognition

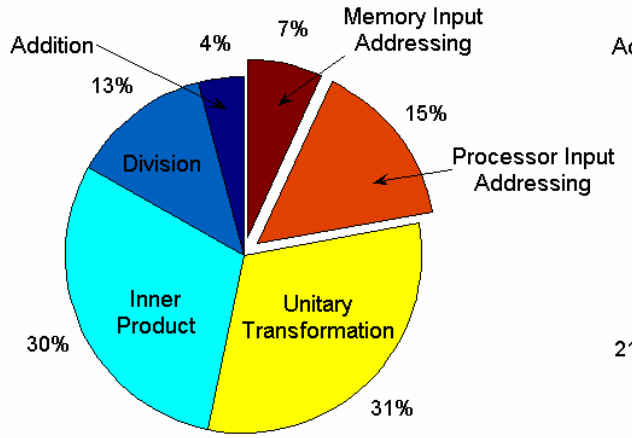
- A scaled instance of the compiler and low level instruction is
- The user can generate a custom instance of the accelerator
- To aid the decision making process the interface provides feedback on expected resources, breakdown by building block, and expected operation count and efficiency
- Reduced … for particular target program space (e.g. decompositions only, one-sided operations only, no need to normalize, etc.

Param…

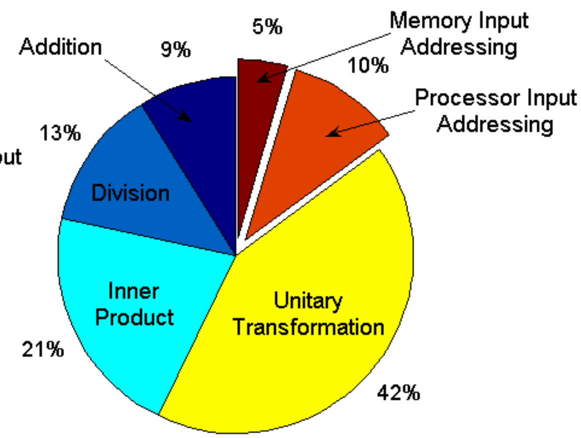
En…

Statistics of an instance

Xilinx V4-LX200	Logic slices		Multipliers		RAMB16		Clk (MHz) V4(SG -11)	V2(SG -5)
	38150/27039	43/30%	0/48	0/50%	72	21%	204	145
65nm TSMC	kGate equivalent	Power (mW)	Clk (MHz)					
	824	169	234					

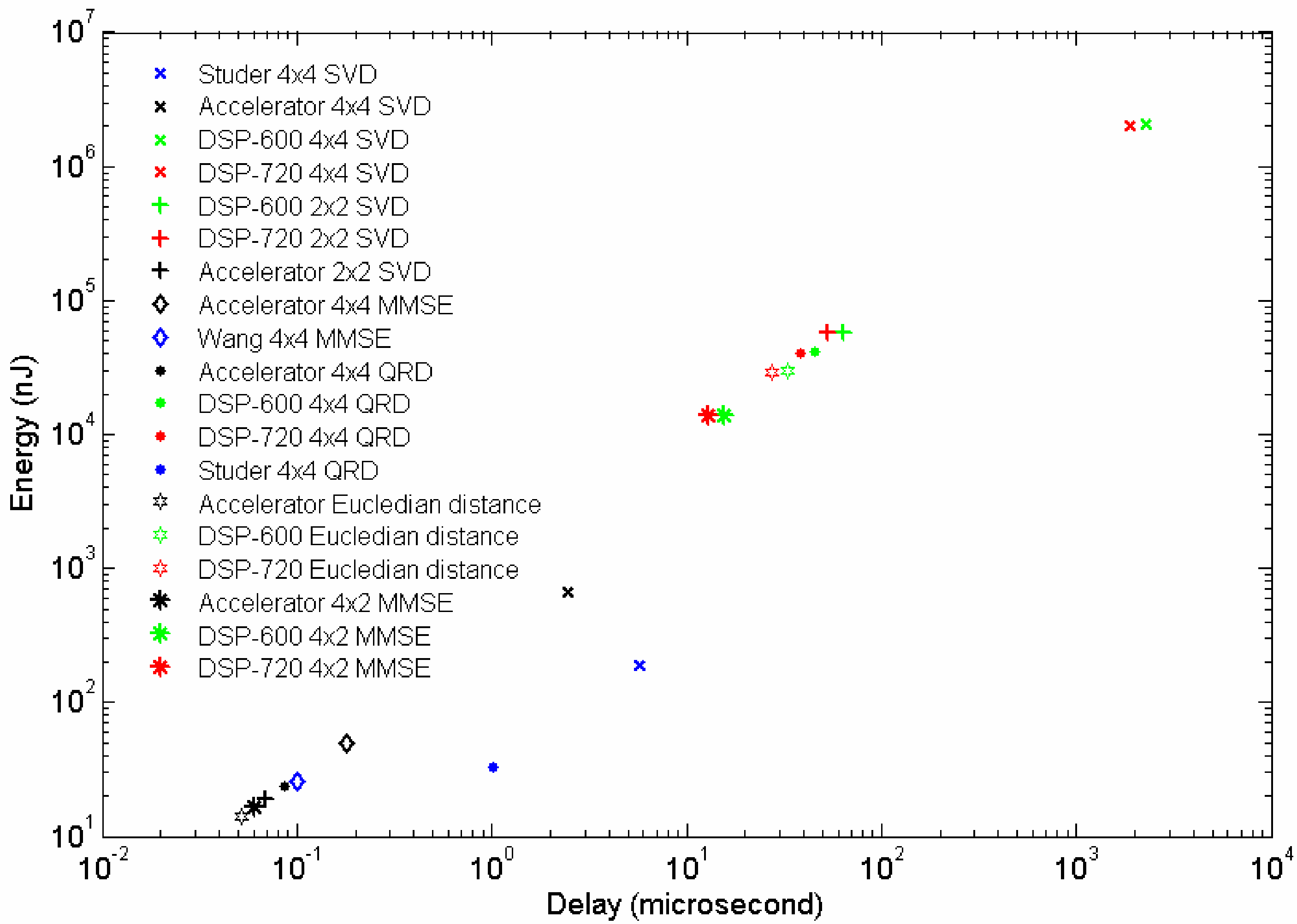


Slice count breakdown V4LX200



Gate count breakdown 65nm TSMC

Location in the performance-flexibility spectrum



THANK YOU