Extended Burn-in for V_{th} variation reduction using NBTI

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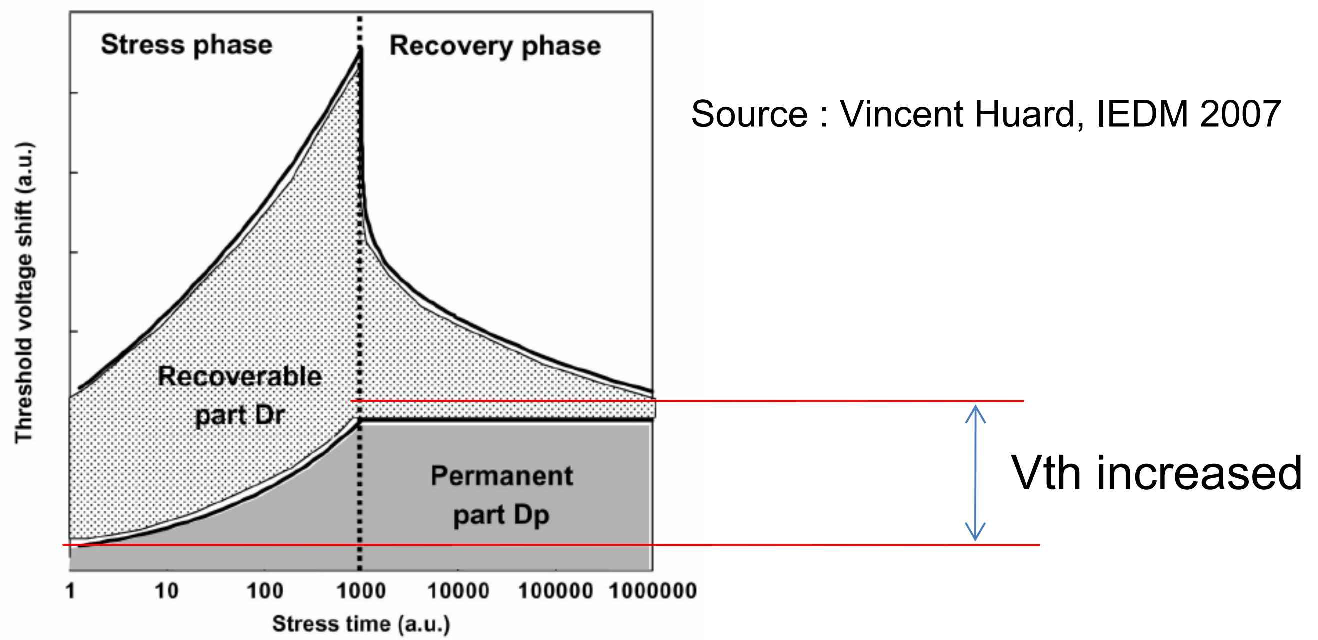
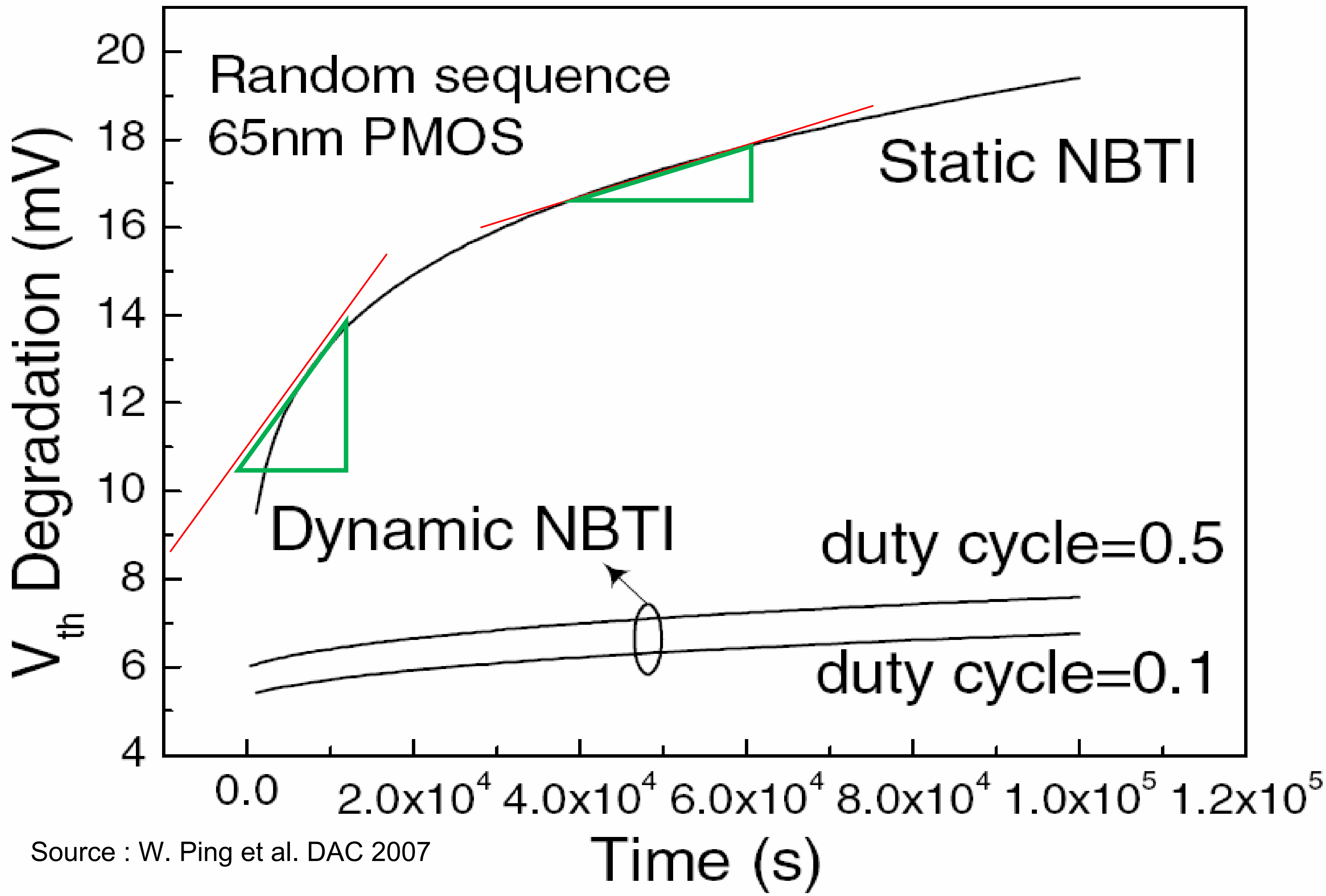
What is NBTI ?

- NBTI : Negative Bias Temperature Instability
- Vth varies on PMOS device
  - Vth increases with negative bias, Vgs=-Vdd
  - But recovers with zero bias ,   Vgs=0



Source : Vincent Huard, IEDM 2007

Time dependence



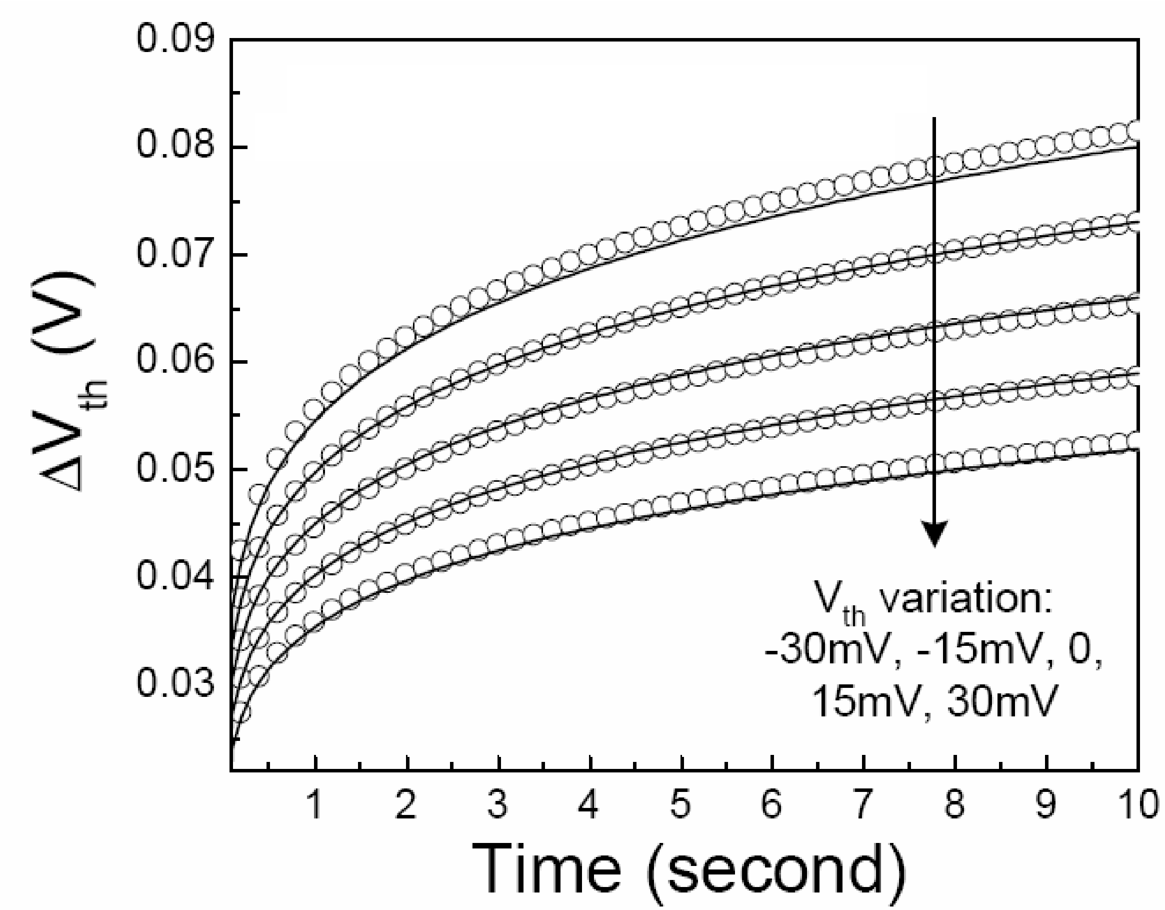
Source : W. Ping et al. DAC 2007

NBTI threats

- Δ Vth-NBTI ↑ as CMOS scales →
  - Circuits reliability ↓
  - Circuits lifetime ↓

- Krishnan, IEDM 2003
  - 10% Idsat to 5% RO frequency degradation
- Pagaduan, IRPS 2000
  - FPGA performance degradation due to NBTI
  - Propagation delay 2.5%
- Neeraj, IEDM 2005
  - Degradation depends on configuration and application.
  - V_{error} > 7 mV (maximum allowed error=7.8mV) for a 64 bit DAC.
- J.C. Lin, IEDM 2006
  - SRAM read margin decrease as a result of NBTI stress.
  - Limit NBTI impact using a less “read margin” dominant design.

Observations



Source : W. Ping et al. DAC 2007

ΔVth process ≡ ΔVth NBTI

ΔVth process + ΔVth NBTI

=> Overall process variation reduced

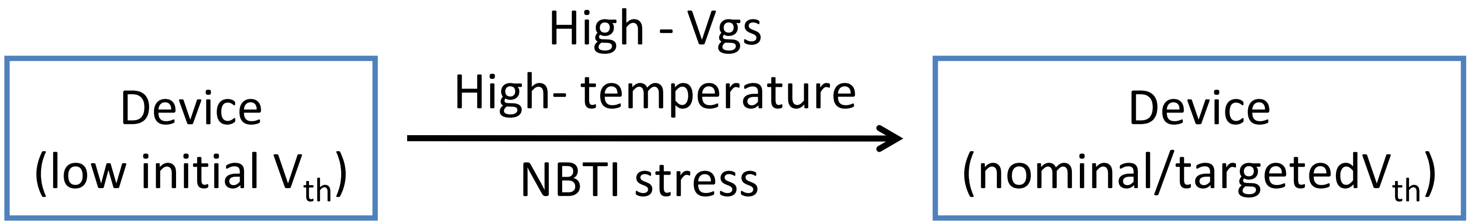
Opportunity

- ΔVth is 40% at 2009 and increasing (ITRS).
- ΔVth can be reduced by an intentional NBTI stress

Table DESN9a Design for Manufacturability Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
Normalized mask cost from public and IDM data	1.0	1.3	1.7	2.3	3.0	3.9	5.1	6.6	8.7
% V_{dd} variability: % variability seen in on-chip circuits	10%	10%	10%	10%	10%	10%	10%	10%	10%
% V_{th} variability: doping variability impact on V_{th}, (minimum size devices, memory)	31%	35%	40%	40%	40%	58%	58%	81%	81%
% V_{th} variability: includes all sources	33%	37%	42%	42%	42%	58%	58%	81%	81%
% V_{th} variability: typical size logic devices, all sources	16%	18%	20%	20%	20%	26%	26%	36%	36%
% CD variability	12%	12%	12%	12%	12%	12%	12%	12%	12%
% circuit performance variability circuit comprising gates and wires	46%	48%	49%	51%	60%	63%	63%	63%	63%
% circuit total power variability circuit comprising gates and wires	56%	57%	63%	68%	72%	76%	80%	84%	88%
% circuit leakage power variability circuit comprising gates and wires	124%	143%	186%	229%	255%	281%	287%	294%	331%

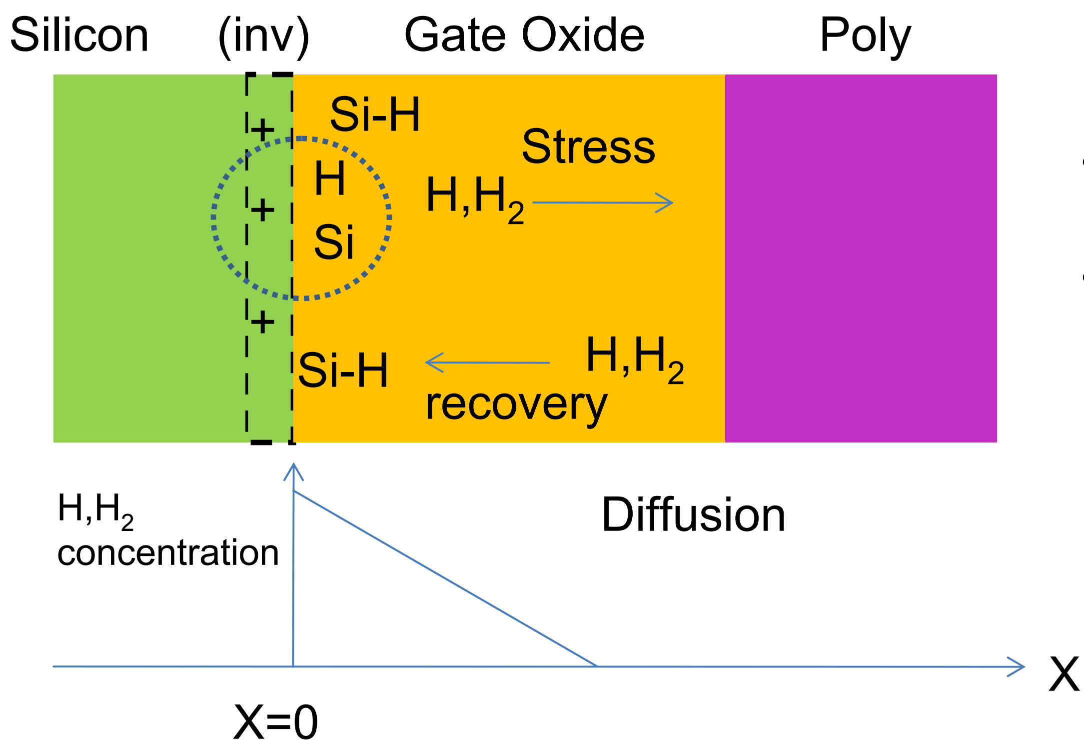
Proposed Burn-in flow



- Difference between targeted Vth and initial Vth provides “room” for NBTI stress.
- Lowering initial Vth may lead to higher initial Vth variation.
- Burn-in process and initial Vth has to be design carefully for optimum results.

Reaction-diffusion model

- Interface traps generated when device is stressed (negative bias)



- H^+ + O-Si in bulk oxide
- Lost of H^+ cause recovery <100%

Model Formulation

$$\frac{dN_{IT}}{dt} = k_F(N_o - N_{IT})P - k_R N_H N_{IT}$$

Reaction

$$\frac{dN_H}{dt} = D_H \frac{d^2 N_H}{dx^2}$$

Diffusion

Stress:

$$\Delta V_{th}(t) = \left(K_v(t-t_0)^{1/2} + \sqrt[2n]{\Delta V_{th}(t_0)}\right)^{2n}$$

Recovery:

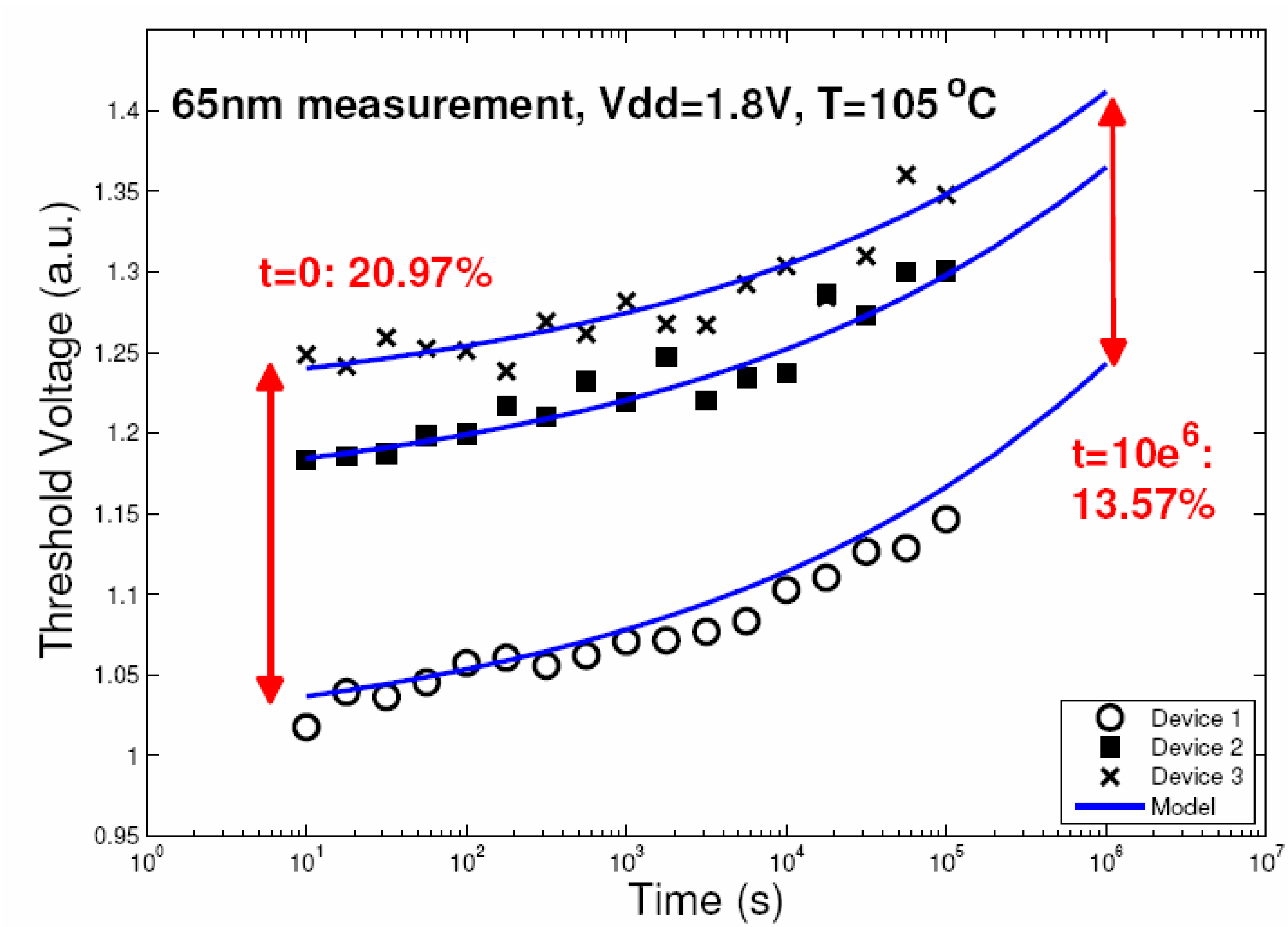
$$\Delta V_{th}(t) = \Delta V_{th}(t_1)\left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(t-t_1)}}{(1+\delta)t_{ox} + \sqrt{Ct}}\right)$$

Source : W. Ping et al. DAC 2007

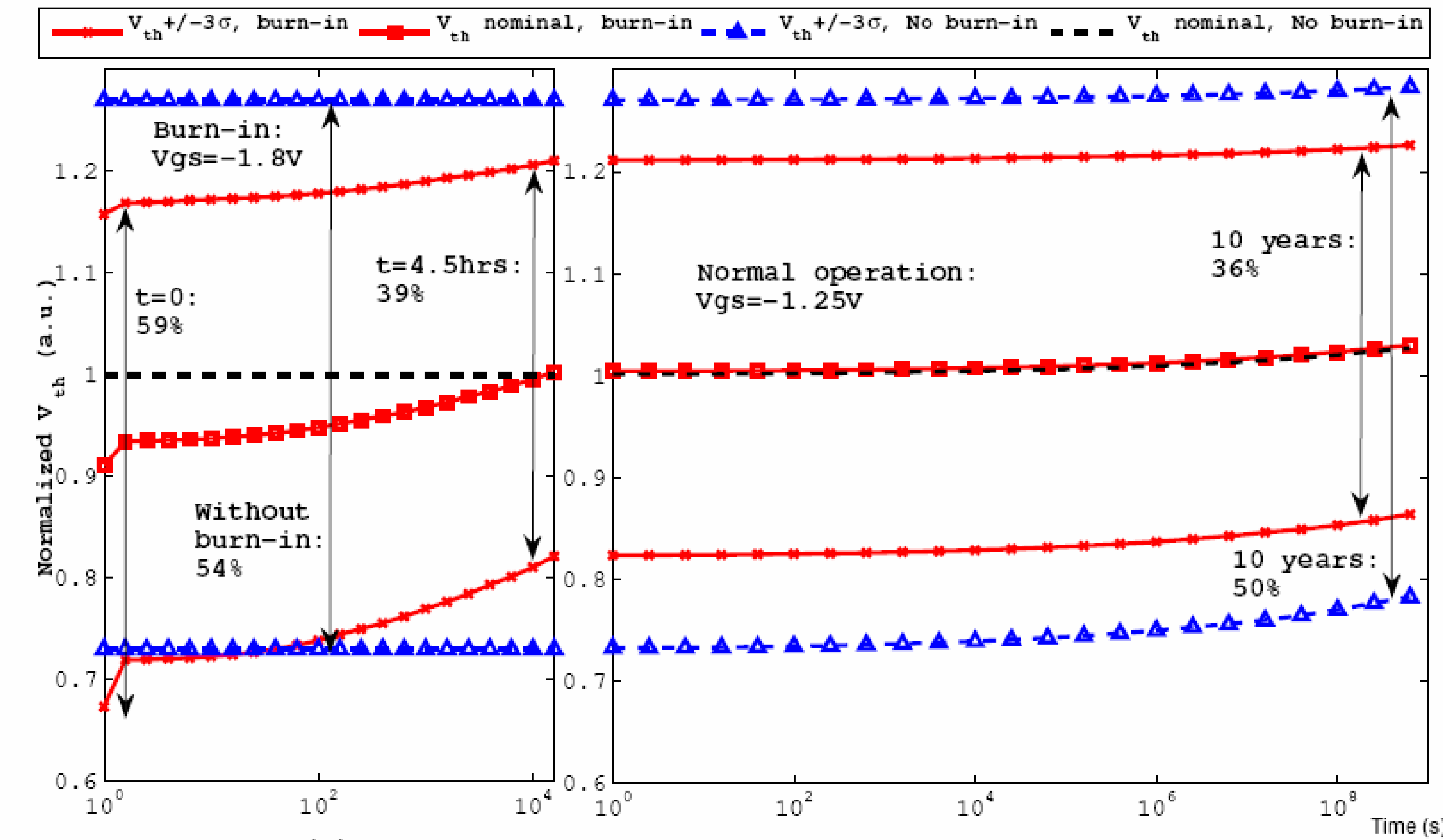
Combine both stress and recovery :

$$\Delta V_{th-nbti} = [\frac{(V_{gs} - V_{th})K_1 * e^{K_2(V_{gs}-V_{th})}}{1-\beta_t}]^{1/3}, \beta_t = 1 - \frac{K_3}{K_4 + K_5 t}$$

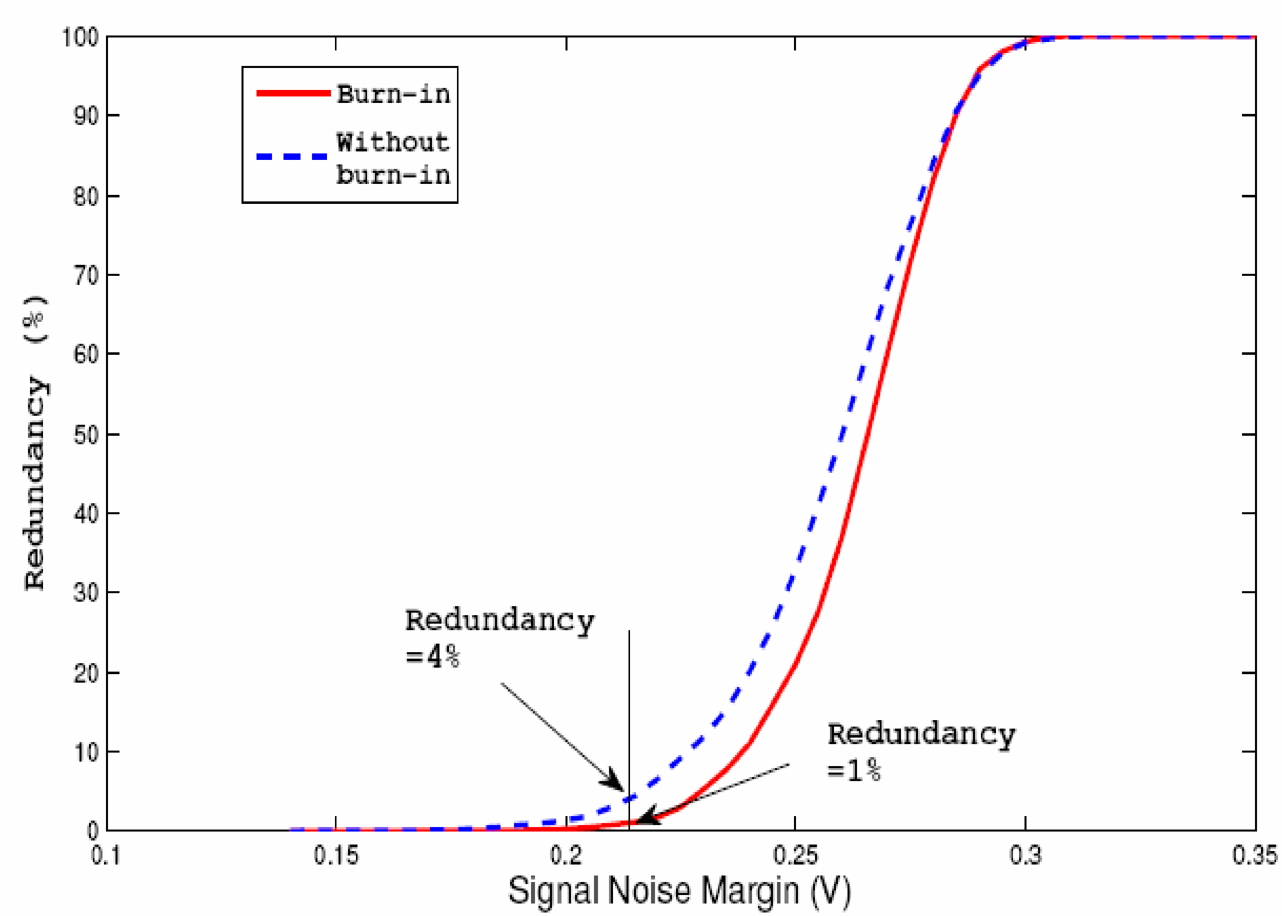
“Burn-in” with negative bias



PMOS burn-in under high DC stress



Case study 1



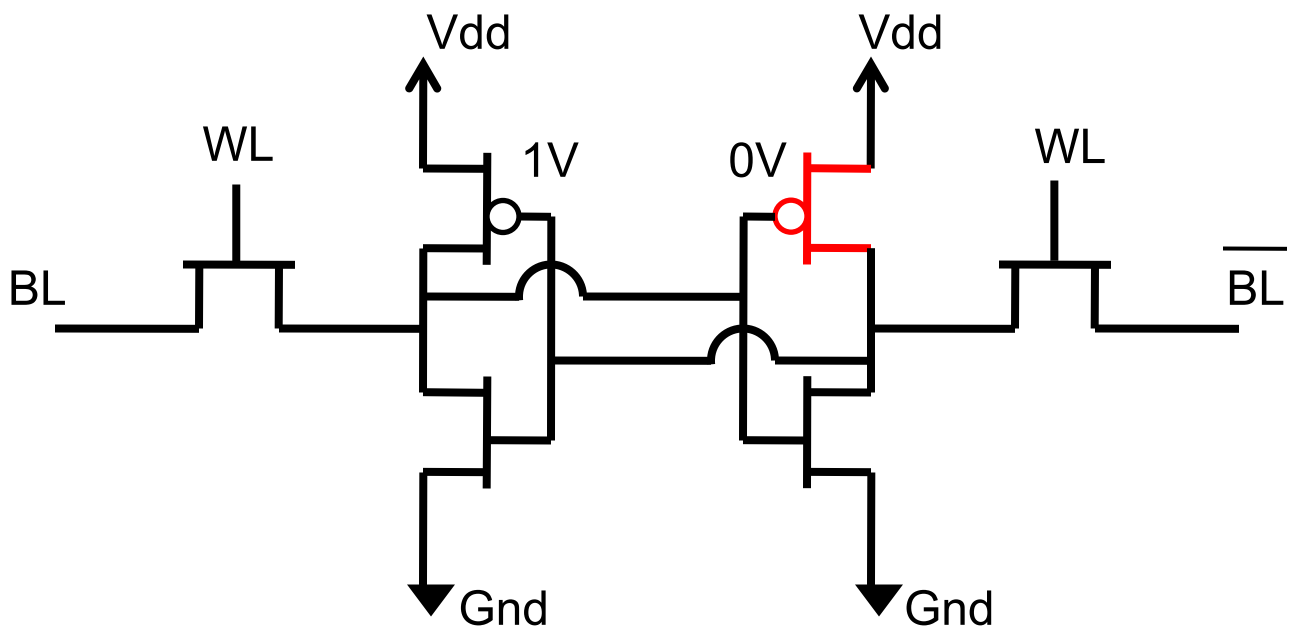
SPICE Monte Carlo simulation on 6T SRAM .

3000 samples,

NMOS
ΔVth=27%

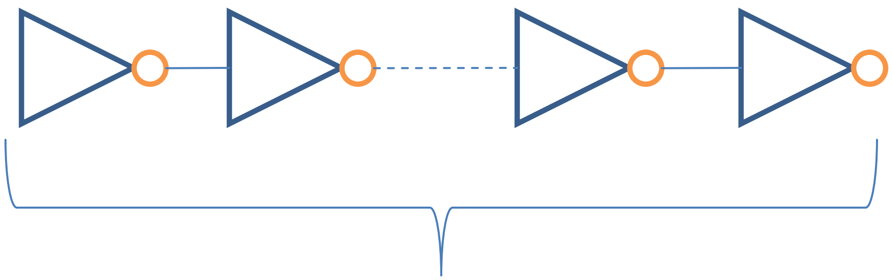
PMOS
ΔVth=27% (initial)
ΔVth=17% (4.5 hours burn-in)

Burn-in example



- Data bit =0 "stress" PMOS on right
- Data bit =1 "stress" PMOS on left
- Flipping data bit frequently : NBTI on both sides
- Lower V_{th} device will degrade faster => V_{th} mismatch reduced

Case study 2



11 stages inverter chain

SPICE Monte Carlo simulation results (3000 samples)

	Without burn-in	NBTI burn-in
Mean Delay (ps)	154.7	154.6
Delay variation (ps)	10.3	8.1

Summary

- NBTI induce parametric shift, threaten circuit reliability and lifetime.
- 4.5 hours burn-in reduces V_{th} variation from 27% (initial) => 17% (after burn-in)

On going work

- Generation of input vectors to bias internal PMOS in digital circuits.
- Analog circuit case study – “burn-in” to reduce design effort on battling V_{th} mismatch.
- Proof-of-concept silicon data.