Fault-Tolerant Logic Syntehsis for Field Programmable Gate Arrays (FPGAs)

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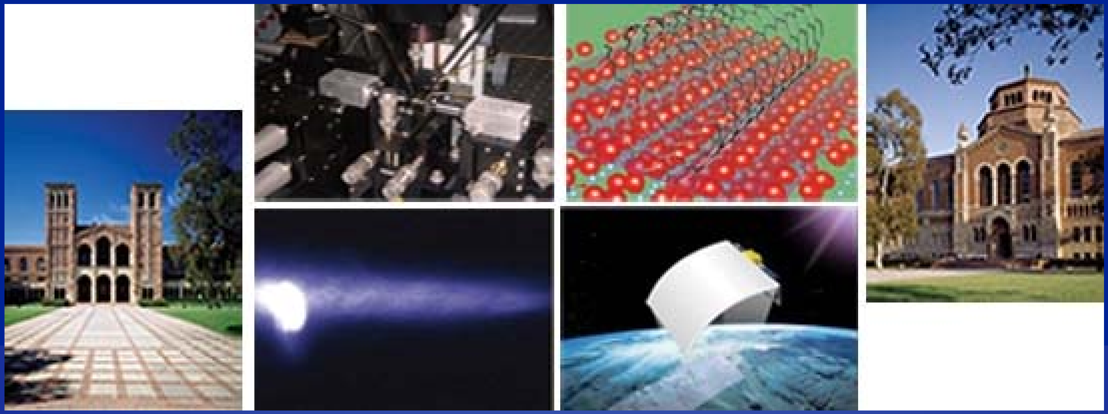


Address comments to lhe@ee.ucla.edu

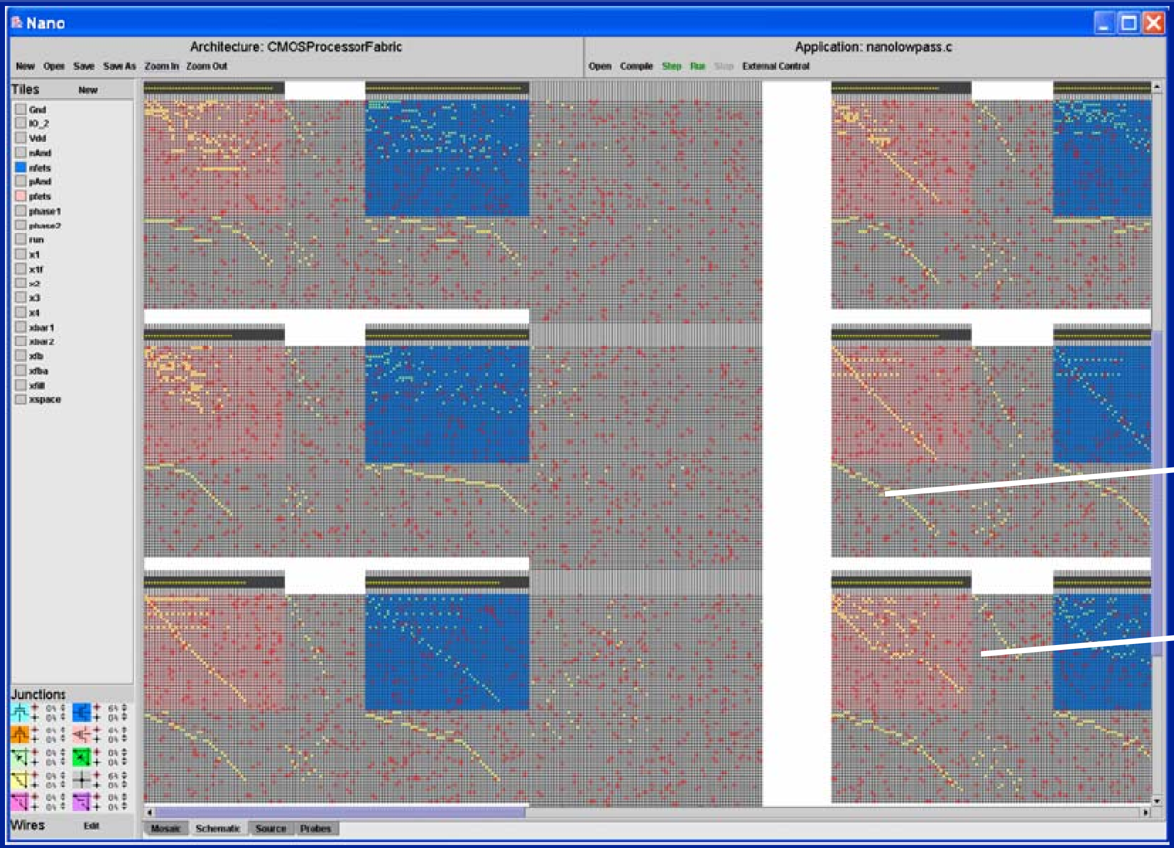
Outline

- **Background and Motivation**
  - Manufacture defects in Nano devices
  - SER in scaled CMOS

- **Robust Resynthesis Algorithms**
  - Resynthesis using Fault-Tolerant Boolean Matching
  - Resynthesis using Dual-Output LUTs

- **Ongoing Work and Conclusions**

Nano-scale Devices Have High Defect Rate



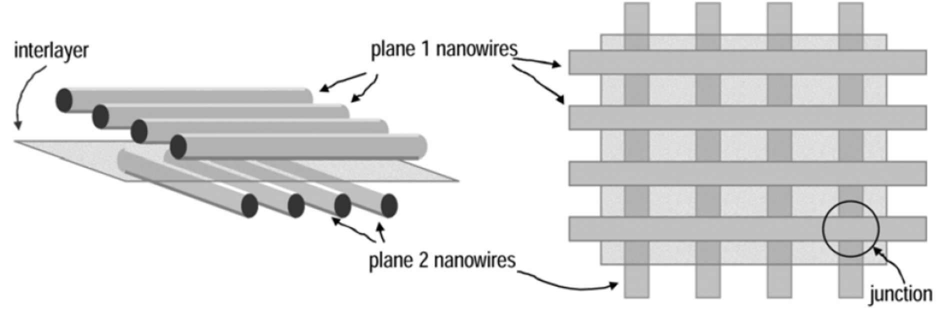
A 4-bit µP mapped to a Nano wire-based crossbar.

Yellow dots: configured junctions

Red dots: defective junctions

- Up to 10% defect rate in Nano wire junctions
  - <10^{-9} defect rate in a 90nm-SRAM bit

(source: Hewlett-Packard Laboratories & ITRS)



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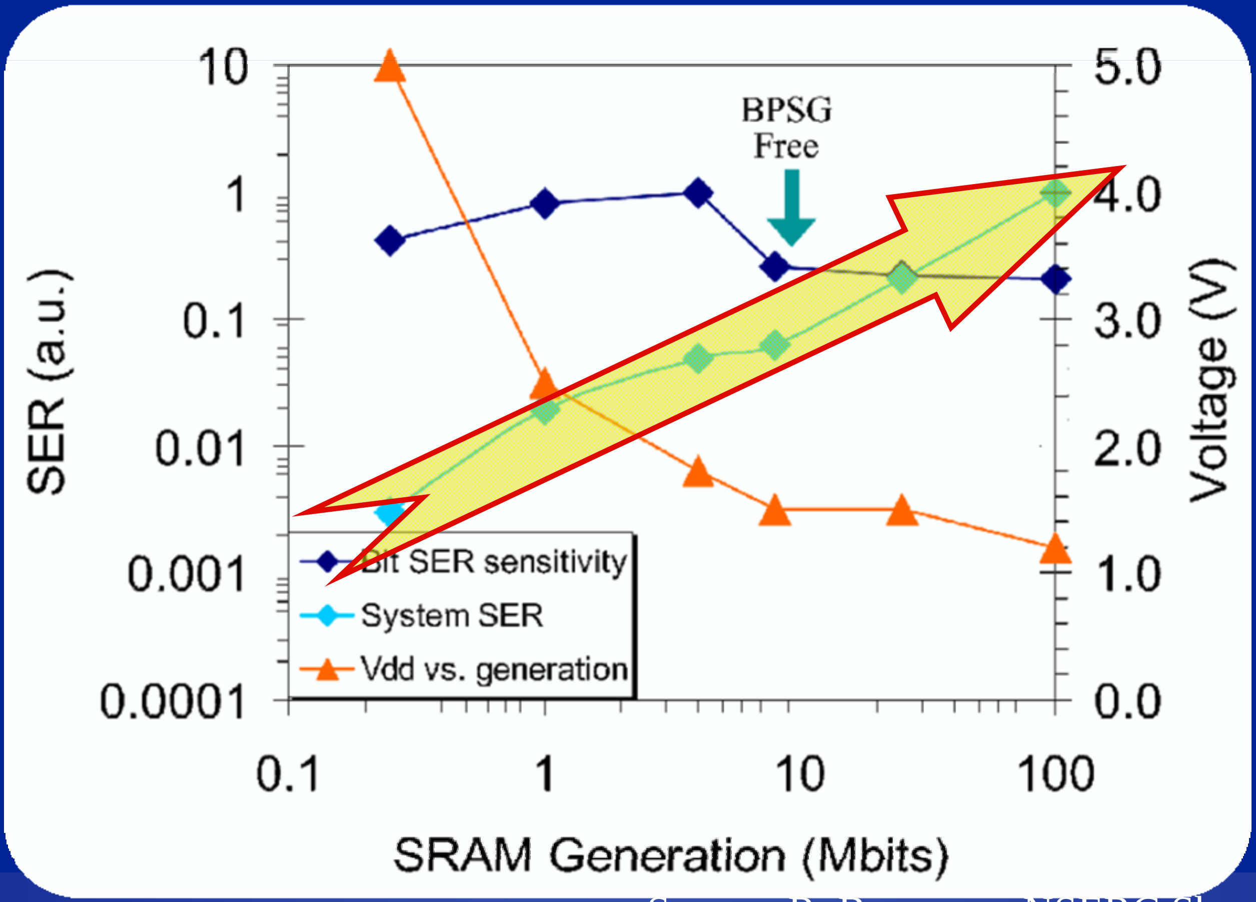
Scaled CMOS Suffers From SER

- **System-level SER keeps increasing**
  - Affects configuration SRAM cells in FPGAs - Permanent SER
  - Affects combinational circuits and registers - Transient SER



Source: R. Baumann, NSERC Short Course, 2005

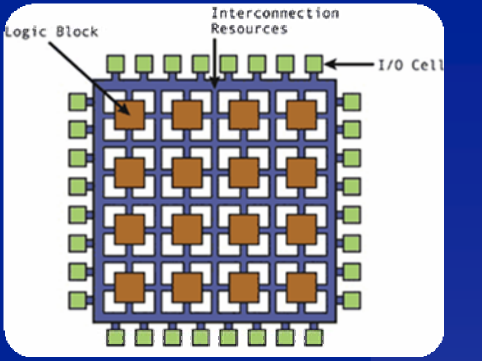
Slide 4

z1

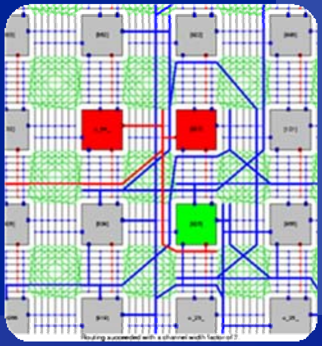
aqua curve for SER

BPSG, is a type of silicate glass, BPSG has been implicated in increasing a device's susceptibility to soft errors
zero, 4/24/2009

Recent SER Mitigation Techniques for FPGAs

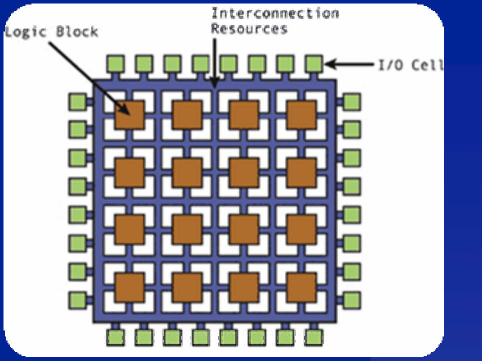


- **Device and architecture co-optimized**
  - Device tuning and FPGA architecture exploration E.g., [ICCAD’07][ISFPGA’08]



- **Physical synthesis:**
  - SEU (MCU) aware FPGA routing E.g., [Bozorgzadeh, DAC’07]

Recent SER Mitigation Techniques for FPGAs



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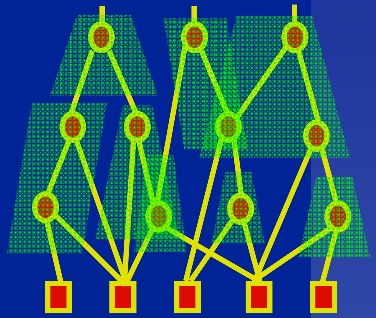
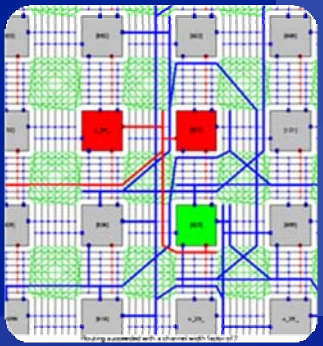


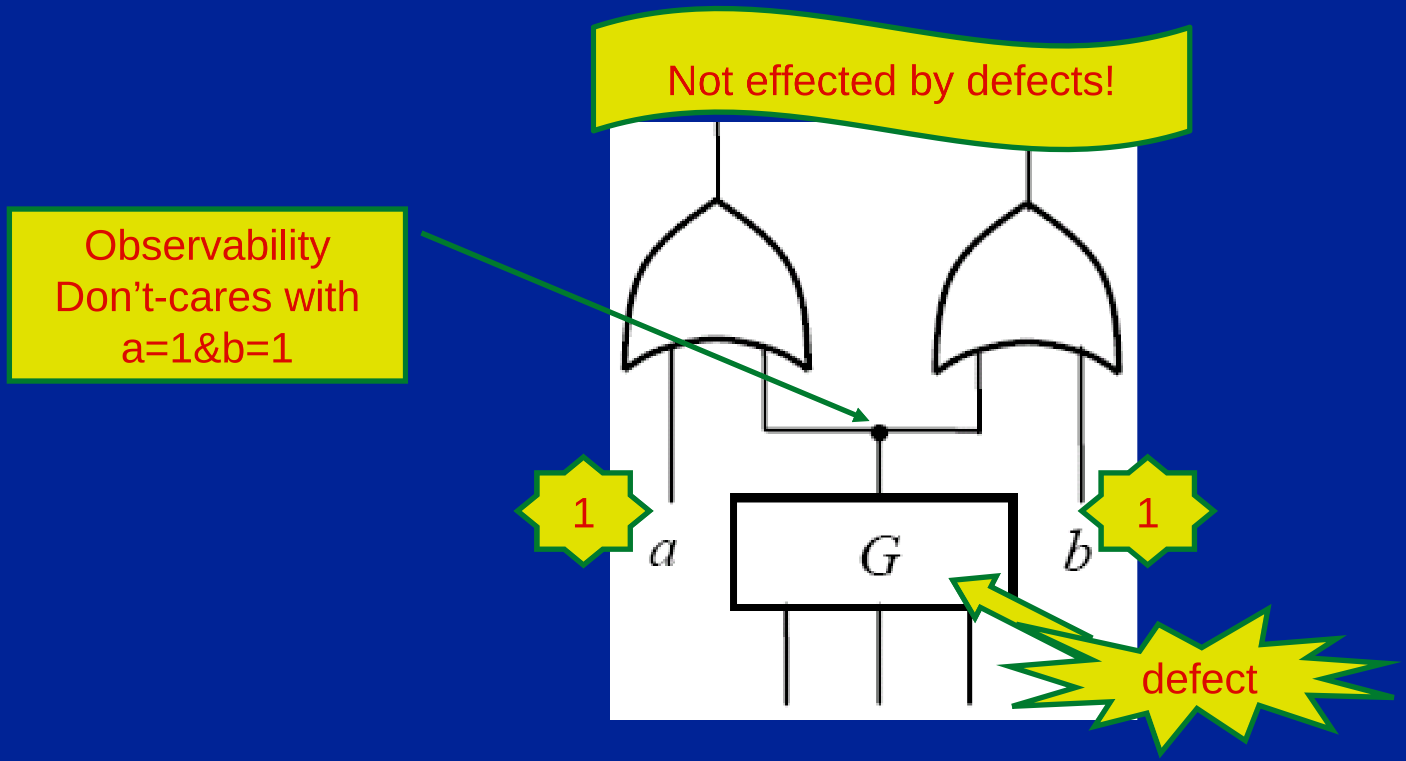
- **Logic synthesis**
  - Stochastic resynthesis [Best paper nomination, ICCAD’08] [SELSE’09]
  - Limited area/power/performance overhead
  - Low testing and synthesis cost



- **Physical synthesis:**
  - SEU (MCU) aware FPGA routing E.g., [Bozorgzadeh, DAC’07]

Key Design Freedom: Logic Masking

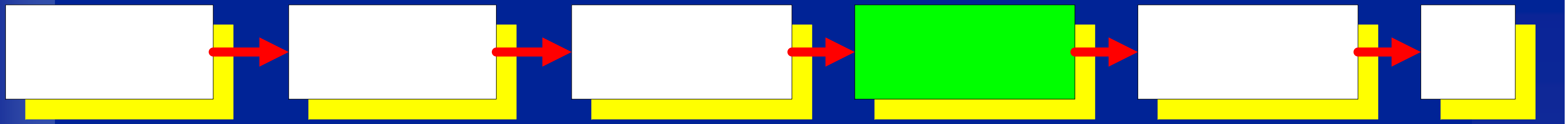
- Defects/SEUs are created equally but not propagated equally
- Stochastic logic synthesis increases MTTF by 30% with negaligible area/delay overhead [ICCAD'08]


Not effected by defects!

Observability Don't-cares with a=1&b=1

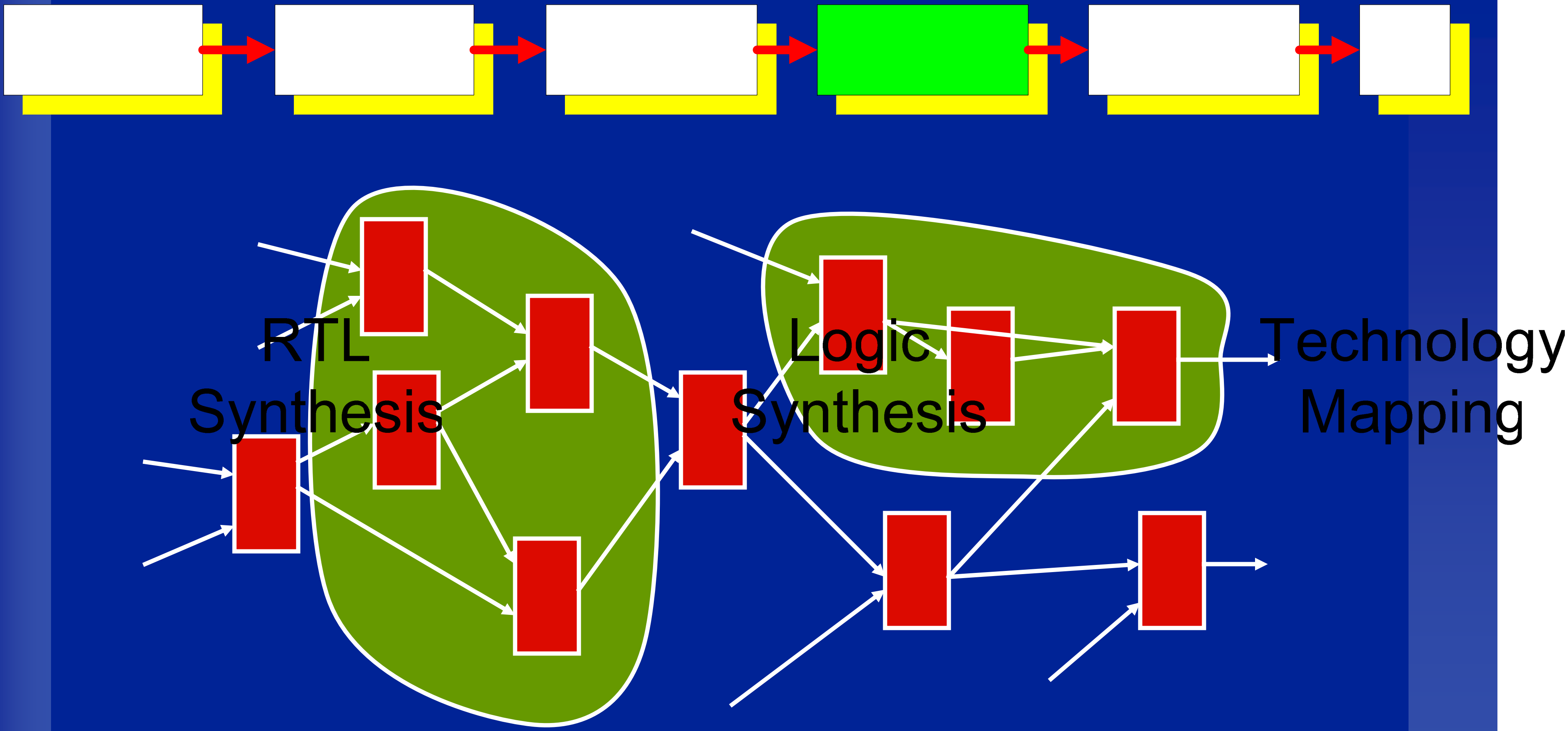
defect

Resynthesis Techniques for Logic Masking



- **Local rewriting** **[Hu, ICCAD'08]**
  - Iterative logic masking insertion by LUT reconfiguration
  - Flexible for various design freedoms
  - Complexity is dominated by the LUT reconfiguration algorithm
- **Global rewriting** **[Lee, SELSE'09]**
  - One-pass approach to achieve global optimum
  - Applicable to limited design freedoms due to runtime complexity

Local Writing-Based Resynthesis



RTL Synthesis

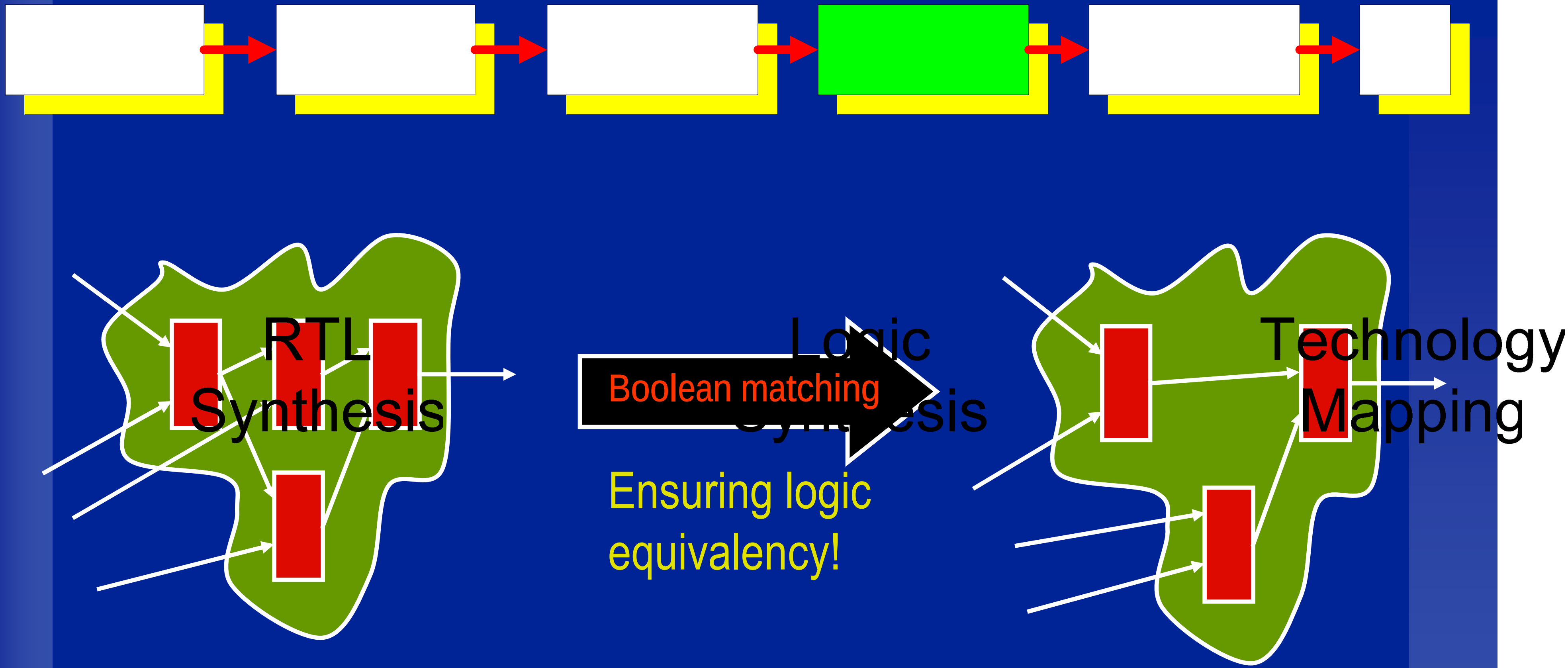
Logic Synthesis

Technology Mapping

- **Multi-iterations of Boolean Matching-based Resynthesis**

(Source: Andrew Ling, University of Toronto, DAC'05)

Boolean Matching in FPGA Resynthesis



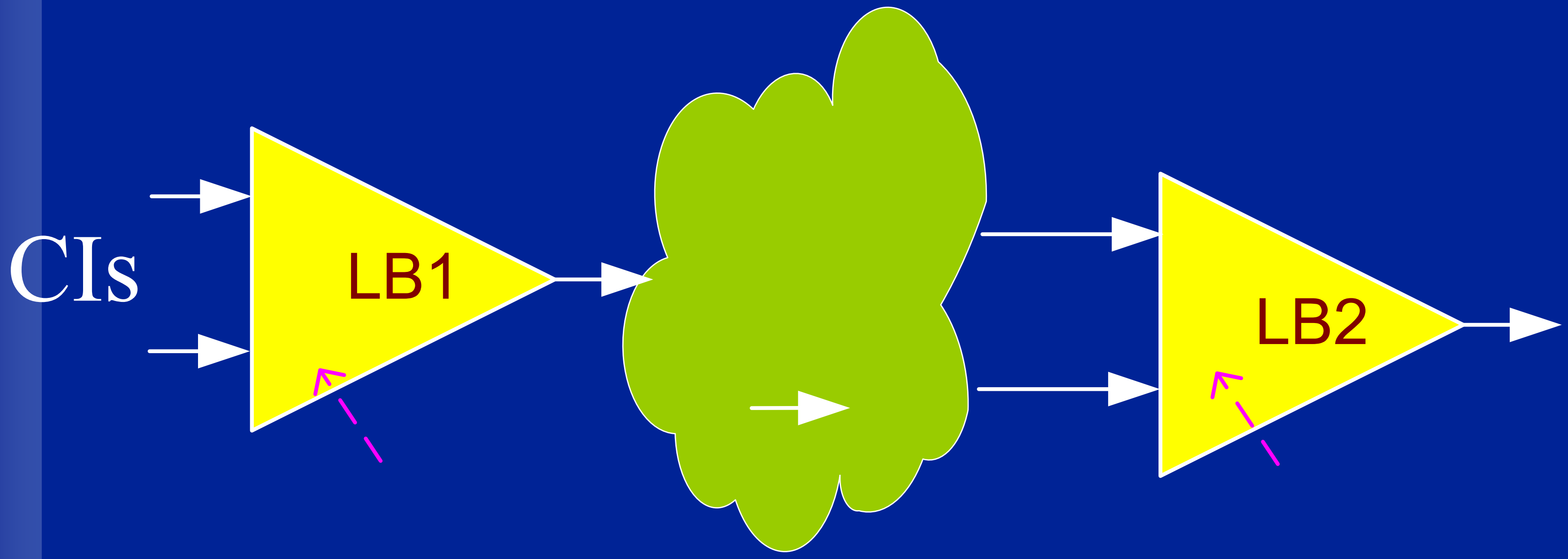
Boolean matching

Ensuring logic equivalency!

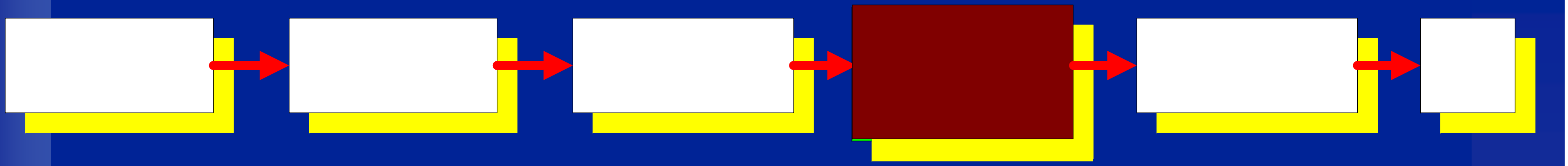
- Attempt to re-map a logic block by Boolean matching

Modeling of Faults

- Model both faults in LUT configurations and the faults in intermediate wires as random variables, whose probabilities are given as inputs of our problem.



ROSE: RObust REsynthesis w/ FTBM



RTL Synthesis

Logic Synthesis

Technology Mapping

- **Fault-Tolerant Boolean Matching**
  - Inputs
    - Programmable Logic Block (PLB) *H* and Boolean function *F*
    - **Fault rates for the inputs and the SRAM bits of the PLB**
  - Outputs
    - Either that *F* cannot be implemented by PLB *H*
    - Or the configuration of *H* **which minimizes the probability that the faults are observable in the output of the PLB under all input vectors.**
  - FTBM tasks breakdown:
    - Step 1: Find a Boolean matching solution
    - Step 2: Evaluation the stochastic fault rate of a solution

FTBM Step1: SAT Encoding

Conjunctive Normal Form (CNF) for
Boolean Satisfiability (SAT) reasoning

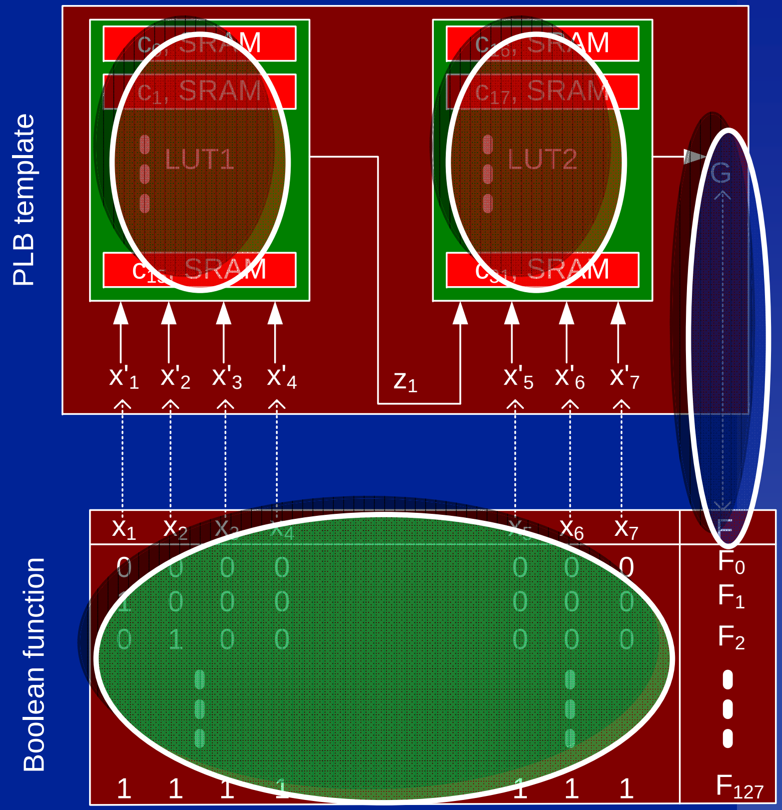
$$\Psi(\mathcal{H}) =$$

$$(\overline{x'_1} \wedge \overline{x'_2} \wedge \overline{x'_3} \wedge \overline{x'_4} \rightarrow (z_1 \leftrightarrow c_0) \wedge \cdots \wedge$$
$$(x'_1 \wedge x'_2 \wedge x'_3 \wedge x'_4 \rightarrow (z_1 \leftrightarrow c_{15})$$

$$\Psi(F) =$$

$$(\overline{x_1} \wedge \overline{x_2} \wedge \cdots \wedge \overline{x_k} \rightarrow F_0) \wedge$$
$$(x_1 \wedge \overline{x_2} \wedge \cdots \wedge \overline{x_k} \rightarrow F_1) \wedge \cdots \wedge$$
$$(x_1 \wedge x_2 \wedge \cdots \wedge x_k \rightarrow F_{2^k-1})$$

$$\underline{\exists c_1 \cdots c_n}\,\underline{\forall x_1 \cdots x_k}\,\exists z_1 \cdots z_m$$
$$\Psi(\mathcal{H}) \wedge \Psi(F) \wedge (\underline{G \leftrightarrow F})$$



- If implementable, multiple configurations might exist
- The one with minimal fault rate is needed!

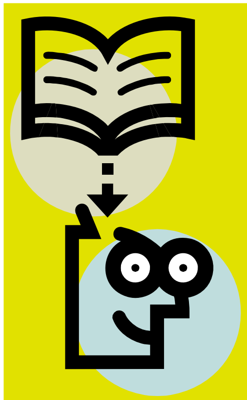
FTBM Step2: Fault Rate Calculation Based on SSAT

- **Simulation-based fault rate calculation**
  - **Not scalable for multiple defects**
- **SAT-based fault rate calculation**
  - **Intelligently modeling random defects**

$$\exists c_1, \cdots, \exists c_n, \Re p_1, \cdots, \Re p_k, \Re d_1, \cdots, \Re d_n, \exists c'_1, \cdots, \exists c'_n$$
$$\forall x_1, \cdots, \forall x_k, \exists x'_1, \cdots, \exists x'_k, \exists z_1 \cdots \exists z_m, \exists G, \exists F$$
$$E\{\Psi(\mathcal{H}) \wedge \Psi(F) \wedge (G \leftrightarrow F) \wedge$$
$$\bigwedge_{i=1,\cdots,n} d_i \leftrightarrow (c'_i \neq c_i) \wedge \bigwedge_{i=1,\cdots,k} p_i \leftrightarrow (x'_i \neq x_i)\} \geq \beta$$

$p_i \leftrightarrow (x'_i \neq x_i)$ Faults in intermediate wires

$d_i \leftrightarrow (c'_i \neq c_i)$ Faults in LUT configurations



Deterministic SAT vs. SSAT

Deterministic SAT

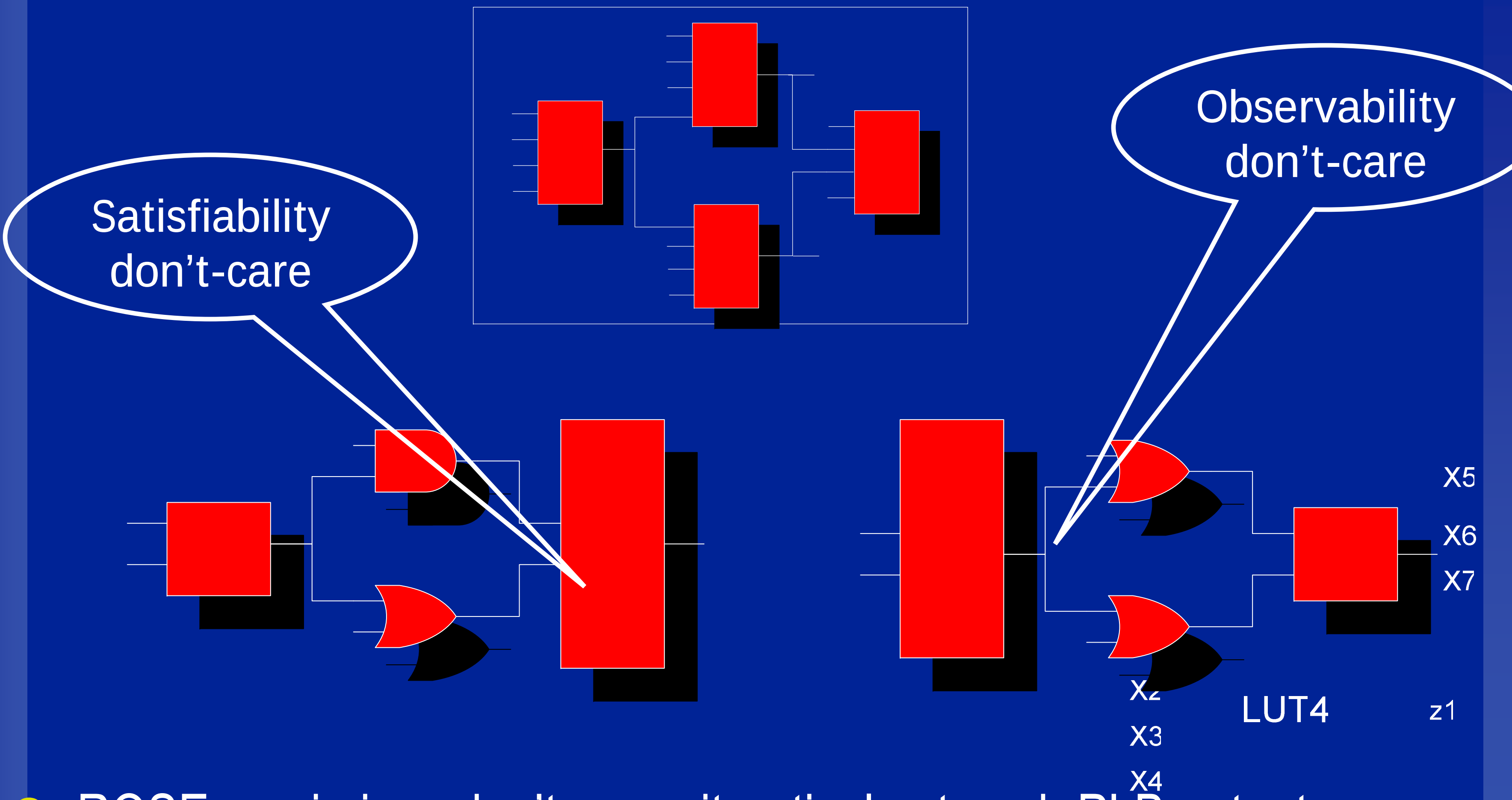
$$\exists x_1, \ldots, \exists x_n . (\varphi(x_1, \ldots, x_n) = 1)$$

Stochastic SAT

$$\exists x_1, \reflectbox{R} x_2, \ldots, \exists x_{n-1}, \reflectbox{R} x_n$$
$$(E\varphi(x_1, \ldots, x_n) \geq \beta)$$

PLB Structure for Fault-Tolerant Resynthesis

- Robust PLB structure introduces more potential of don’t-cares



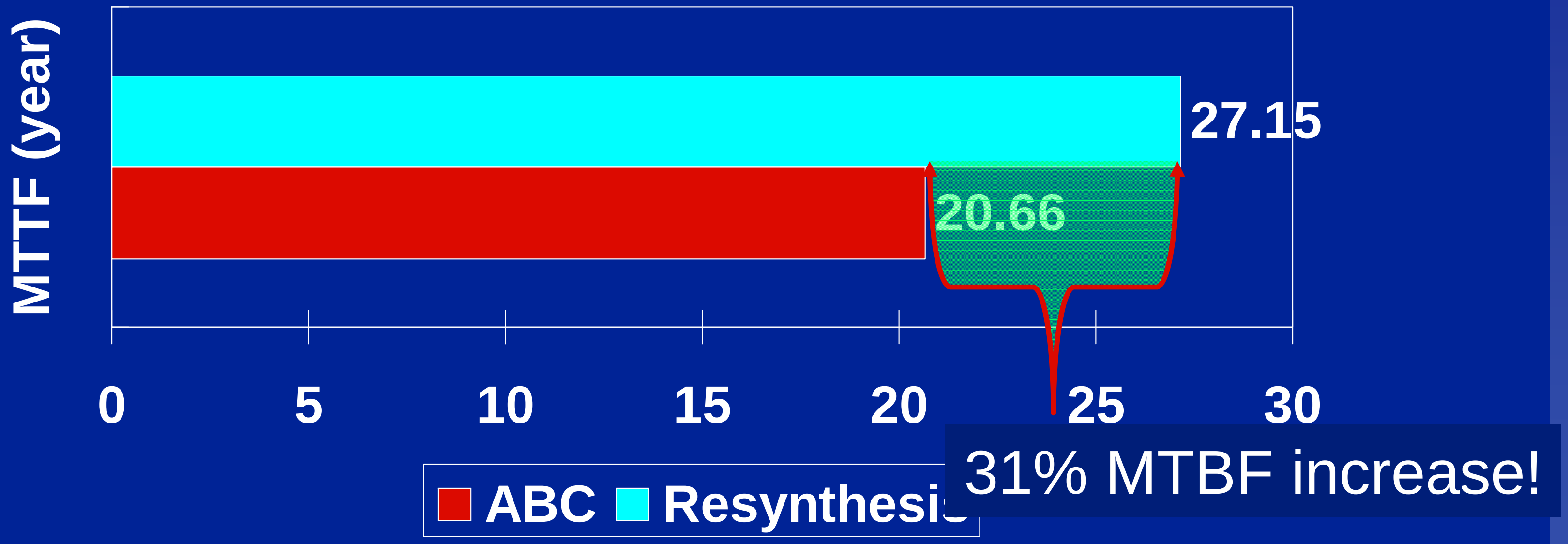
Satisfiability don’t-care

Observability don’t-care

- ROSE maximizes don’t-cares iteratively at each PLB output

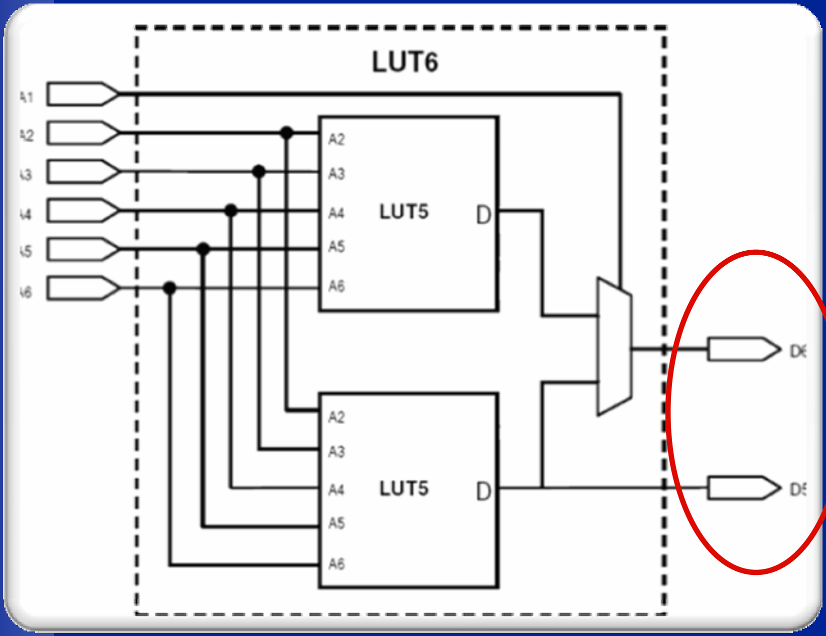
Estimation of Mean Time To Failure

- SER modeling: [Mukherjee, HPCA, 2005]
- Assume max-size FPGA: 330,000 LUTs

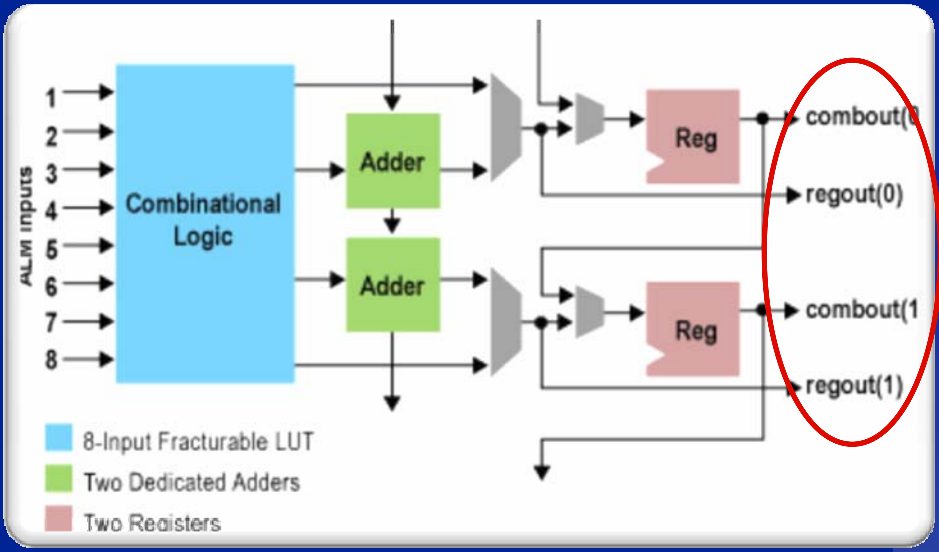


31% MTBF increase!

More Opportunities in Modern FPGAs



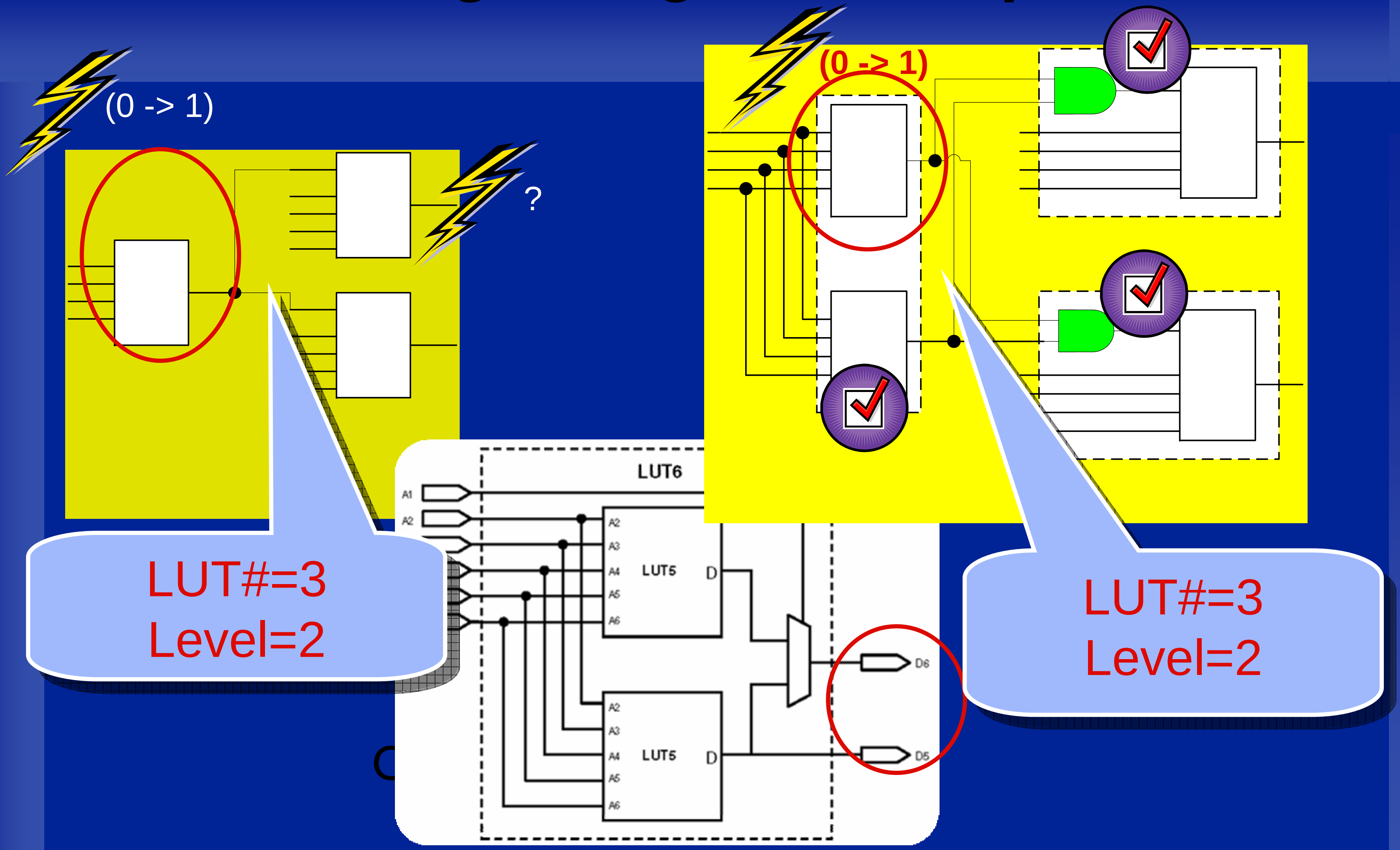
Xilinx Virtex-5 LUT



Altera Stratix III ALM

- **Dual-output LUT**
  - Merging two small LUTs into one dual-output LUT
  - Originally designed to increase the logic density

Fault Masking Using Dual-Output LUTs



LUT#=3
Level=2

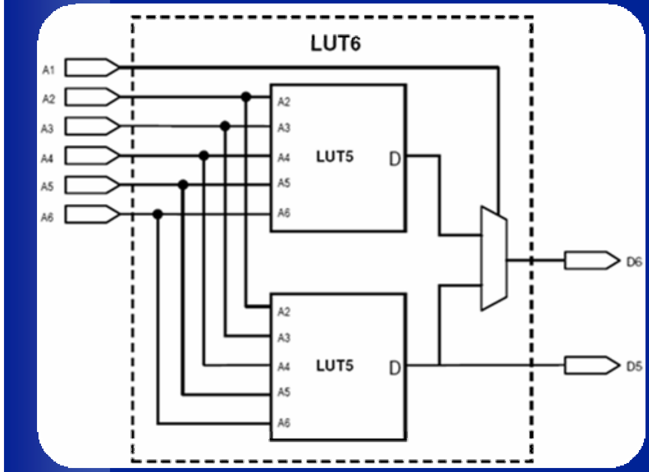
LUT#=3
Level=2

Xilinx Virtex-5 dual-output LUT

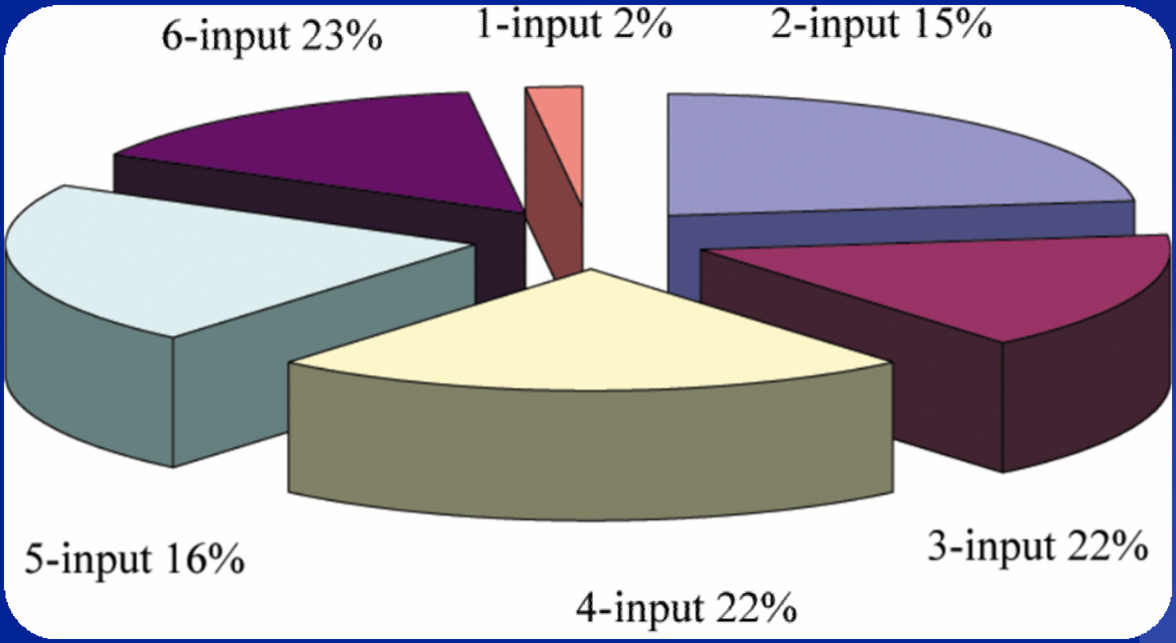
- **One spare pin is needed for duplication and encoding, respectively**

Potential of the Optimization Using Dual-Output LUTs

Xilinx Virtex-5 LUT architecture

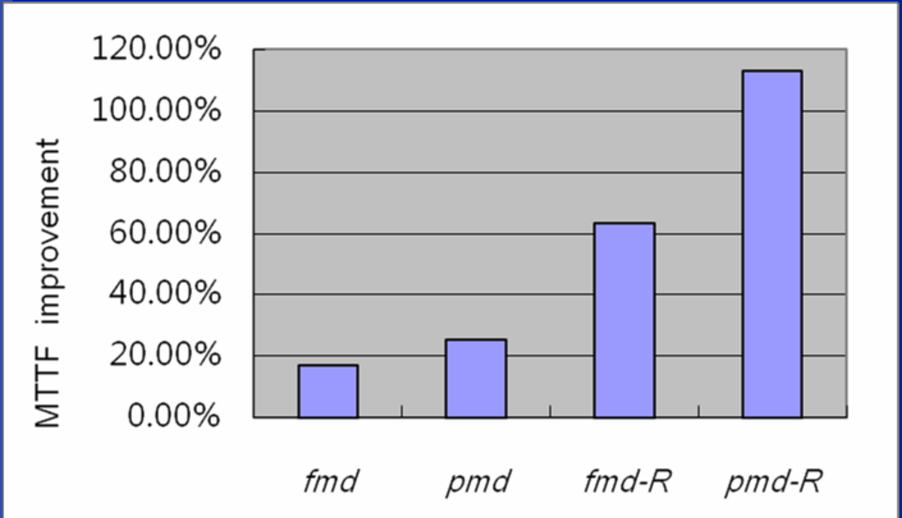


Pin utilization rate for Xilinx Virtex-5 applications

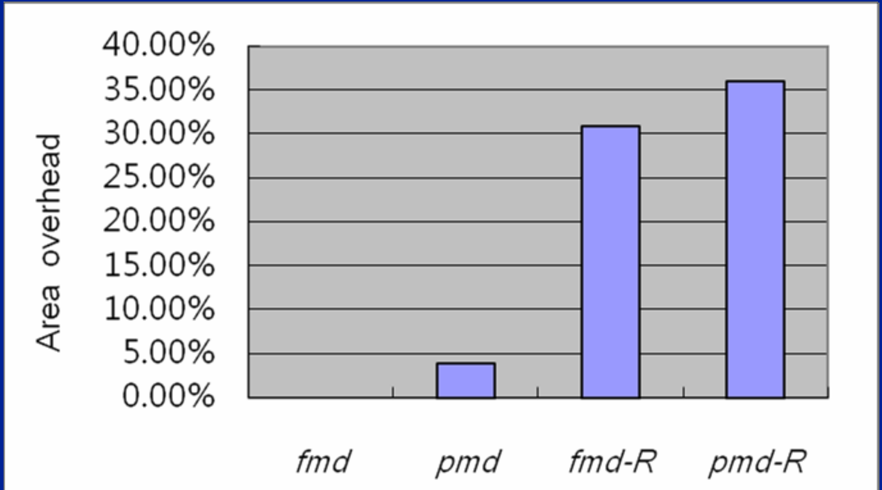


- **Pin utilization rate is low with state-of-art logic synthesis**

Preliminary Results for FT w/ Dual-Output LUTs

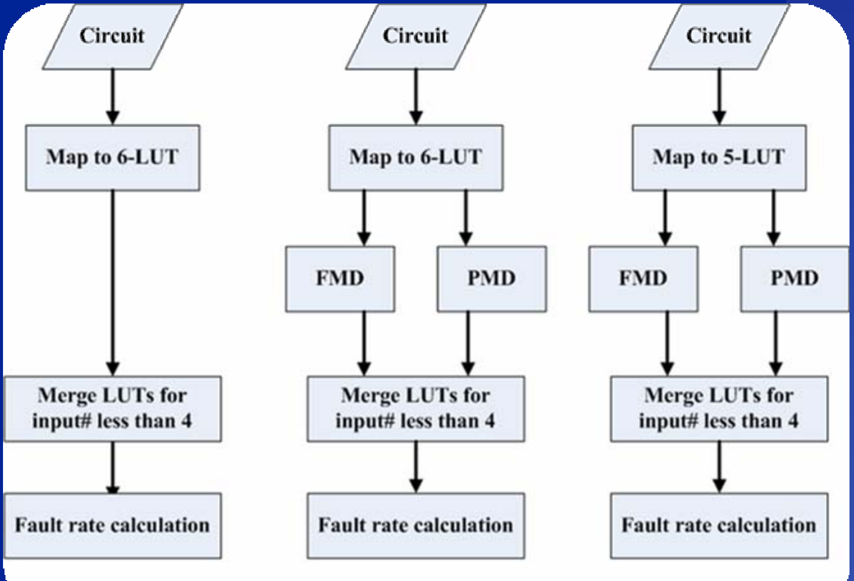


(A) MTTF improvement(combinational)



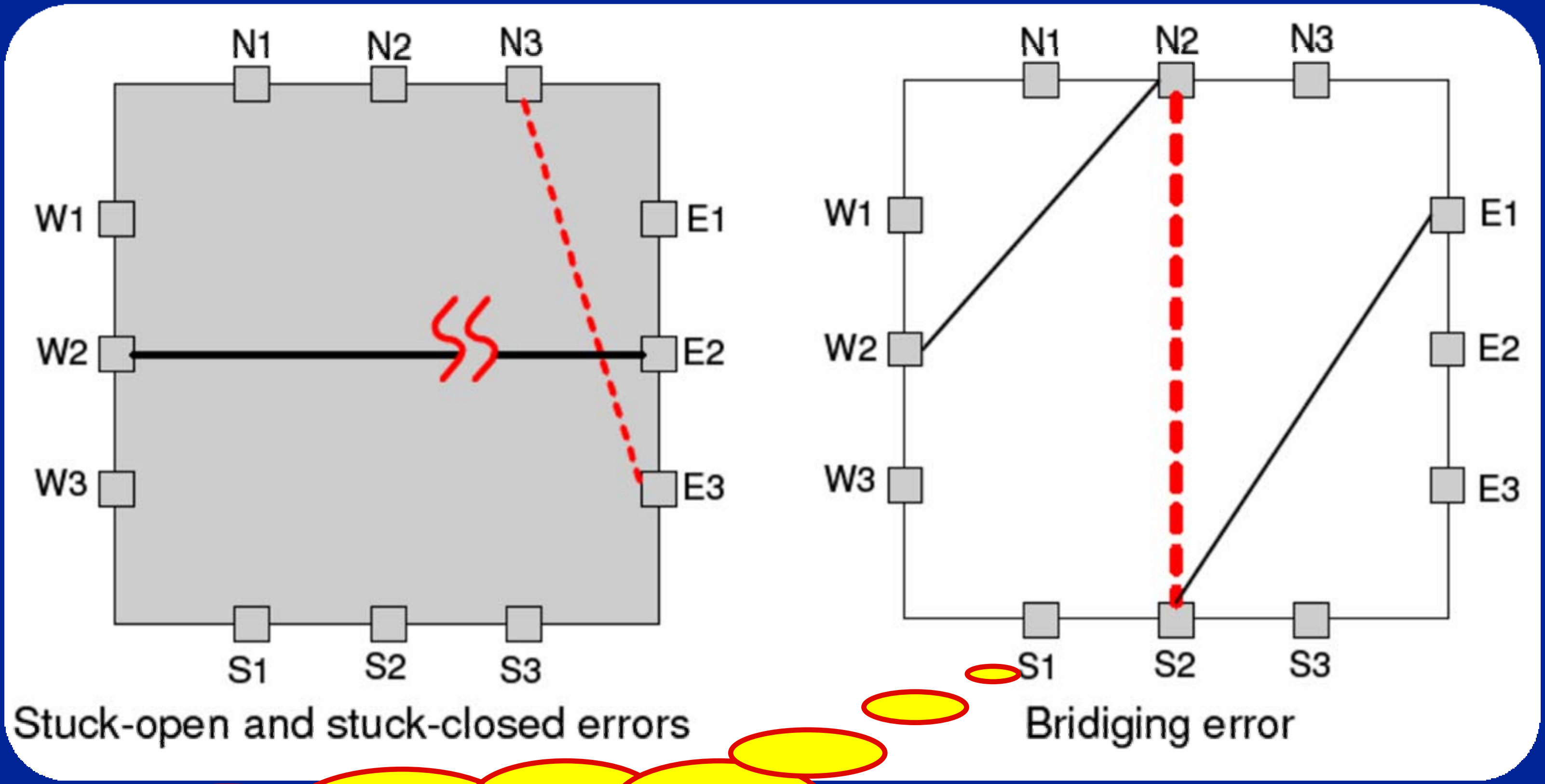
(A) Area overhead(combinational)

Front-end synthesizer: ABC
Benchmark set: MCNC
Architecture: 6-LUTs



(A) base (B) FMD, PMD (C) FMD-R, PMD-R

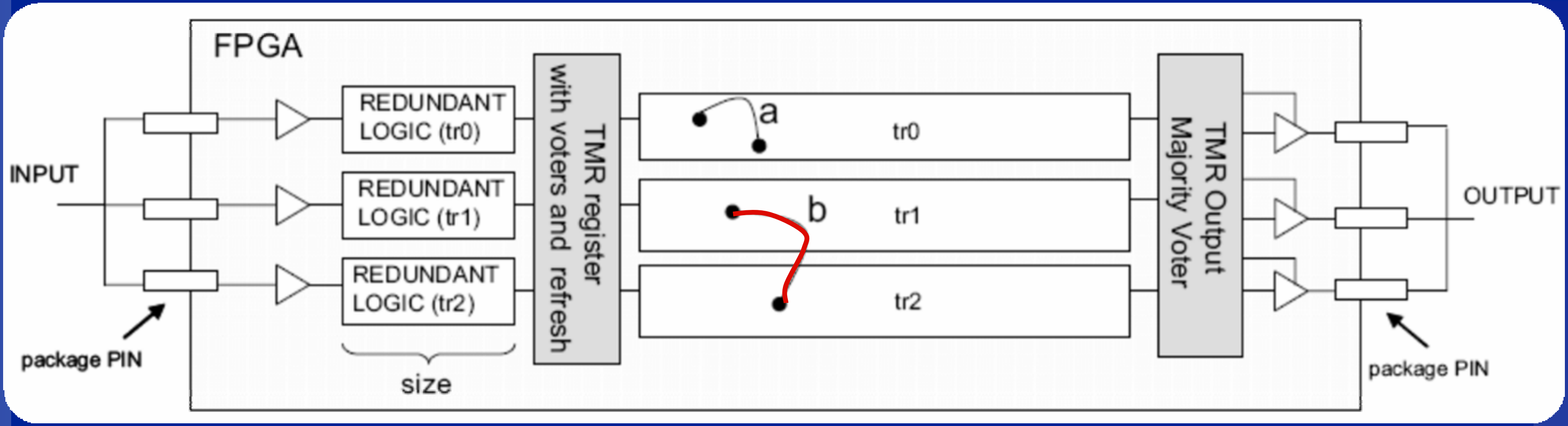
Logic Synthesis Interacting w/ Physical Synthesis: Faults in FPGA Routing

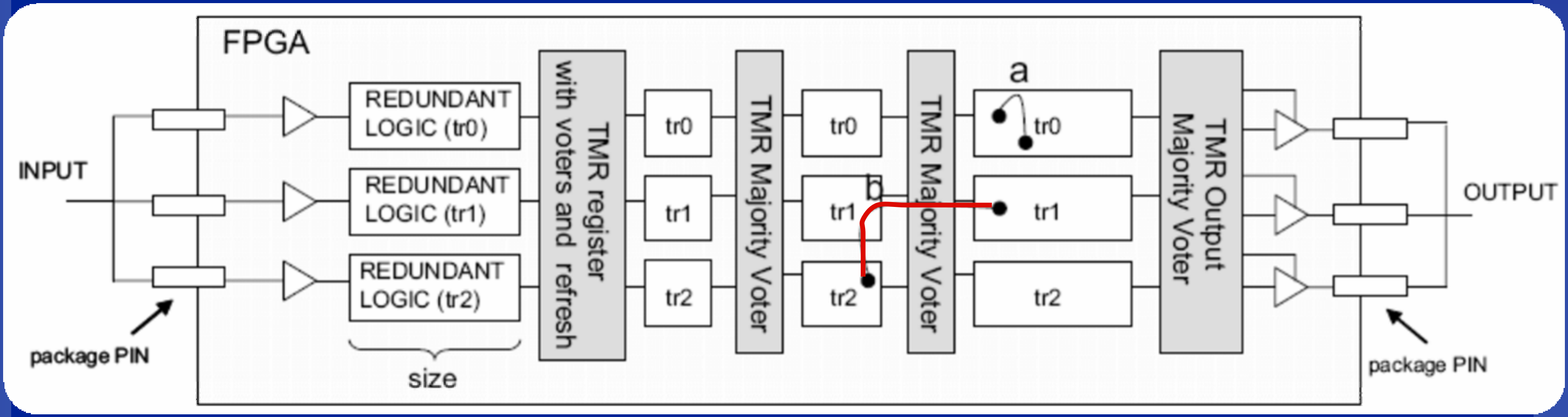


One SEU might result in multiple faults!

(Source: Ghazanfar Asadi, MAPLD'04)

Partial TMR Considering Routing Bridging Faults





(Source: F. Lima Kastensmidt et al, DATE'95)

More Ongoing Research Directions in EDA Group

- **Logic Synthesis w/ more design freedoms**
  - Retiming for Single Event Transient (SET) Mitigation
  - In-Place LUT configuration for design closure
- **Fast Fault simulation using FPGA-based Emulator**
  - Logic synthesis w/ the embedded emulator for large circuit optimization
- **FPGA-based test-bed for system-level vulnerability assessment**
  - System vulnerability stack for microprocessor architecture