Schottky Tunneling Source MOSFET Design for Mixed Mode and Analog Applications

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Outline

- **Background and Motivation**
- **Device Concept**
- **Key Fabrication Steps**
- **Device Measurements**
- **Analog Performance**
- **Conclusion**

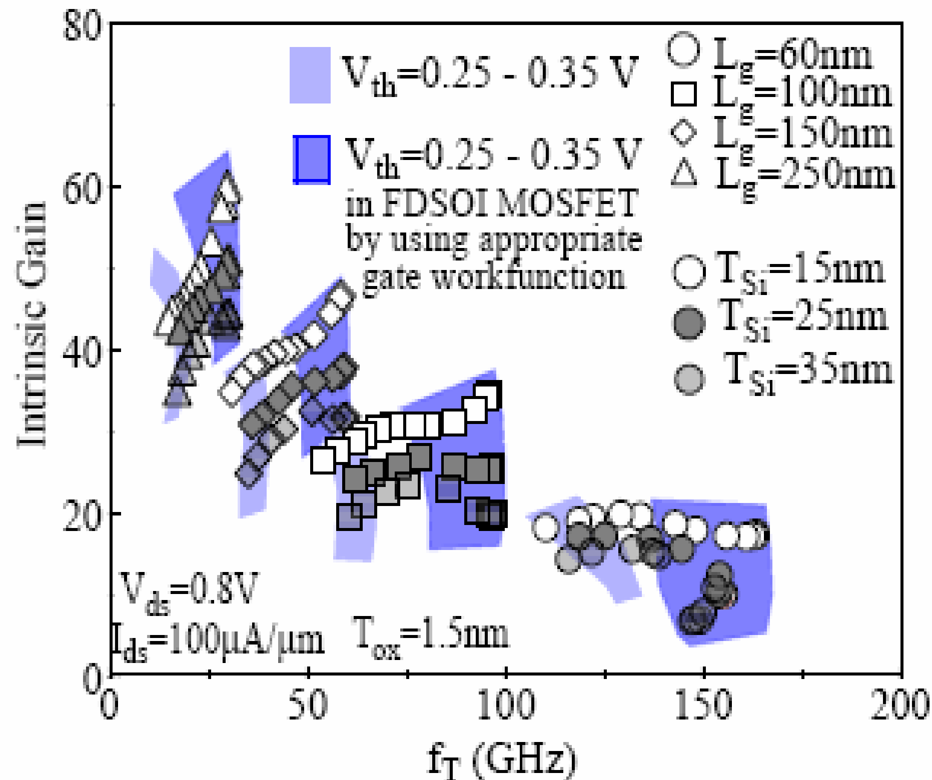
Background

- ➢ CMOS Evolution aims at increasing performance of digital systems ⇨ *Minimizing power, increase speed*
- ➢ High Demand for increasing *communication and mixed mode applications*
- ➢ Mixed signal systems, where analog and digital systems must be realized on the same die *(SOC)*
- ➢ CMOS scaling makes RF applications possible which require f_t > 100GHz
- ➢ Analog Performance suffers due to conflicting requirements ⇨ *Analog design lagging behind digital by more than two generations*

Background

- Analog Circuit Requirements:

High Output Resistance (R_{OUT}), Intrinsic Gain A_V ($g_m x R_{OUT}$), and Cutoff frequency (f_t), linearity, noise and mismatches



S. Suryagandh et al, TED, vol. 51, pp. 1122, 2004.

- SCE degrade R_{OUT} as we scale L_G
- Drastic reduction in Intrinsic Gain ($g_m x R_{OUT}$)
  - conv. 90nm: A_V ~ 10
- Increasingly difficult to achieve both high gain and high f_t,

Motivation

- In order to continue scaling of transistors in analog circuits, *alternate structures must be explored*

- These alternate structures must be optimized for both analog and digital performance ⇨ *conducive to SOC applications*

- One such structure is the *Asymmetric Schottky Tunneling Source FET*

- Explore and optimize the analog performance of the Asymmetric Schottky Barrier Tunneling Source n-FET with fully metal S/D down to sub-90nm nodes

Schottky Barrier FETs

- **Explore the performance of the Schottky Barrier MOSFET (w.r.t. improved parasitics, improved scalability)**
- **Optimize the devices for mixed mode applications**

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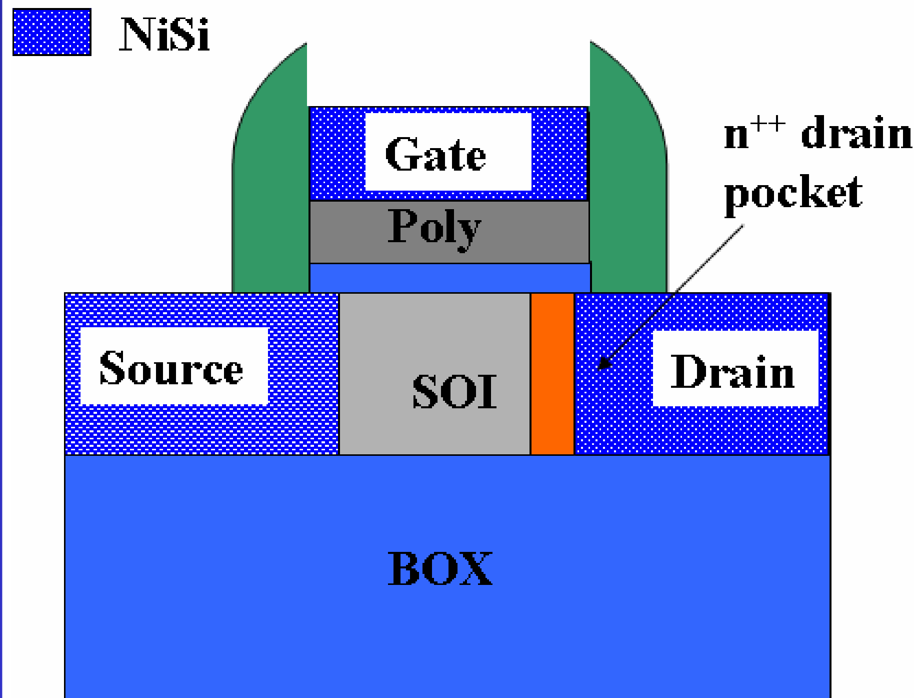
Device Concept



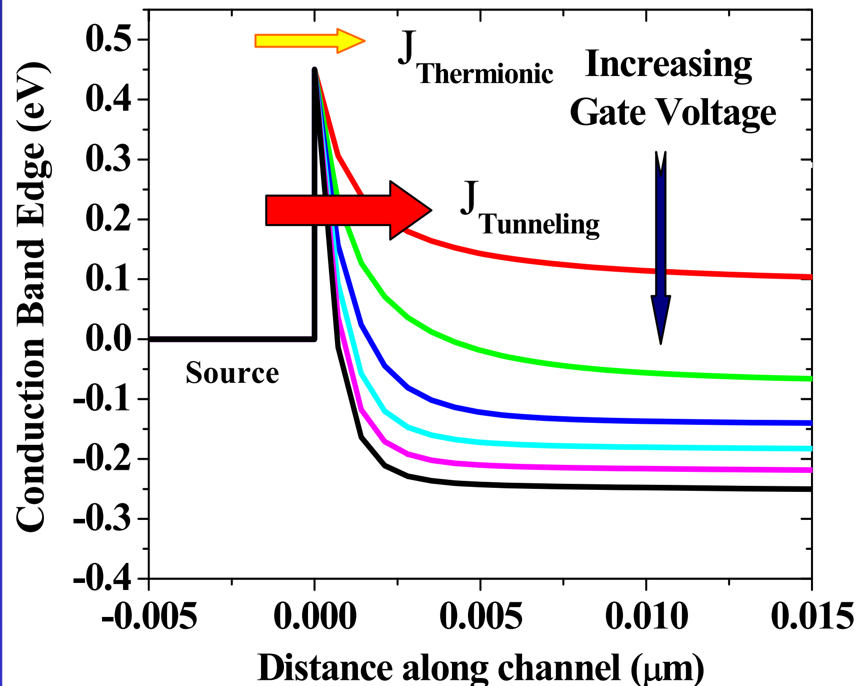
Key features - nFET

- Source injection of carriers through the schottky barrier at the source silicide-channel junction

- N+ Region on the drain side to form ohmic contact between drain and substrate

The gate controls the tunneling through the schottky barrier on the source side by changing the tunneling width as well as the available density of states on the semiconductor side

Device Concept



Band Diagram near the source end at different gate voltages for $\varphi_b = 0.45$ eV

For maximum gate control, schottky junction should be under the gate

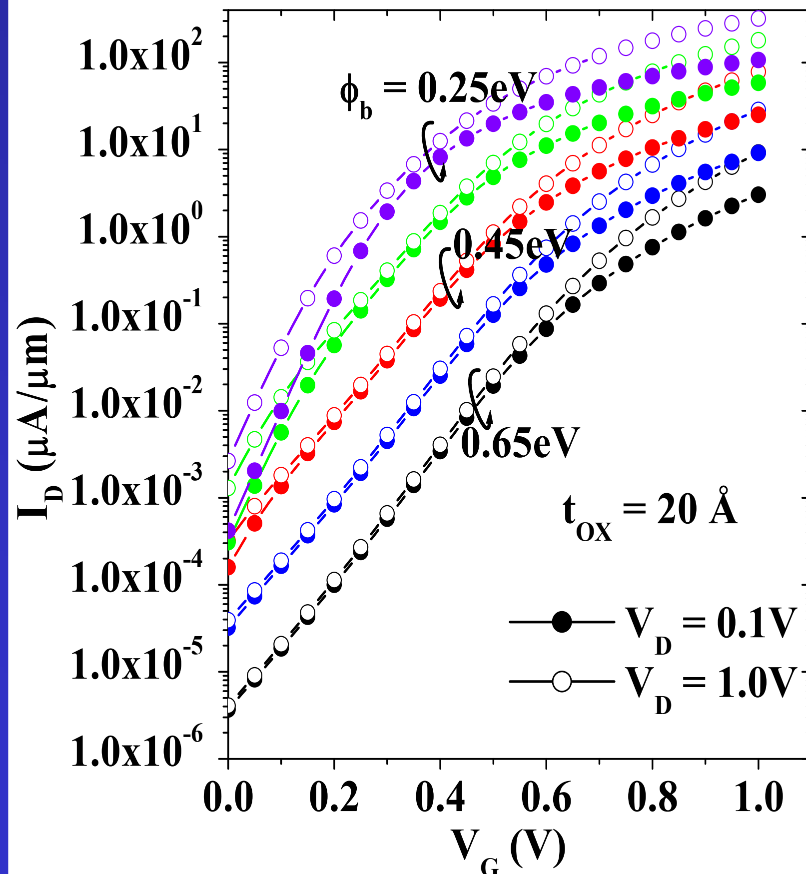
a) At low gate voltage

- **Gate voltage modulates tunneling parameters**
- **Subthreshold current is limited by schottky tunneling resistance**

b) At high gate voltage

- **Tunneling Resistance decreases**
- **Current gets limited by combination of channel and tunneling resistance**

Barrier Height (φ_b)

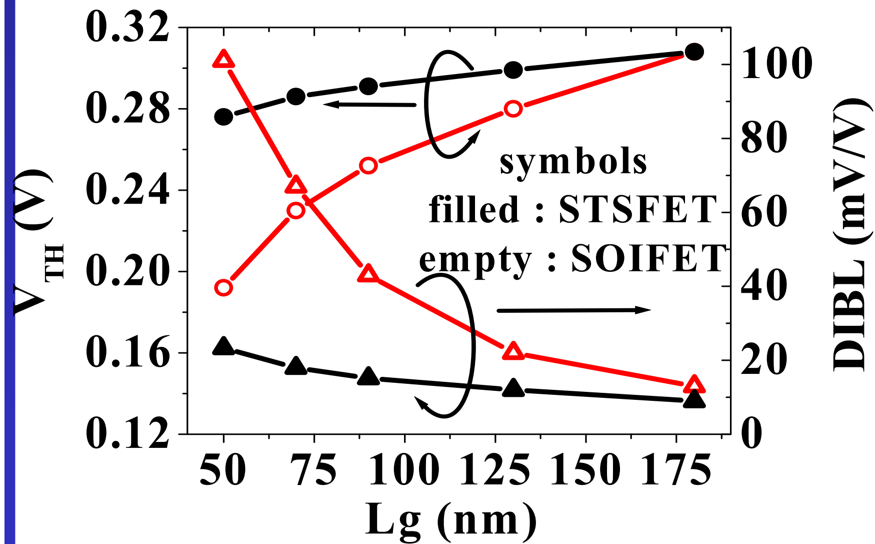


$I_D - V_G$ characteristics for different barrier heights (φ_b)

- At same t_{OX}, subthreshold characteristics dominated by tunneling at high φ_b
- For the same V_{GT}, the drive current degrades at high φ_b
- However, Short Channel Effects (DIBL) are considerably improved with tunneling at high φ_b

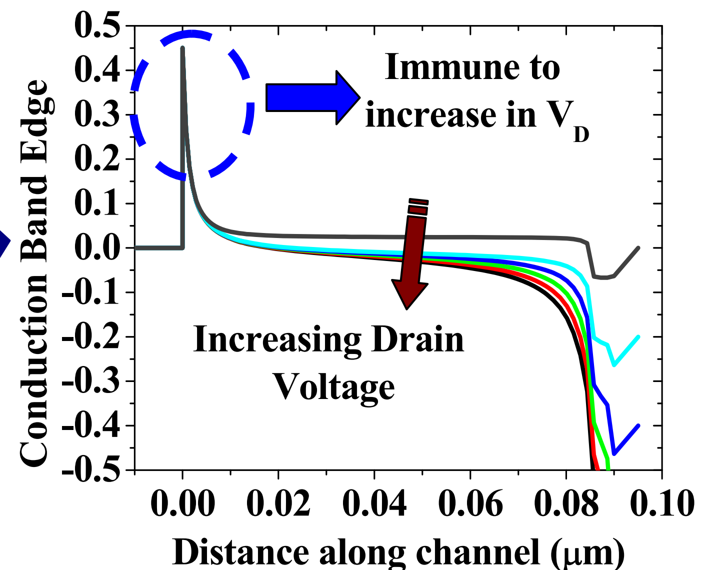
Trade-off in the barrier height to be for optimal performance

Scalability of the STS-FET



Dramatic **Improvement** in Linear V_{TH} **roll-off** and Drain Induced Barrier Lowering **(DIBL)**

- The junction at the source side is not affected by drain voltage (immune to drain field)



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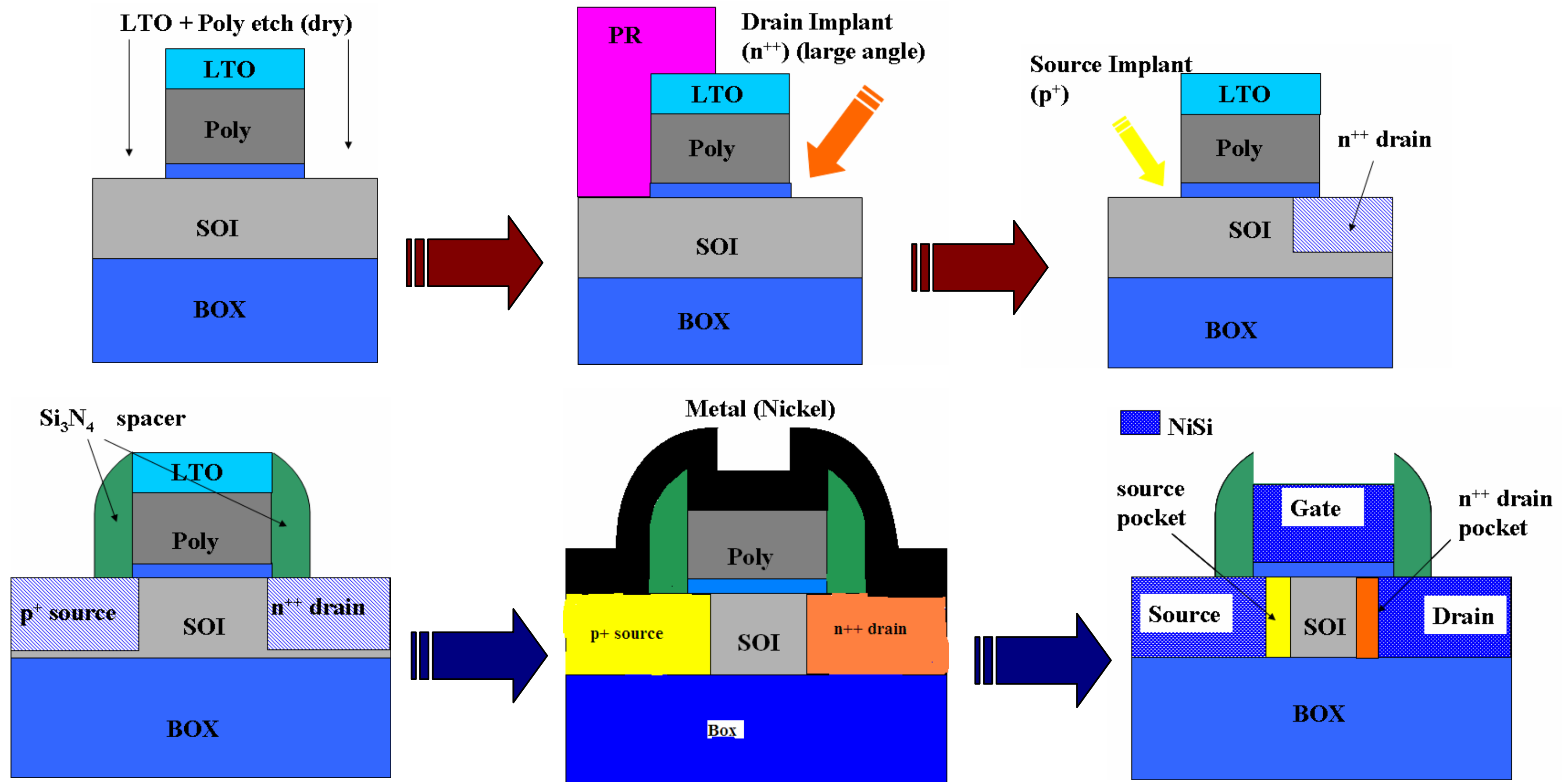
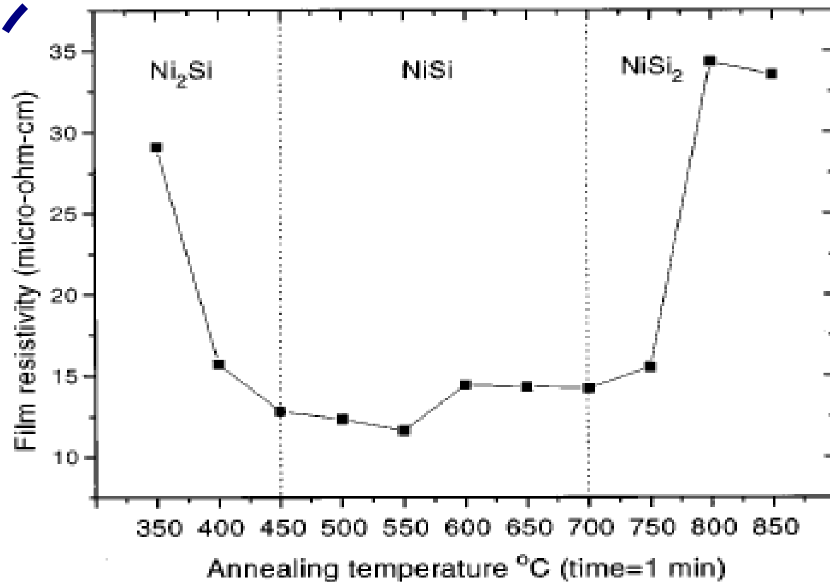
Device Fabrication (Process Flow)



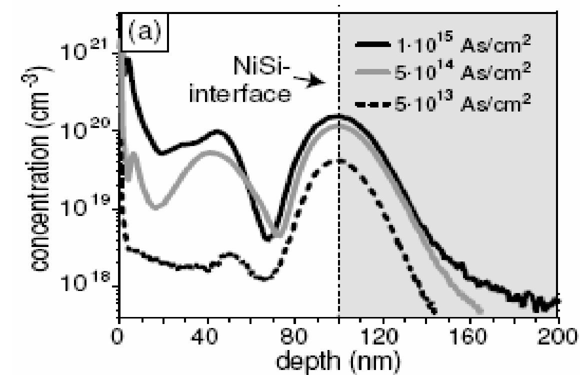
Fabrication facility: Stanford nanofabrication facility

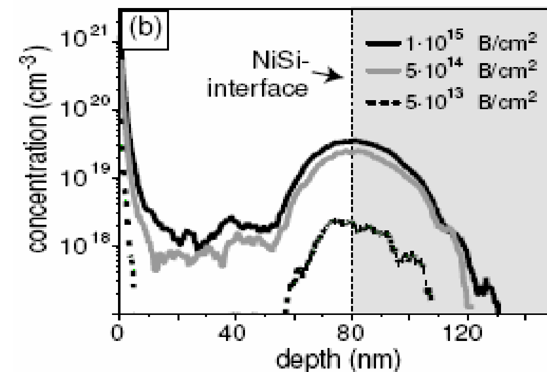
Nickel Silicide



NiSi has the same R_{Sheet} **irrespective of line-width** as well as **thermal stability** over a wide temp. range

φ_{be} of NiSi (0.55-0.65eV) → current injection is dominated by tunneling mechanisms

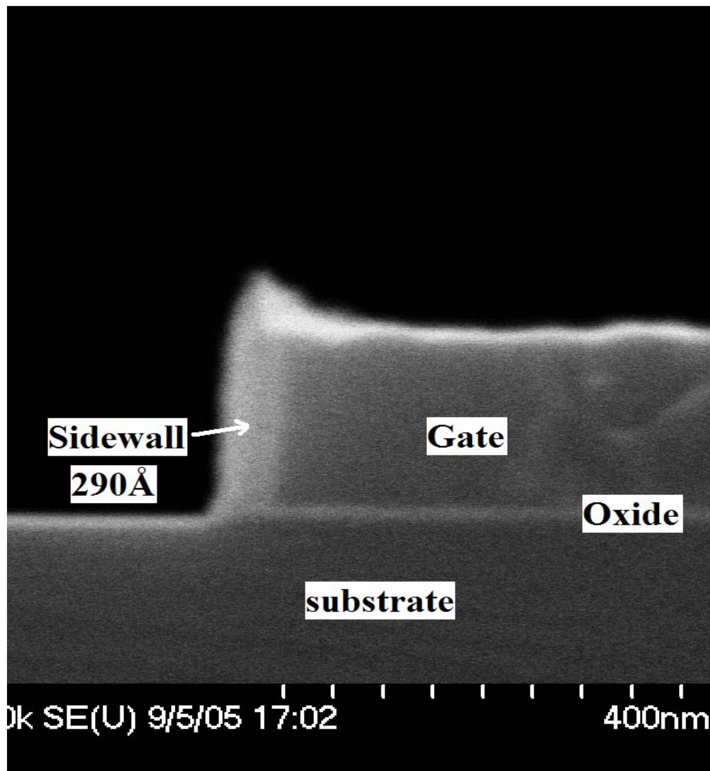


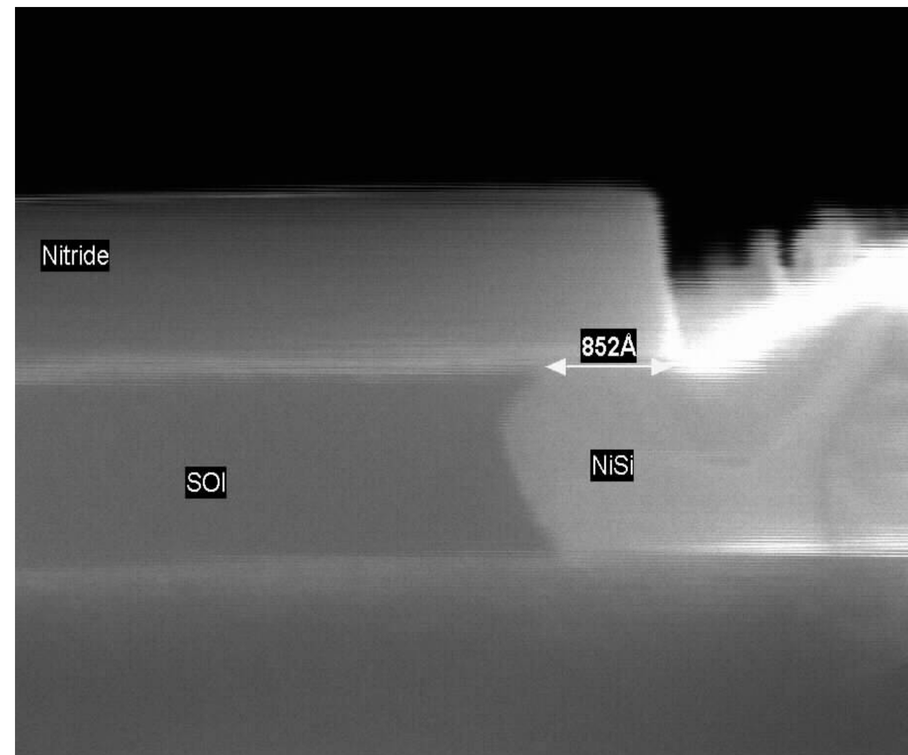


M. Zhang et al, *Proceedings of ESSDERC*, Grenoble, France, pp. 457, 2005.

Dopant segregation during Ni- silicidation observed for As and B (pile up at the interface)

Key Fabrication Steps





- **Ultrathin Nitride Sidewall** & prevention of stringers using the sidewall profile shown

- Full silicidation of the 90nm Si film
- **Encroachment of NiSi** under the gate

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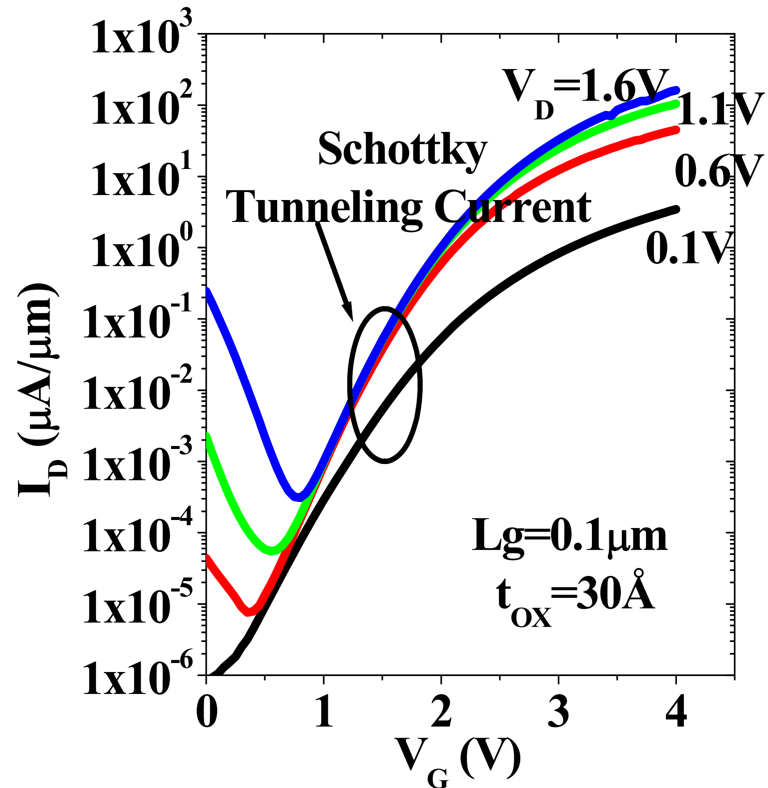
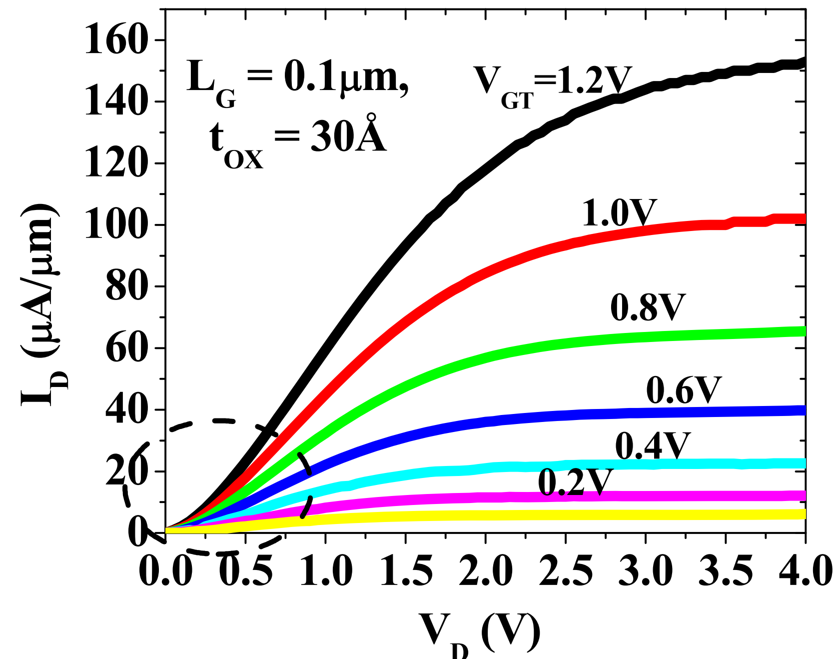
Device Characteristics

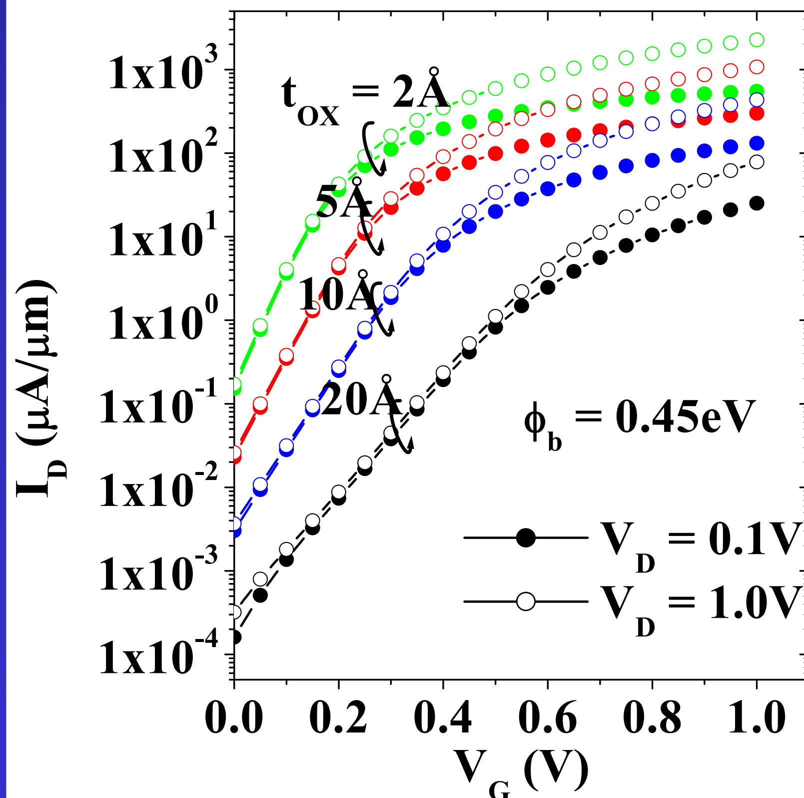


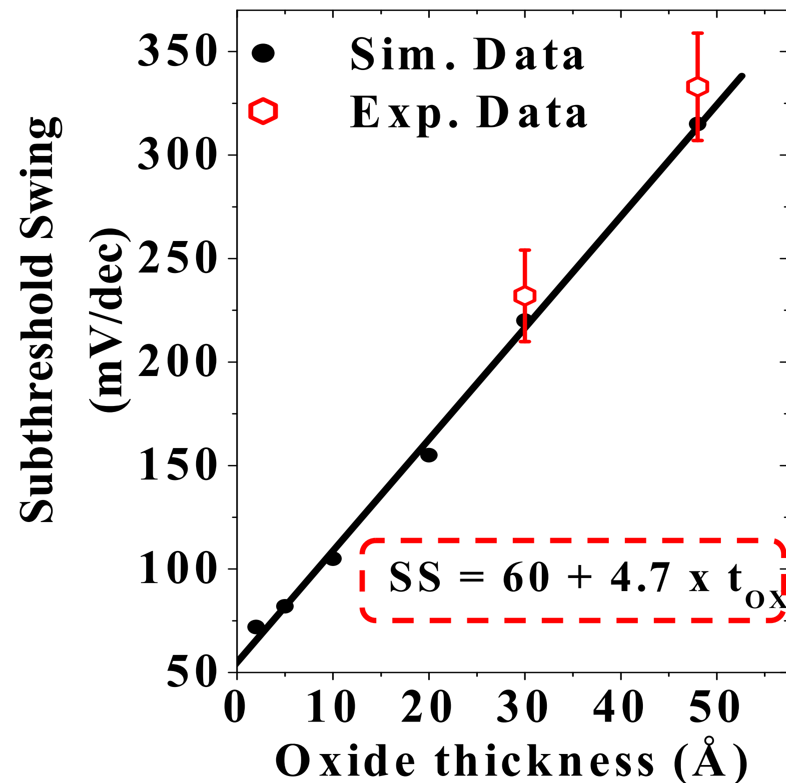
I_D-V_G curves for the NiSi STS nFET L_G = 0.1μm



I_D-V_D curves for the NiSi STS nFET L_G = 0.1μm

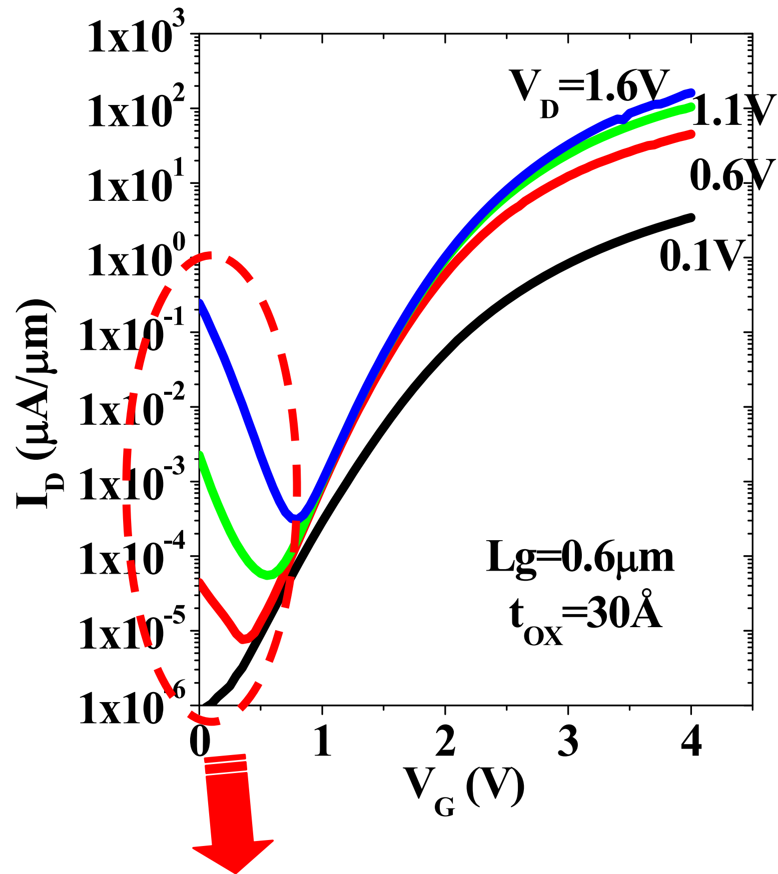
Gate Dielectric Thickness (t_{OX})

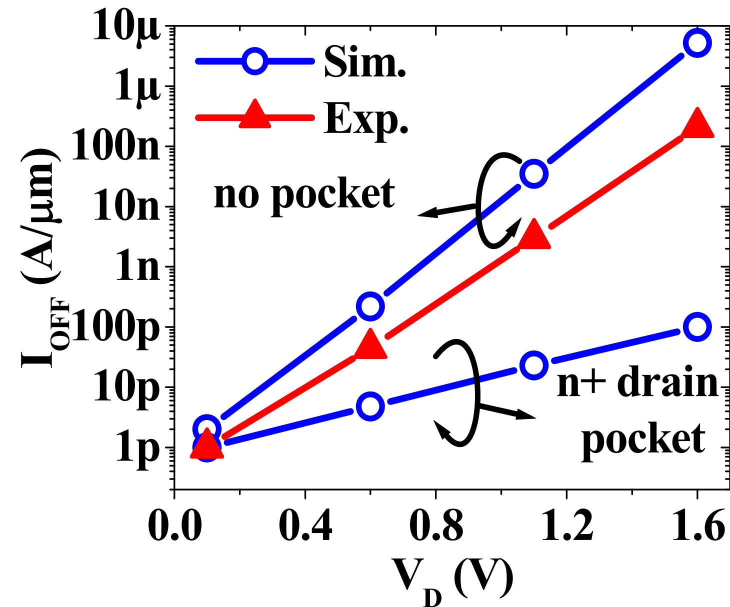




- 1st order: **Subthreshold Swing α t_{OX}** (though still > 60mV/dec)
- Also on-current improves with decreasing t_{OX}
- **Advantage: The swing is a weak function of temperature**

Drain pocket (N_{Drn})



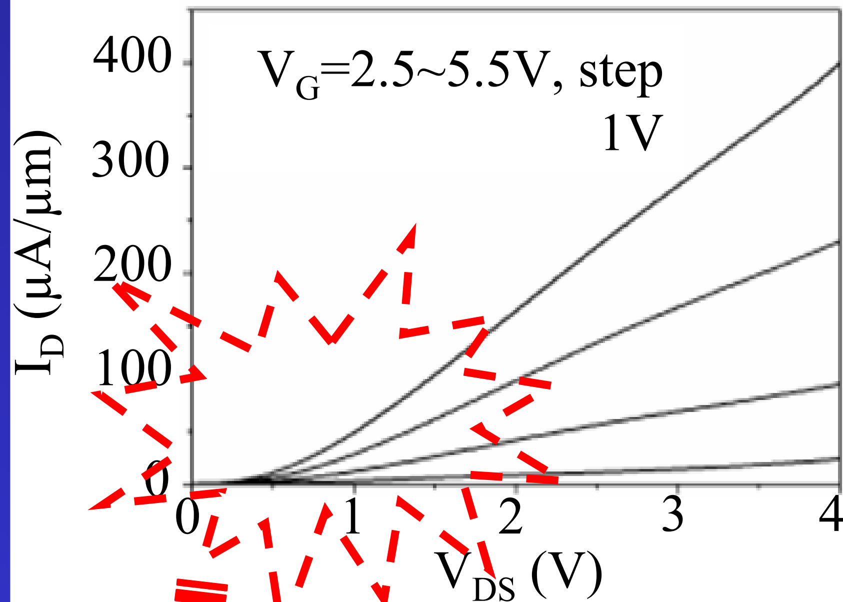


➢Caused due to tunneling of holes from the drain (ambipolar conduction)

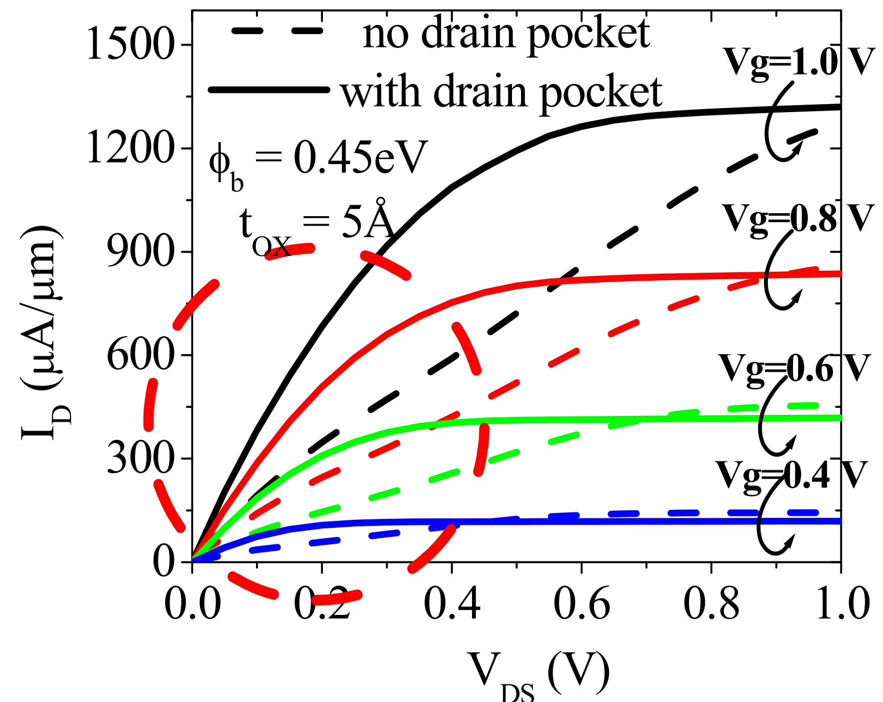
➢Increase in I_{OFF} due to **back injection of holes** from drain to source

➢A n^+ type pocket makes the drain side **junction ohmic** and hence prevents back-injection

Drain pocket (N_{Drn})



Q. T. Zhao et al, *Microelectronic Engineering*, Vol. 70, pp. 186, 2003.



- Degradation in the linear region. Resistance like behavior observed for low V_D's

- Improvement in linear I_D-V_D due to elimination of the drop across the schottky junction at the drain side

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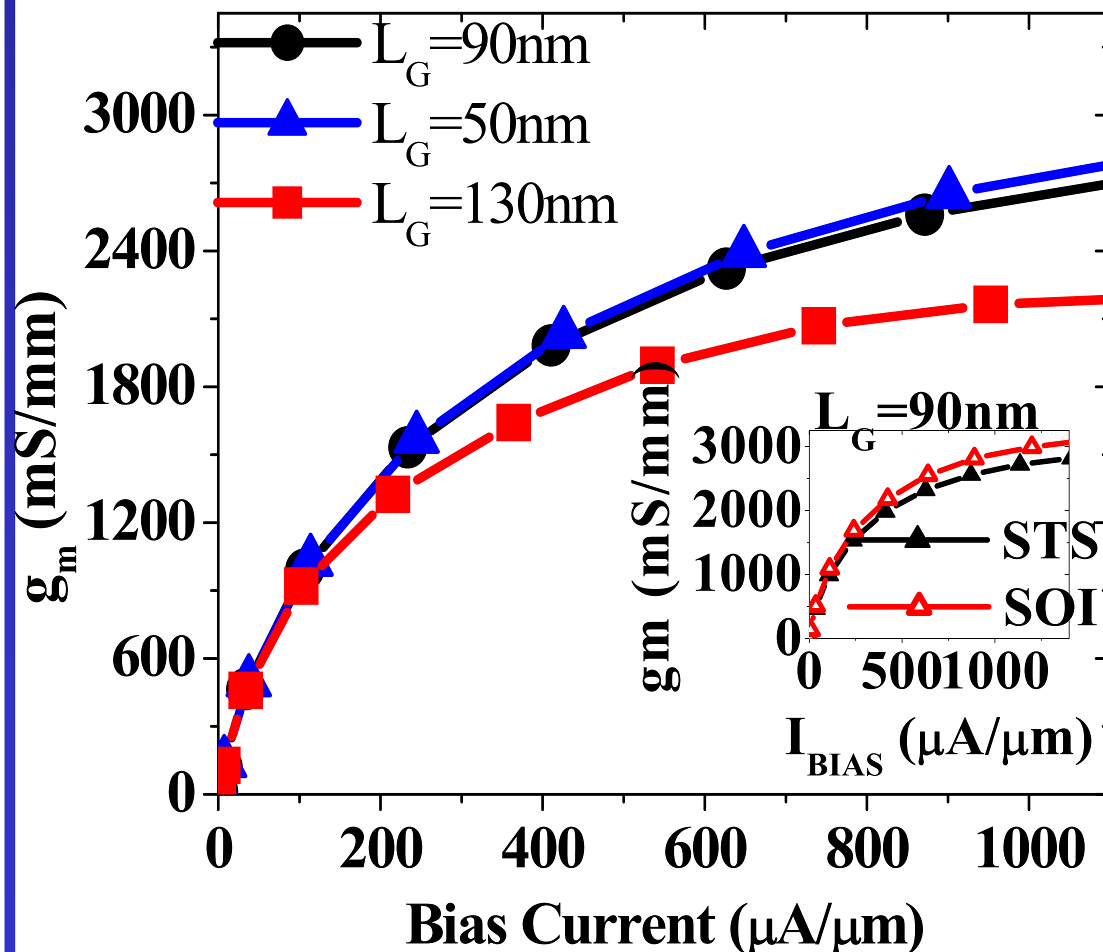
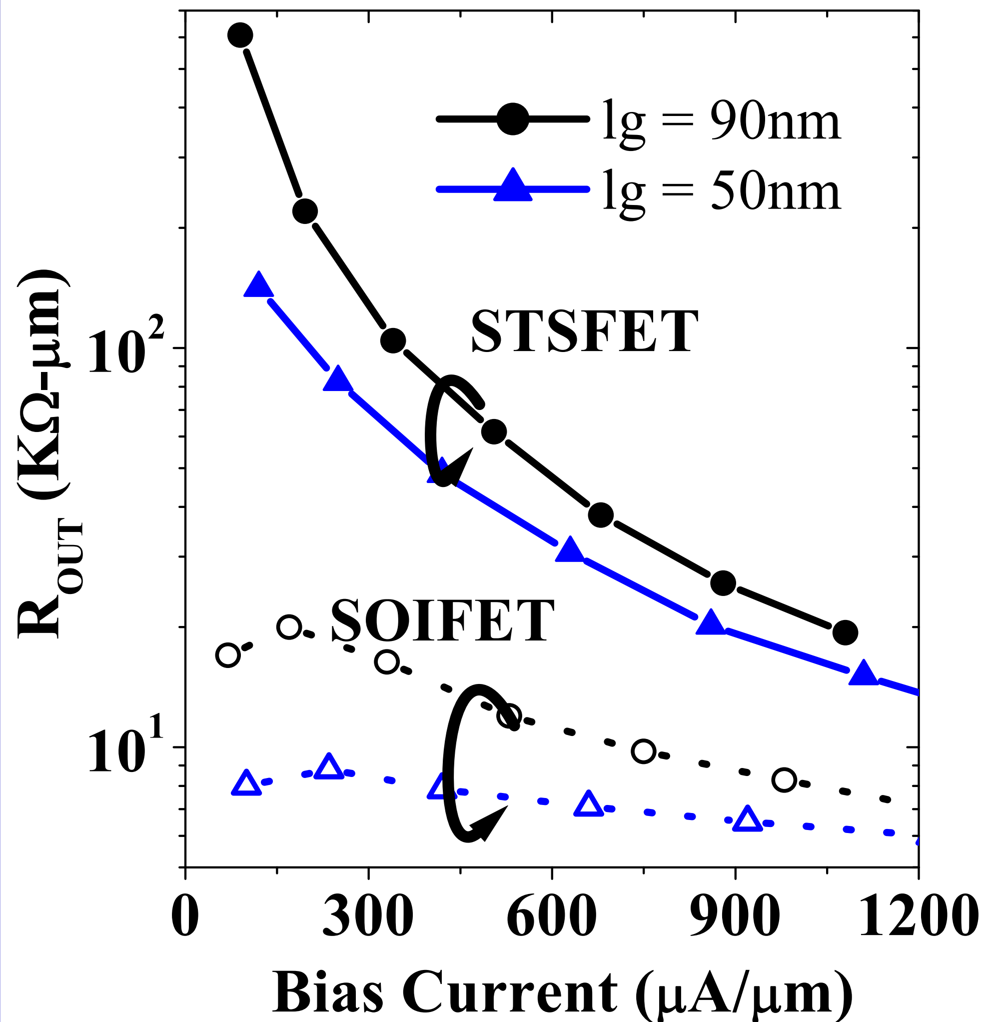
Transconductance (g_m)



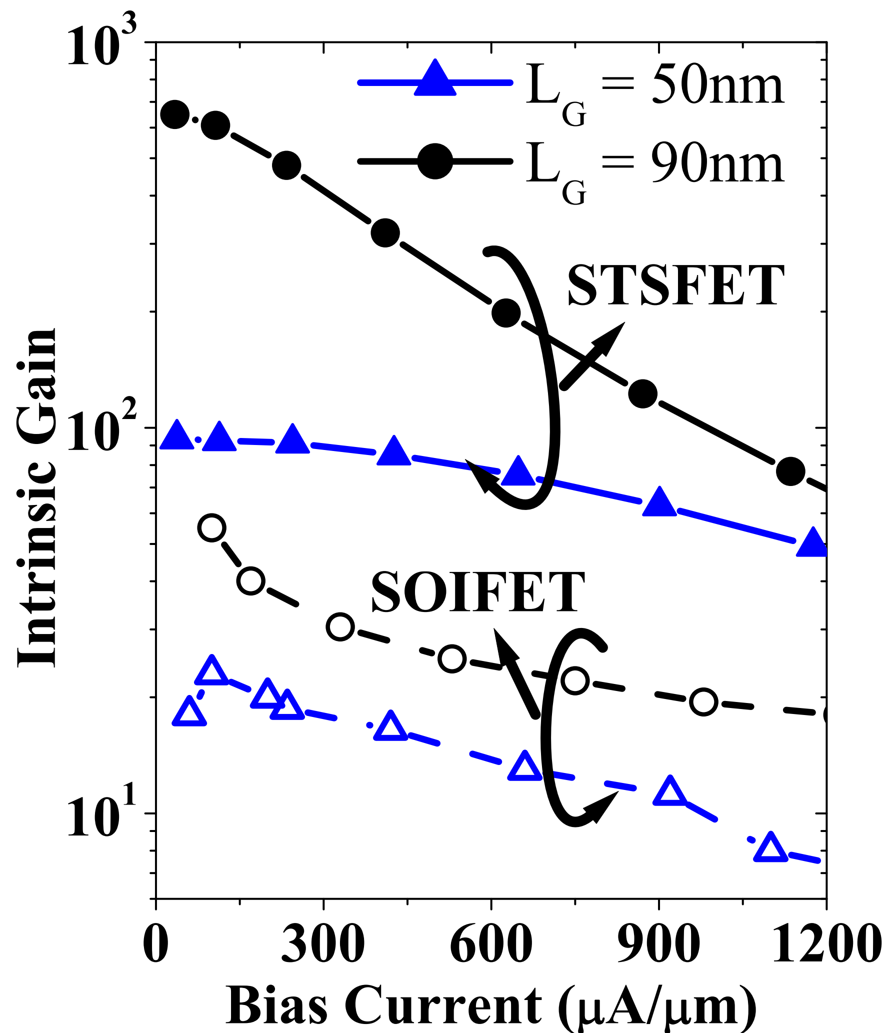
- φ_b= 0.45eV
- The STS FET has a slightly lower g_m due to the tunneling resistance of the Schottky barrier at the source end
- This decrease in g_m can be minimized by reducing the φ_b (~0.3eV)

Output Resistance (R_{OUT})



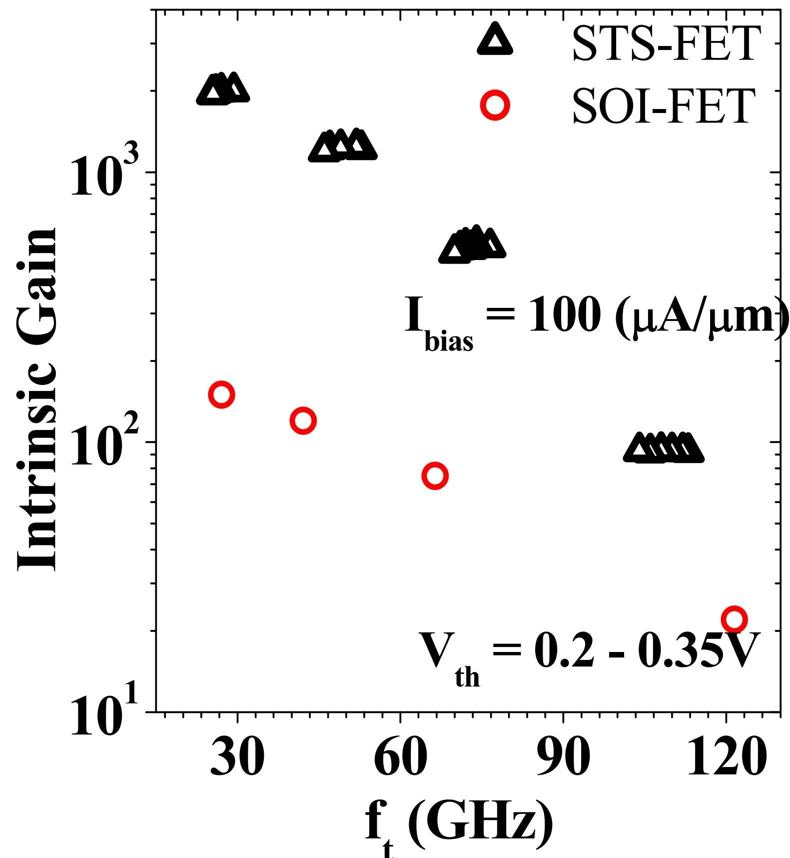
- Since V_D has small effect on tunneling at the source side, DIBL is greatly reduced
- As a result, there is an order improvement in R_{OUT}
- As expected R_{OUT} reduces with increasing I_{bias} due to channel length modulation effects

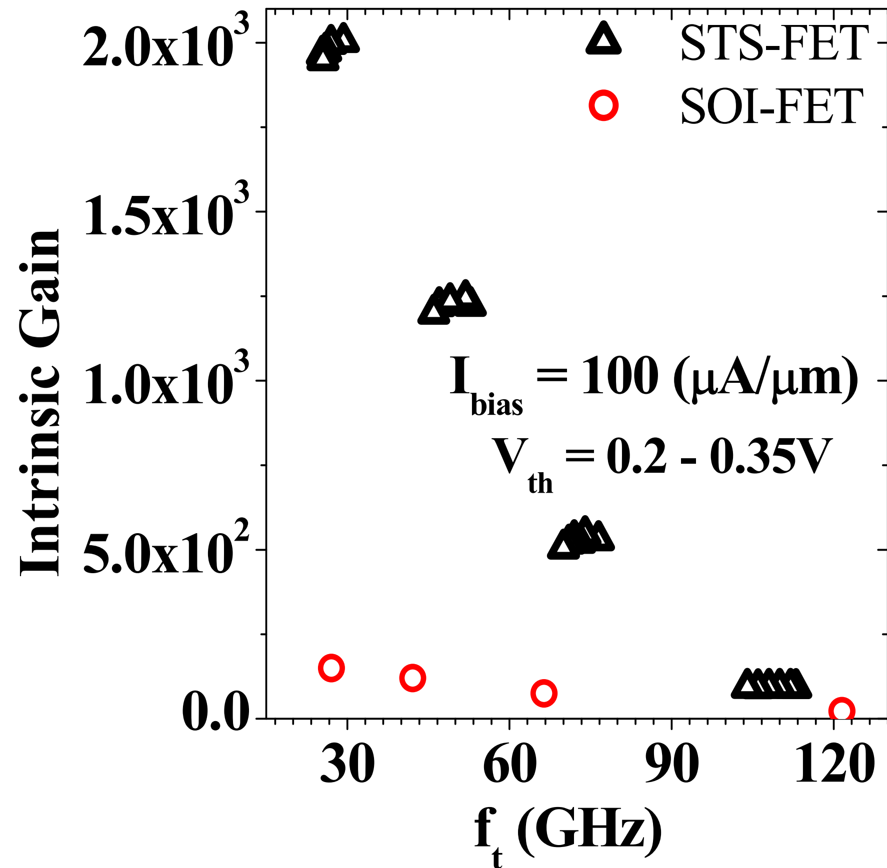
Intrinsic Gain [A_V]



- Net increase in intrinsic gain (A_V) of the STS-FET as compared to conventional SOI-FET
- A_V of close to 100 is obtained for sub-90nm technologies
- Gain is maintained for bias currents as high as 500µA/µm

Frequency-Gain Performance





- Comparable f_t for STS-FET for similar technology nodes
- *Improvement in Frequency-Gain performance* for different technology nodes at a given bias current

Conclusions

- Need to *explore alternate structures* to continue scaling of analog systems

- Asymmetric Schottky Tunneling Source MOSFET concepts studied and key parameters optimized
  - $\varphi_b \sim 0.3 - 0.65$eV, EOT < 10Å,
  - Drain-side pocket to improve linear characteristics

- Optimized device structure highly immune to Short Channel Effects ⇨ *Very Scalable Transistor Structures*

Conclusions (contd.)

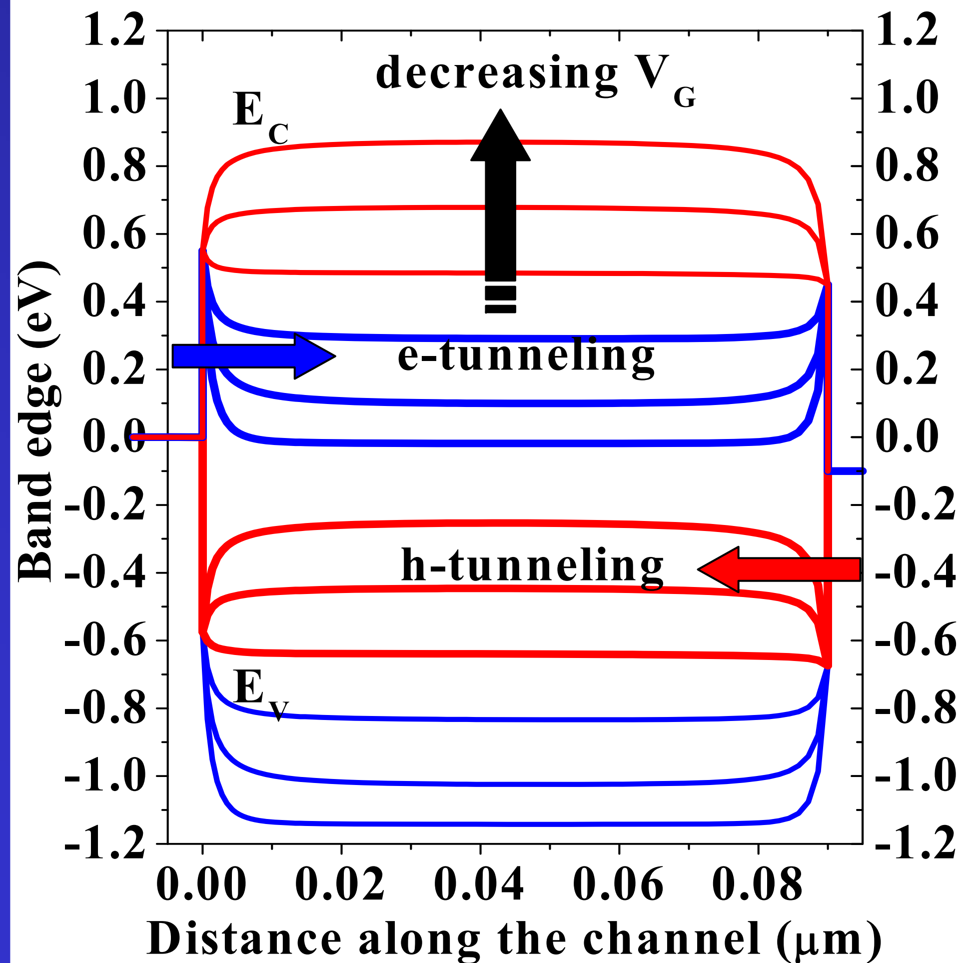
- g_m is slightly lower when compared to conv. MOSFET, but decrease can be minimized by minimizing φ_b
- Big *Improvement in* R_{OUT} *and intrinsic gain* $(g_m x R_{OUT})$ even at $L_G < 90$nm
- *Exceptional frequency-gain performance* even at high bias currents
- Promising Alternative for mixed mode, RF and SOC applications

The end is the beginning

THANK YOU

Questions ?

(a) Back injection (Ambipolar trans.)



- If the drain pocket doping is not high
  → At a certain gate voltage, E-field at the junction changes sign

- Tunneling of holes (Drain-to-Source) becomes favorable
  → Back injection leakage

(b) Summary of Results

Physical Parameter	Optimized value (for n-FET devices)	Comments
Barrier Height (φ_b)	**$0.35eV < \varphi_b < 0.65eV$**	High enough for tunneling to dominate
Gate dielectric thickness (t_{OX})	**$t_{OX} < 10Å$**	t_{OX} should be minimized
Drain Side Pocket (N_{Drn})	**Highly doped n^{++}**	Ohmic junction (like a conventional FET)
Scalability	**highly immune to SCE**	Attractive for analog applications and high scalability