

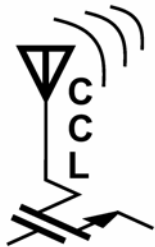
# ***Systematic Transistor and Inductor Modeling for Millimeter-Wave Design***

**Chaunkang Liang and Behzad Razavi**

**Communication Circuits Laboratory**

**Electrical Engineering Department**

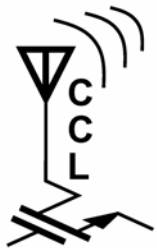
**University of California, Los Angeles**



# Outline

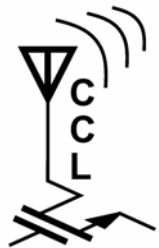
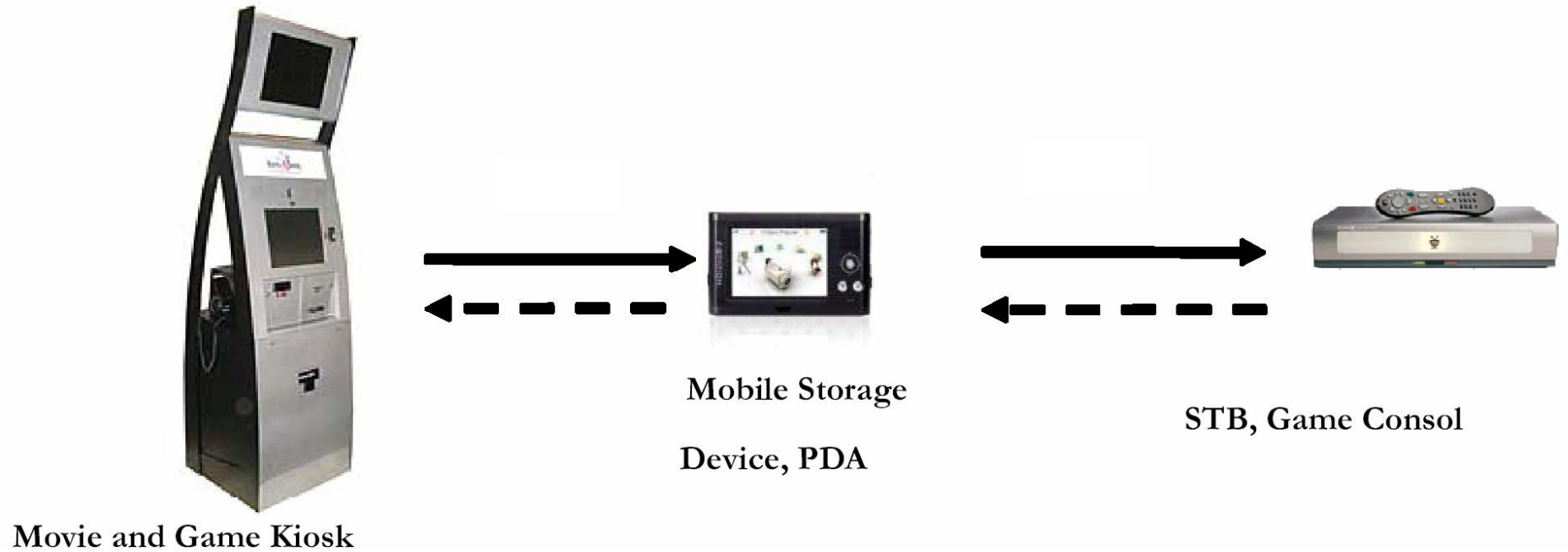
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- Introduction
- Modeling Issues in Transceiver Design
- Proposed Transistor Model
- Interconnect and Inductor Models
- New Layout Techniques
- Experimental results
- Conclusion



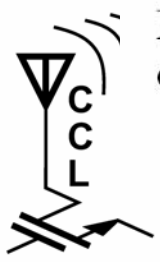
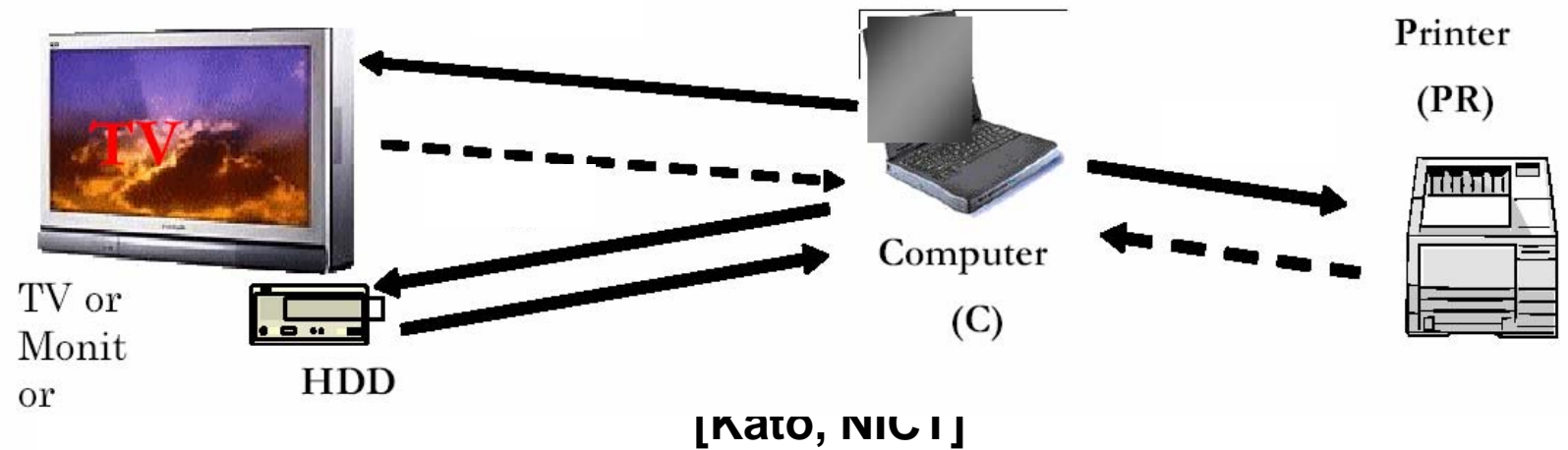
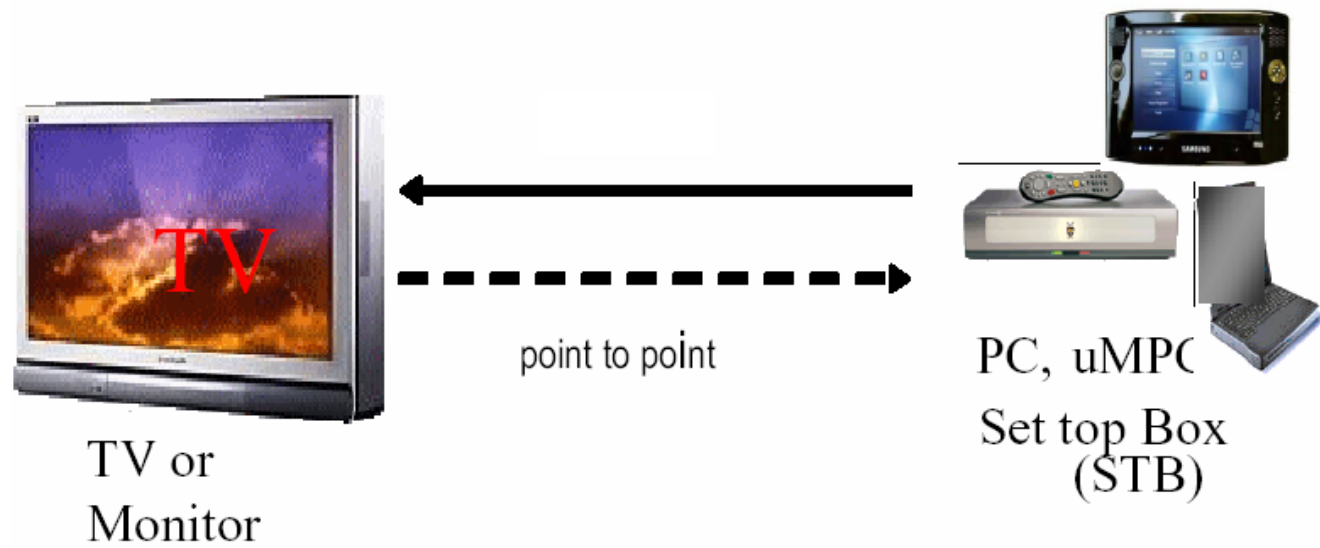
# Application: Quick Download

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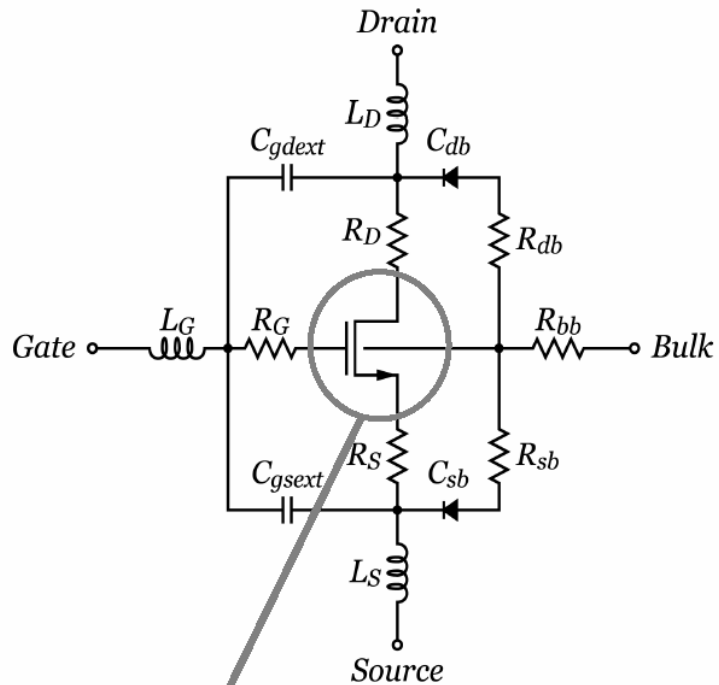


[Kato, NICT]

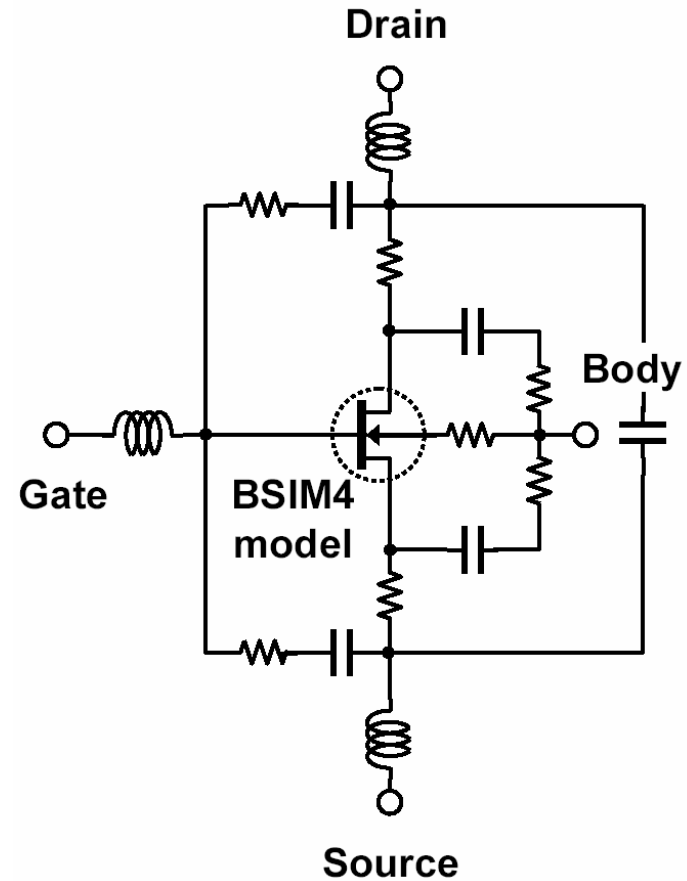
# Other Applications



# Measurement-Based Modeling

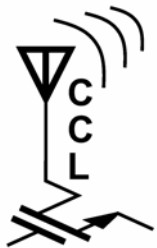


BSIM Modified Model

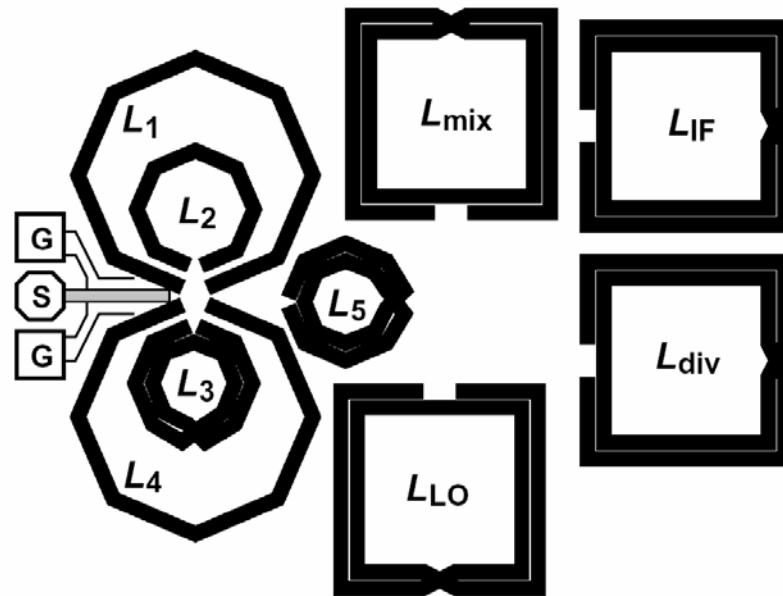
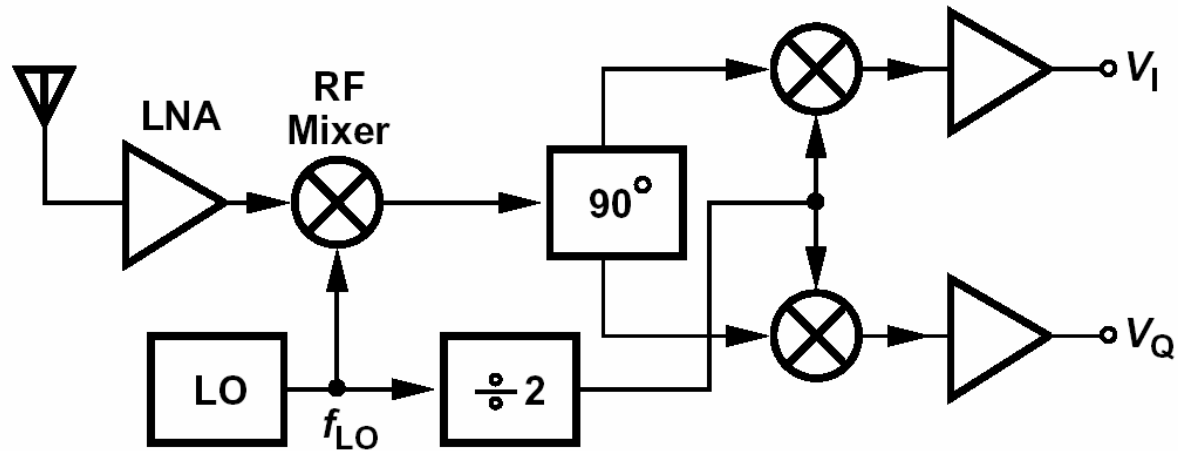


[Chowdhury, ISSCC08]

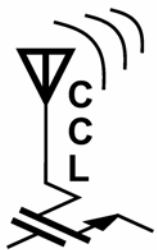
[Suzuki, ISSCC08]



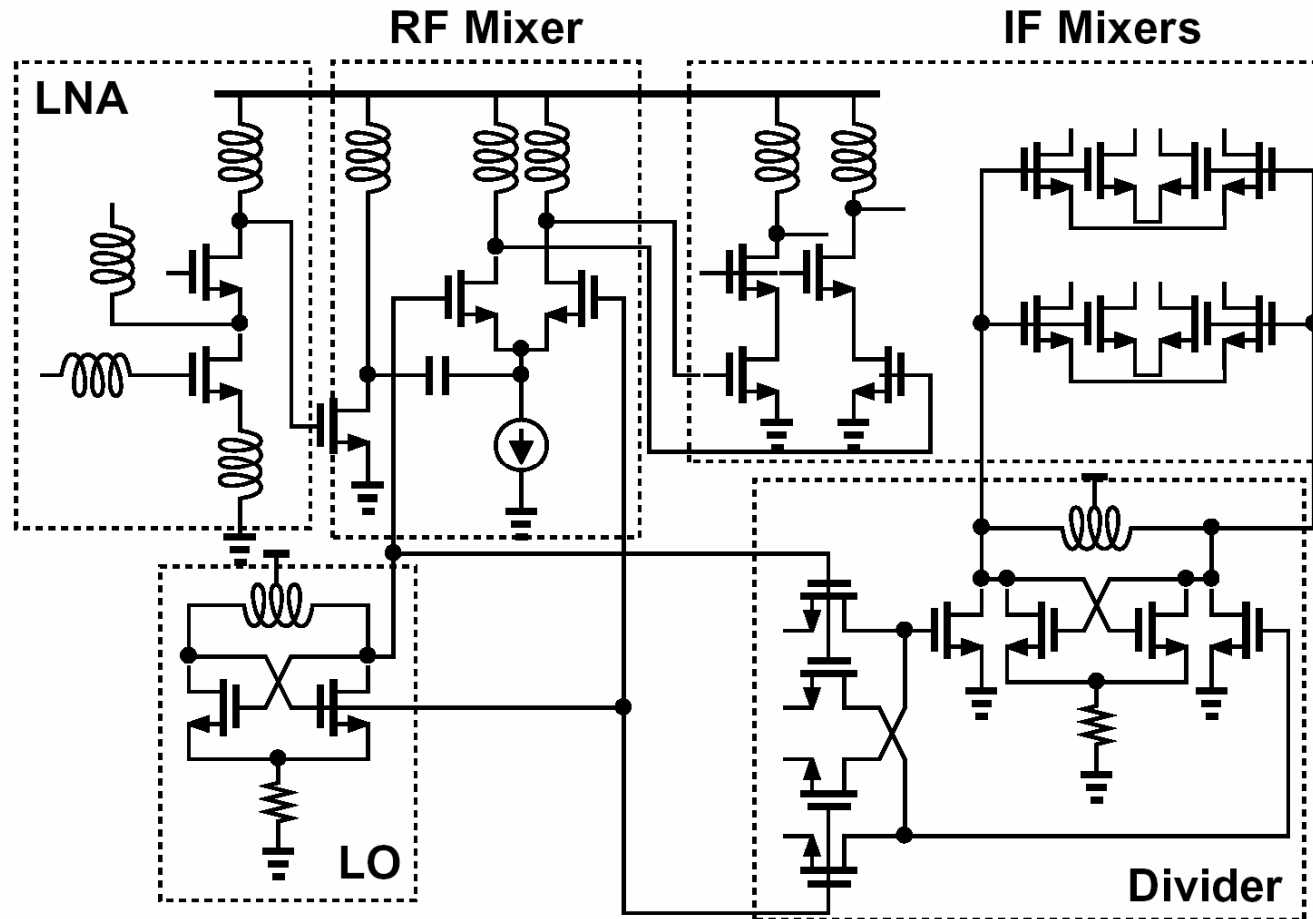
# Example of mmW System



[Razavi, ISSCC07]



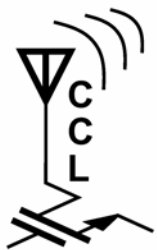
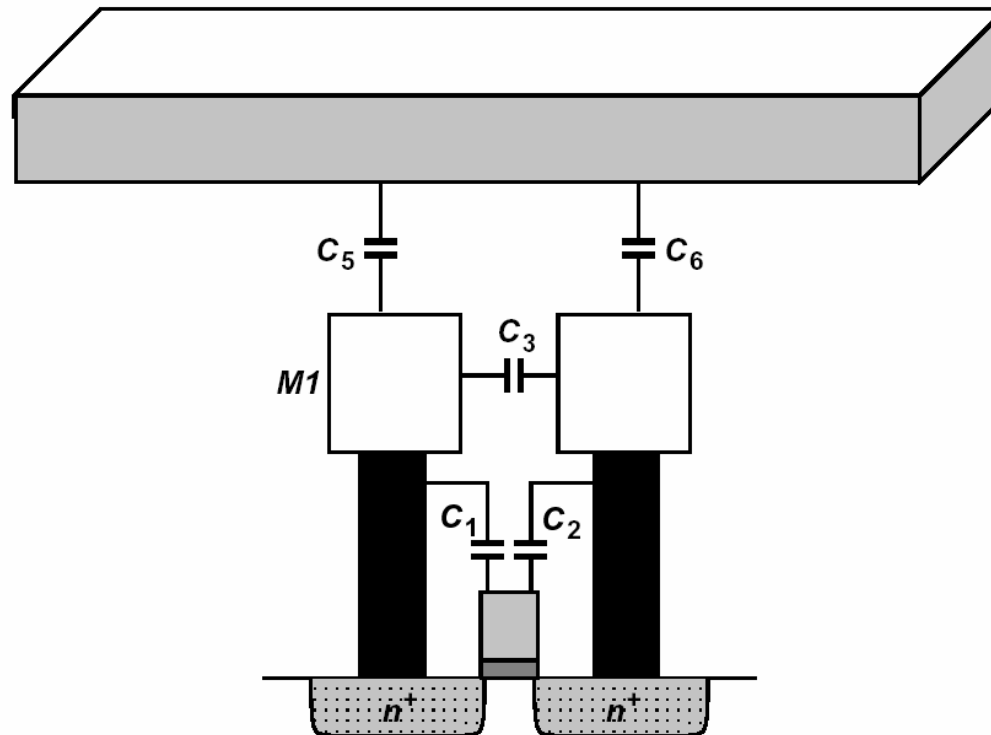
# How Many Transistor Geometries?



$$\frac{W}{L} = \frac{30 \text{ } \mu\text{m}}{0.1 \text{ } \mu\text{m}} \quad \frac{20 \text{ } \mu\text{m}}{0.1 \text{ } \mu\text{m}} \quad \frac{16 \text{ } \mu\text{m}}{0.1 \text{ } \mu\text{m}} \quad \frac{8 \text{ } \mu\text{m}}{0.1 \text{ } \mu\text{m}} \quad \frac{7 \text{ } \mu\text{m}}{0.1 \text{ } \mu\text{m}} \quad \frac{6 \text{ } \mu\text{m}}{0.1 \text{ } \mu\text{m}} \quad \frac{5 \text{ } \mu\text{m}}{0.1 \text{ } \mu\text{m}} \quad \frac{4 \text{ } \mu\text{m}}{0.1 \text{ } \mu\text{m}} \quad \frac{1 \text{ } \mu\text{m}}{0.1 \text{ } \mu\text{m}}$$

# What if a wire runs over a device?

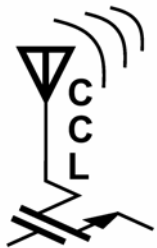
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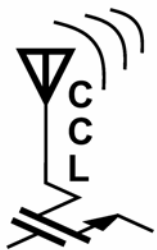
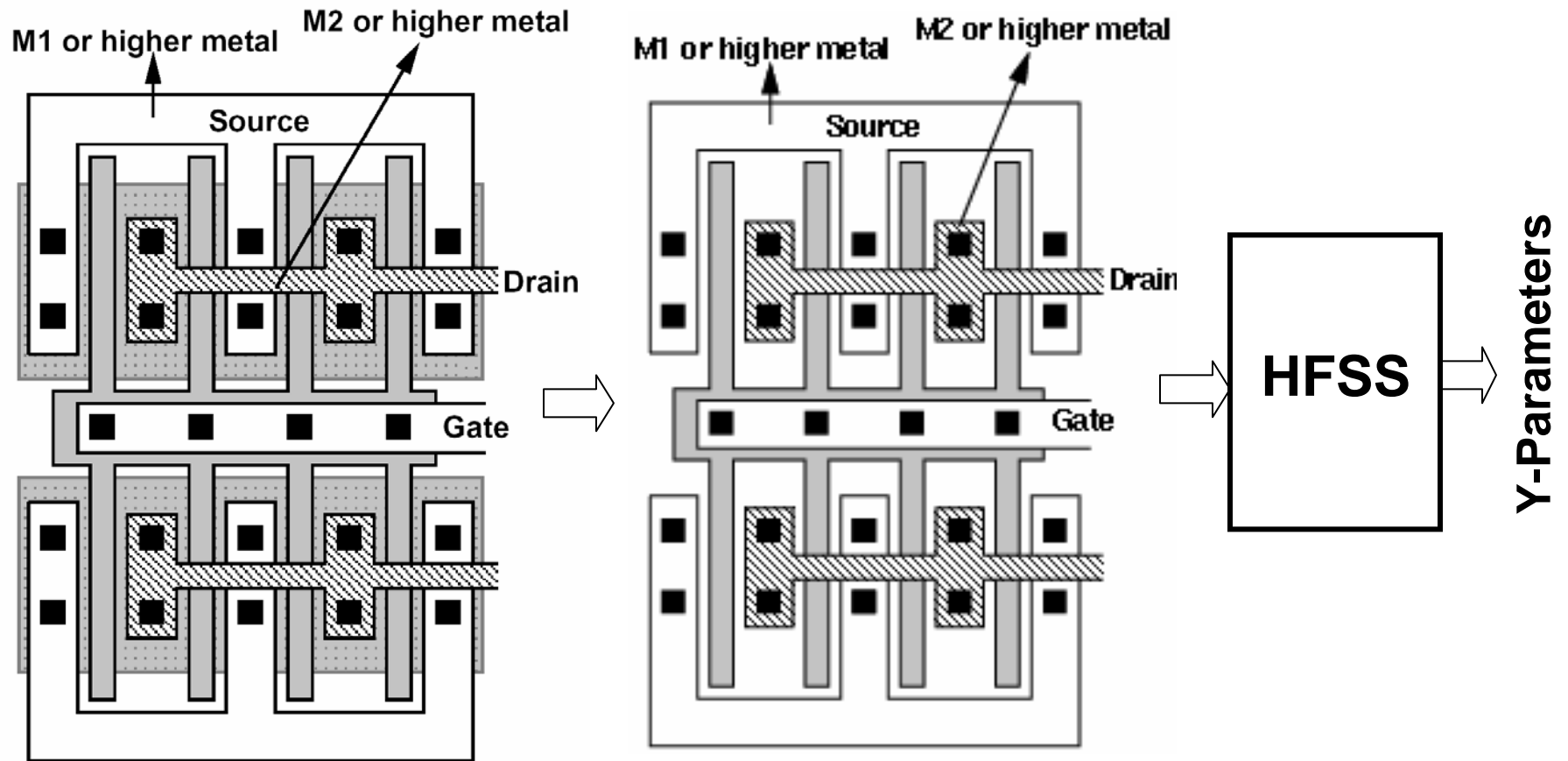
# Objective

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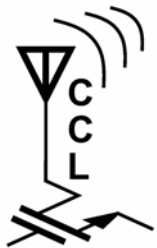
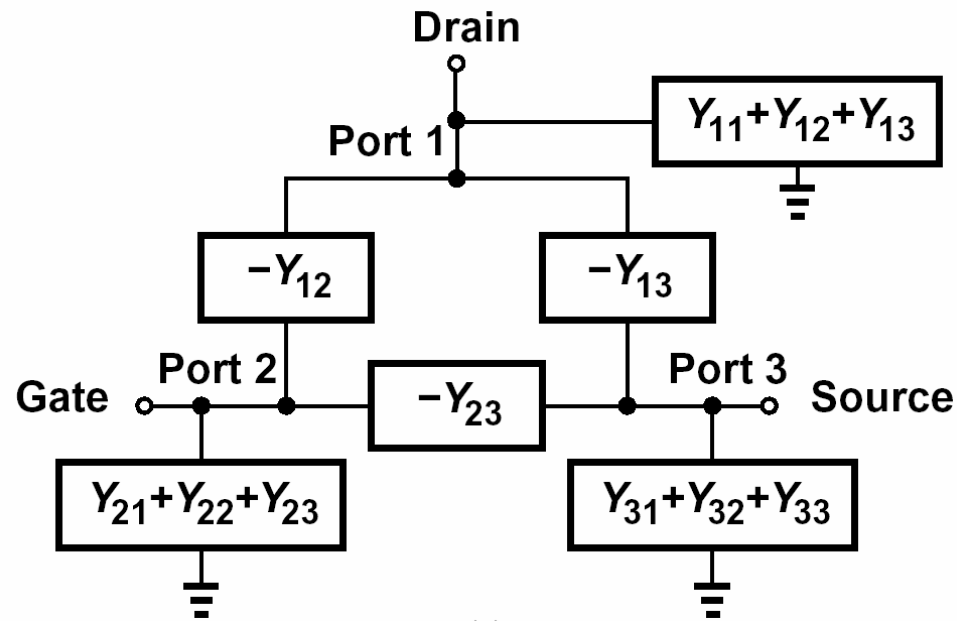
- Develop a simulation-based modeling methodology for device capacitances and inductances that handles any geometry while providing physical insight.
- Modeling must be systematic and reliable to make the designer as confident about sizing in mmW range as at low frequencies.



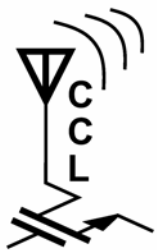
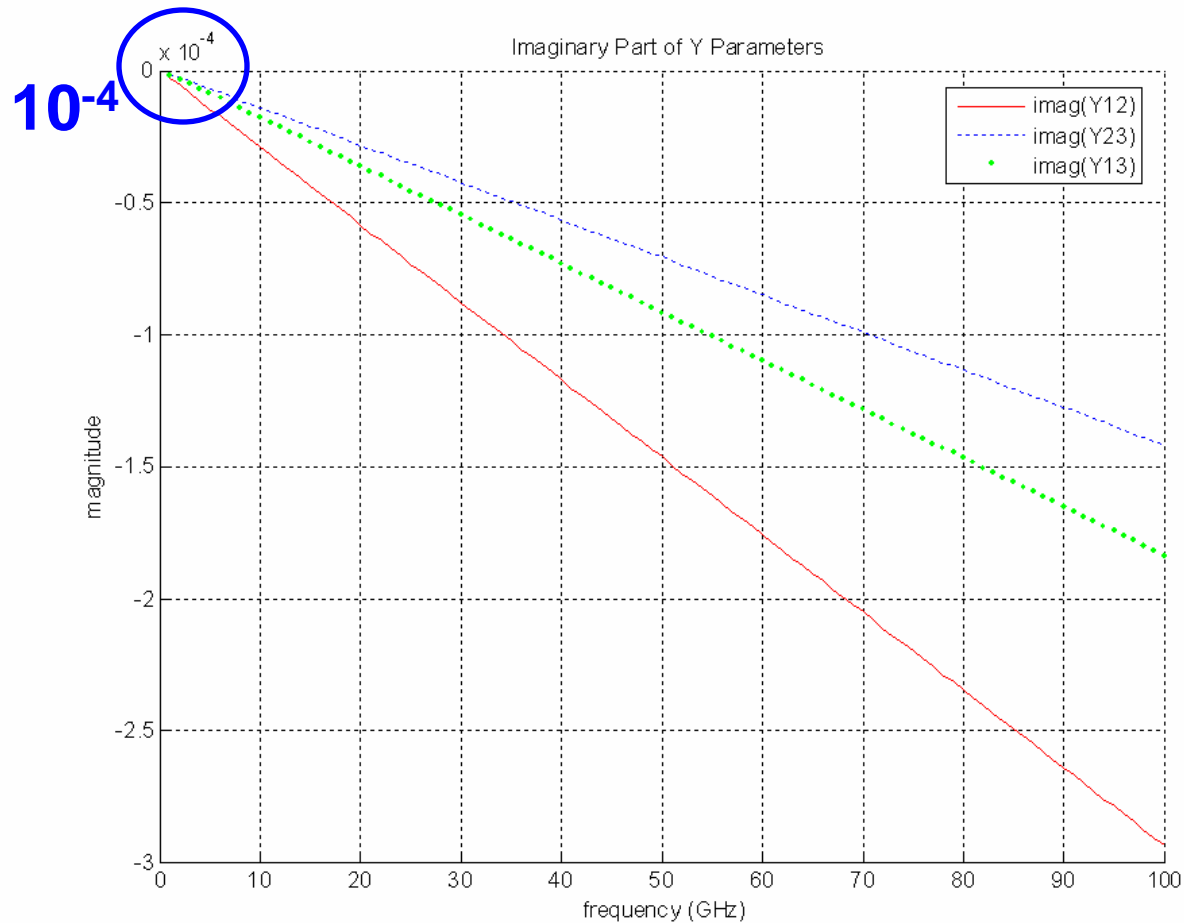
# Modeling Procedure



# Basic Model

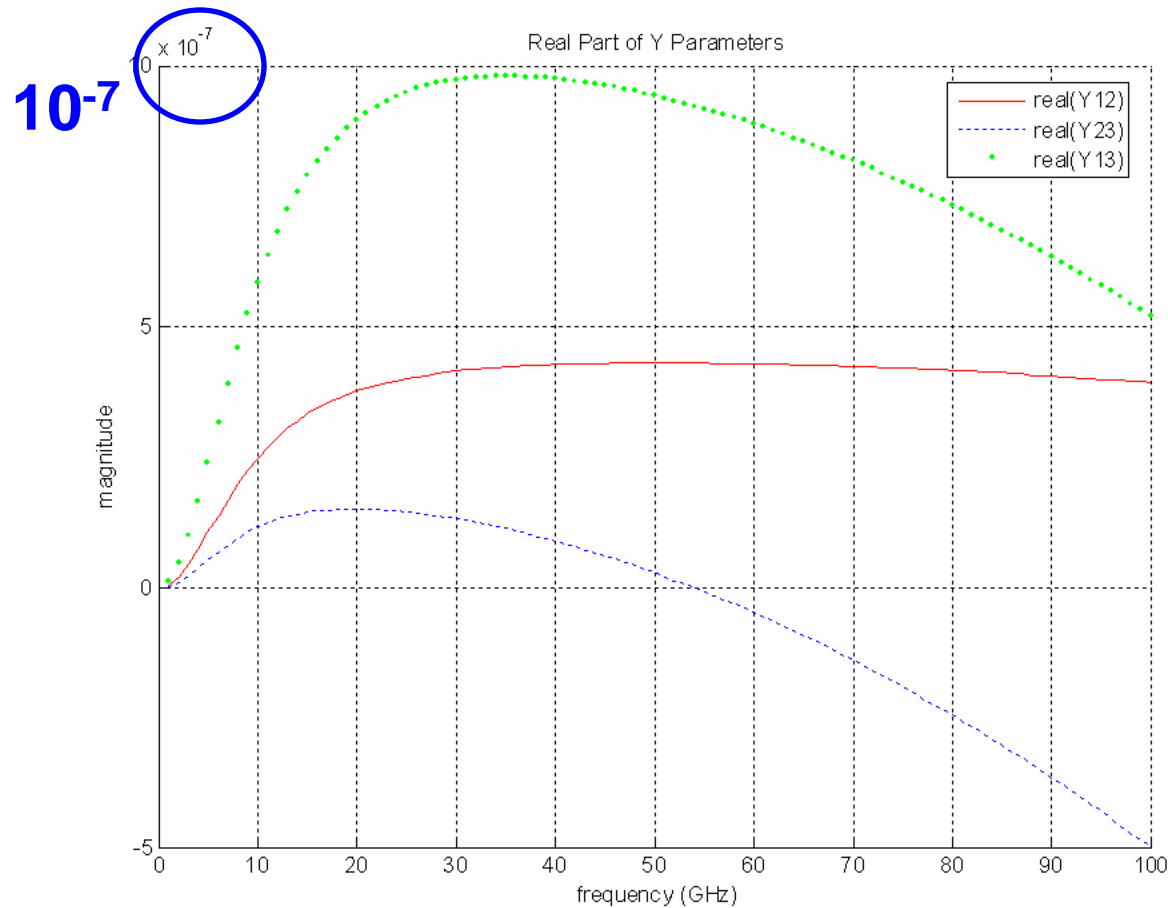


# Nature of Impedances



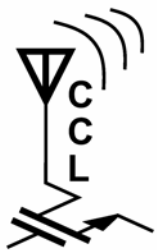
$$\text{Im}\{Y\} \propto -\omega$$

# Nature of Impedances

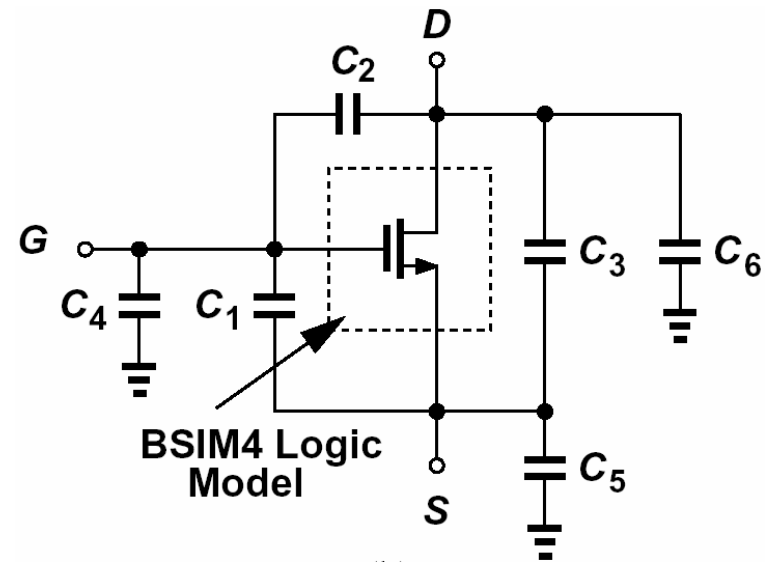
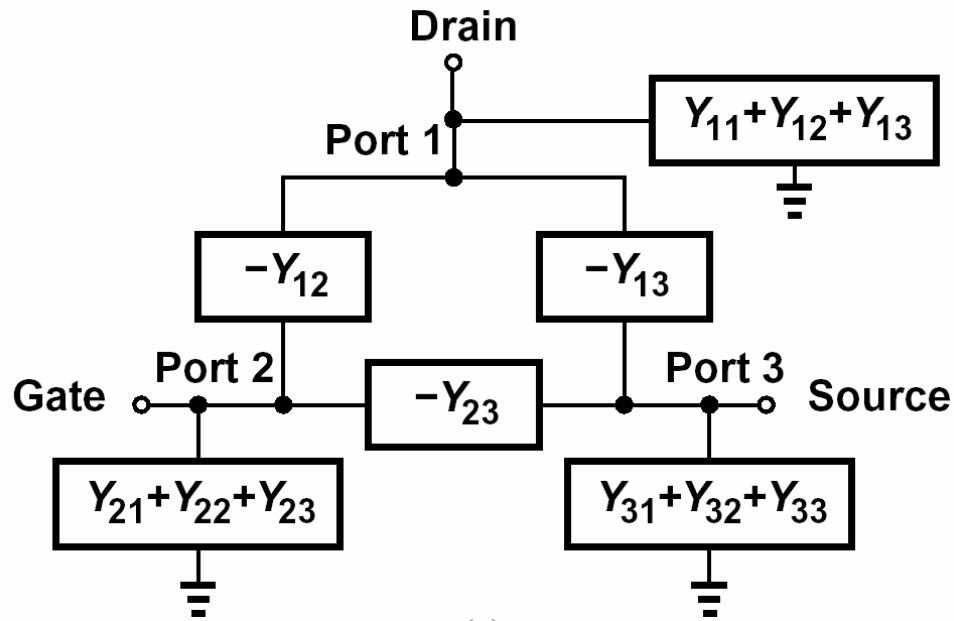


$$\text{Im}\{Y\} \gg \text{Re}\{Y\}$$

$$Y \approx \text{Im}\{Y\} = -j\omega \cdot C$$



# Extraction from Y-Parameters



$$C_1 = \frac{-\text{Im}\{Y_{23}\}}{\omega}$$

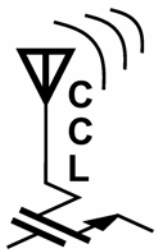
$$C_2 = \frac{-\text{Im}\{Y_{12}\}}{\omega}$$

$$C_3 = \frac{-\text{Im}\{Y_{13}\}}{\omega}$$

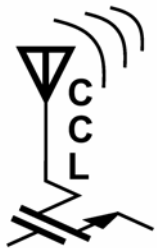
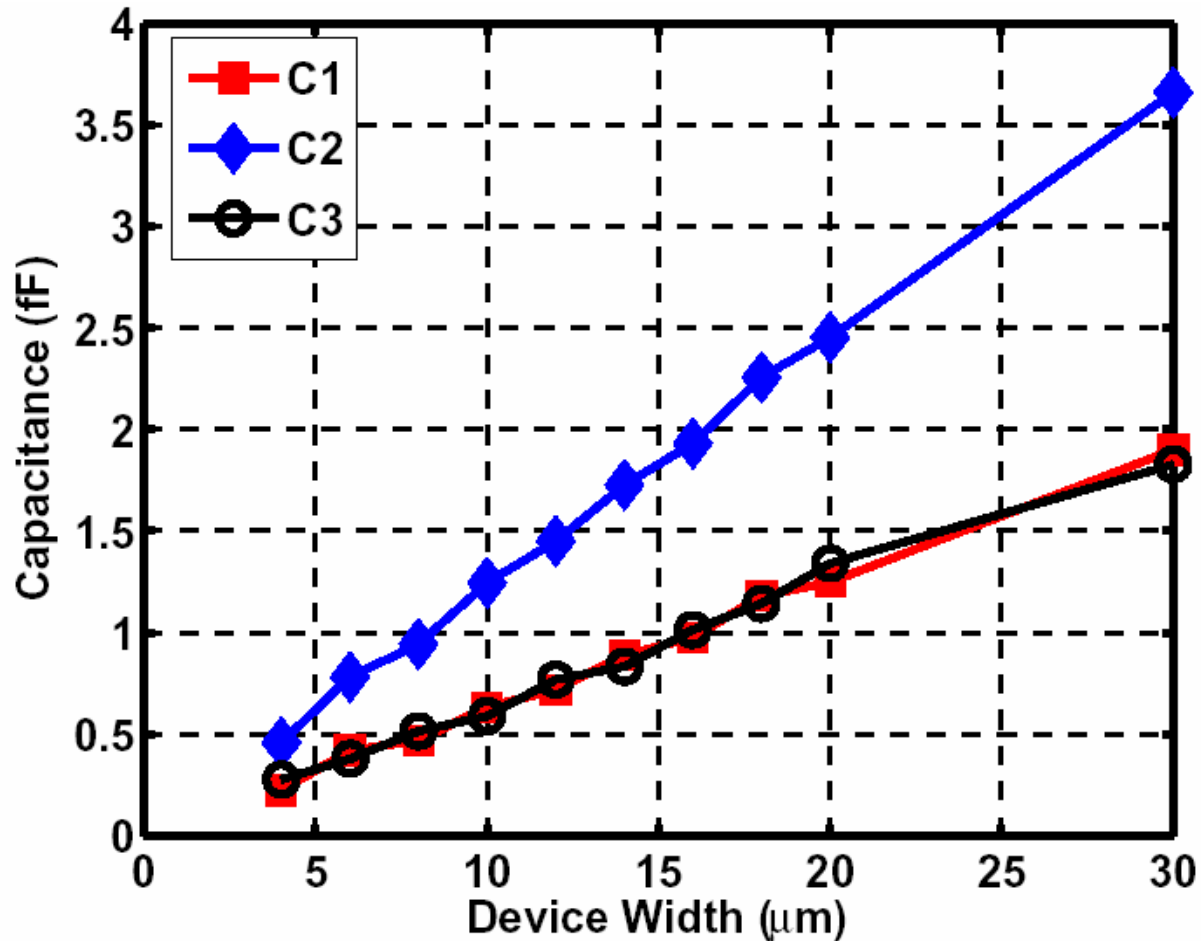
$$C_4 = \frac{\text{Im}\{Y_{21} + Y_{22} + Y_{23}\}}{\omega}$$

$$C_5 = \frac{\text{Im}\{Y_{31} + Y_{32} + Y_{33}\}}{\omega}$$

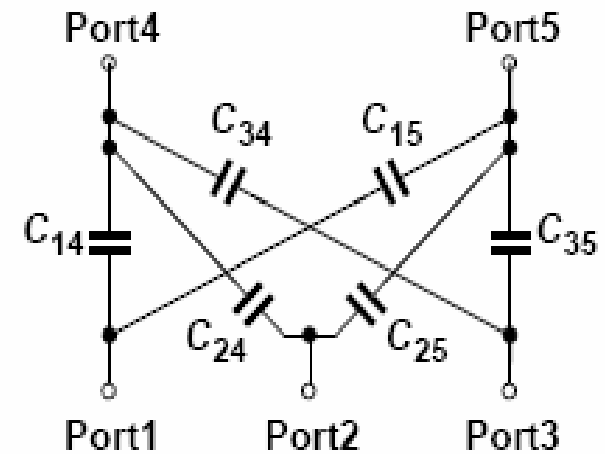
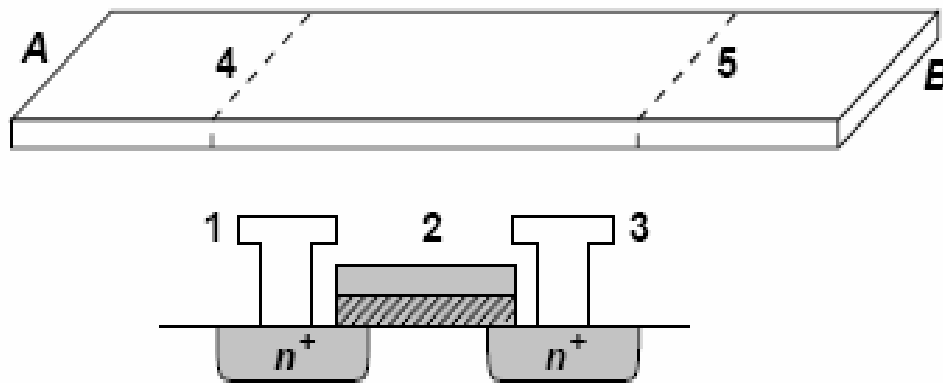
$$C_6 = \frac{\text{Im}\{Y_{11} + Y_{12} + Y_{13}\}}{\omega}$$



# Scalability of Extrinsic Capacitances



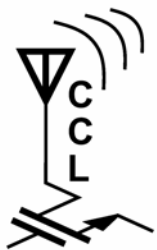
# Extrinsic Interconnects



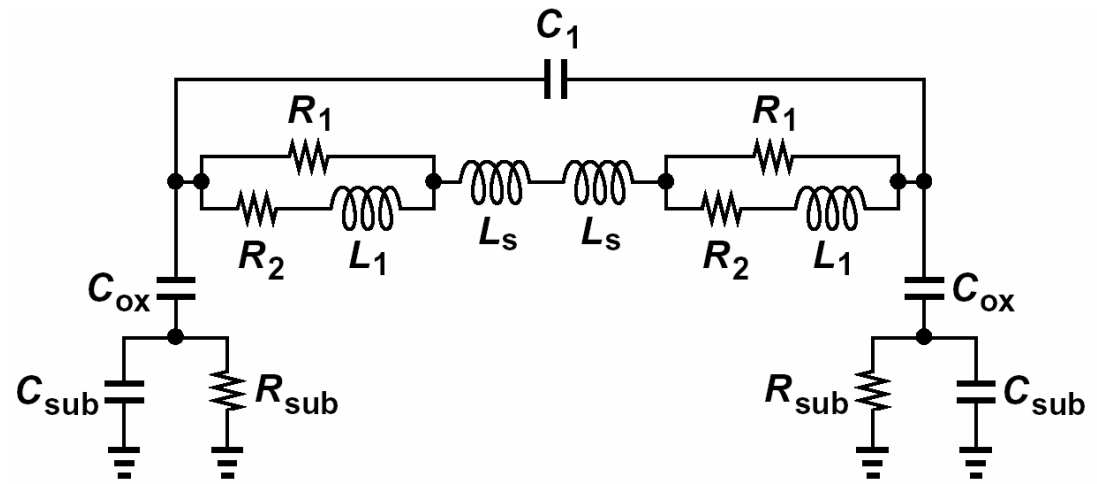
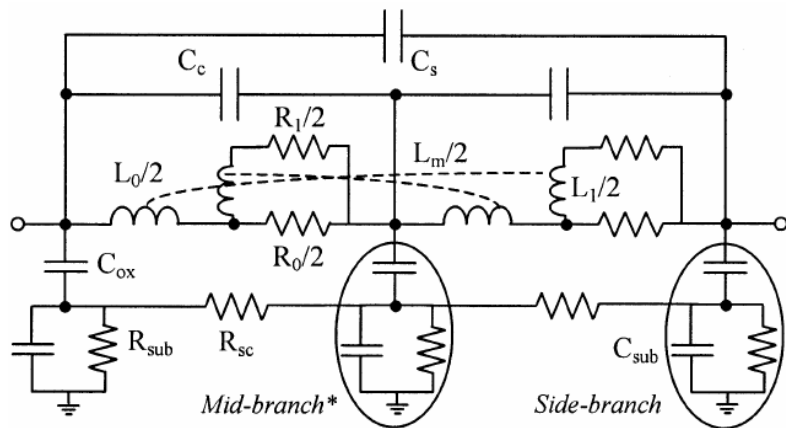
$$C_{14} = \frac{-\text{Im}\{Y_{14}\}}{\omega}$$

$$C_{24} = \frac{-\text{Im}\{Y_{24}\}}{\omega}$$

$$C_{34} = \frac{-\text{Im}\{Y_{34}\}}{\omega}$$

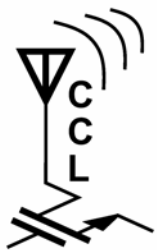


# Inductor Model

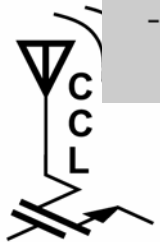
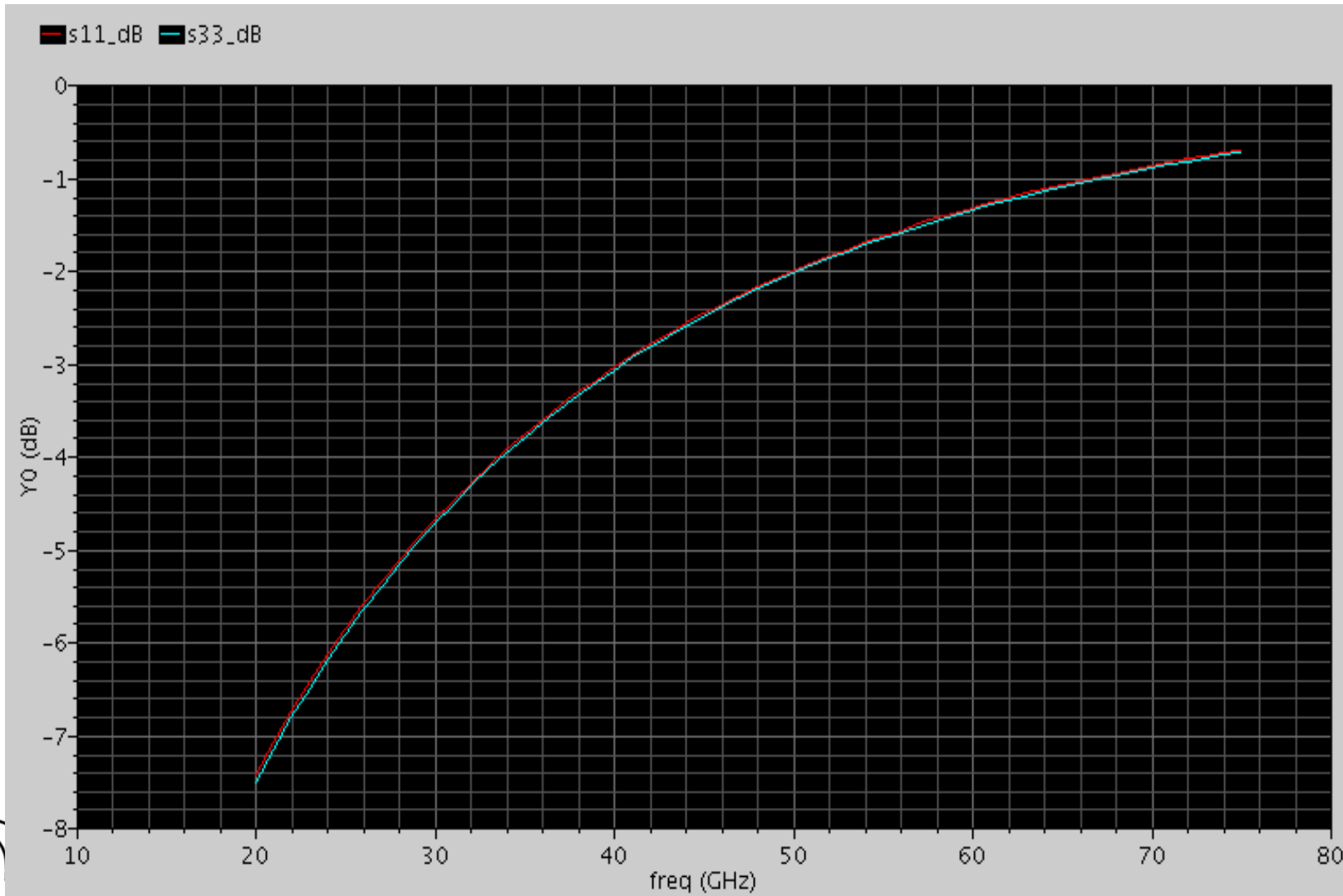


[Cao, JSSC, March03]

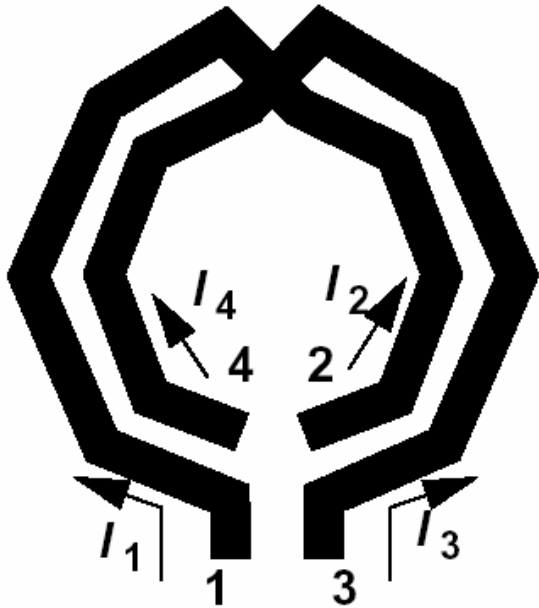
- Lends itself to element-by-element extraction from Y-parameters.



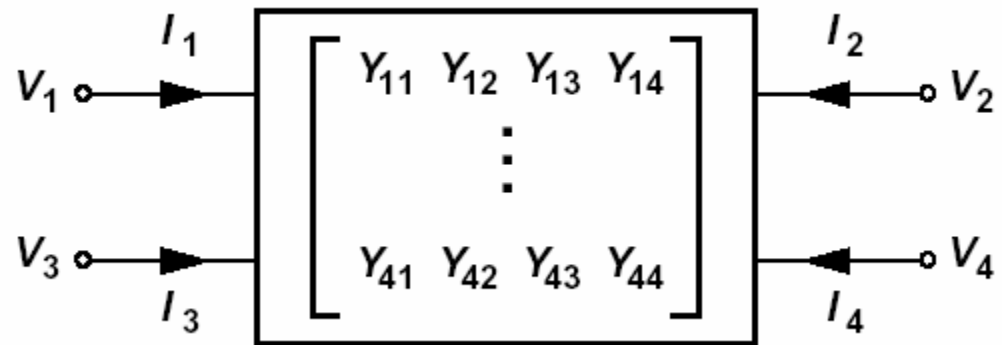
# Fitting Results



# Intertwined Inductors



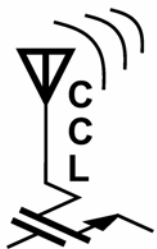
- Mutual coupling reduces area.
- Nodes 1-4 are close to one another.



$$I_1 = Y_{11}V_1 + Y_{12}V_2 + Y_{13}V_3 + Y_{14}V_4$$

⋮

$$I_4 = Y_{41}V_1 + Y_{42}V_2 + Y_{43}V_3 + Y_{44}V_4.$$

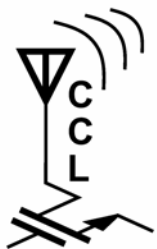
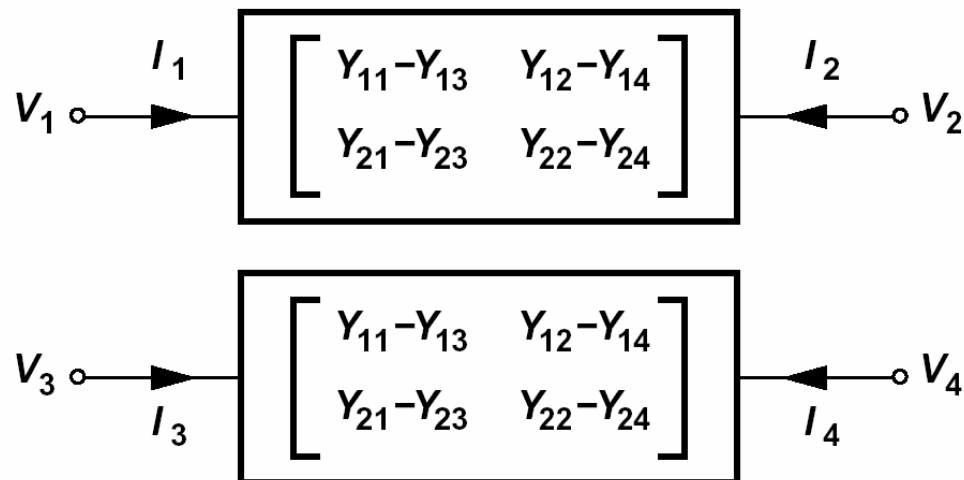


# Effect of Symmetry

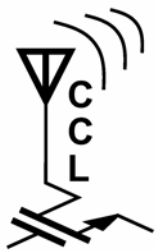
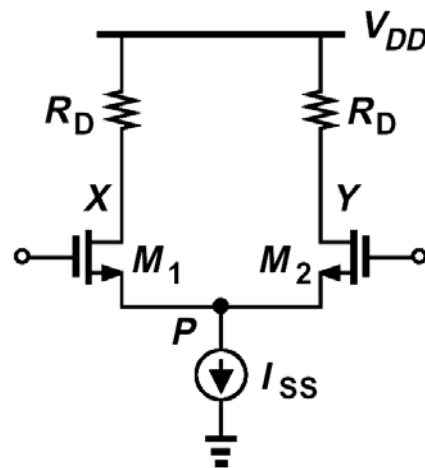
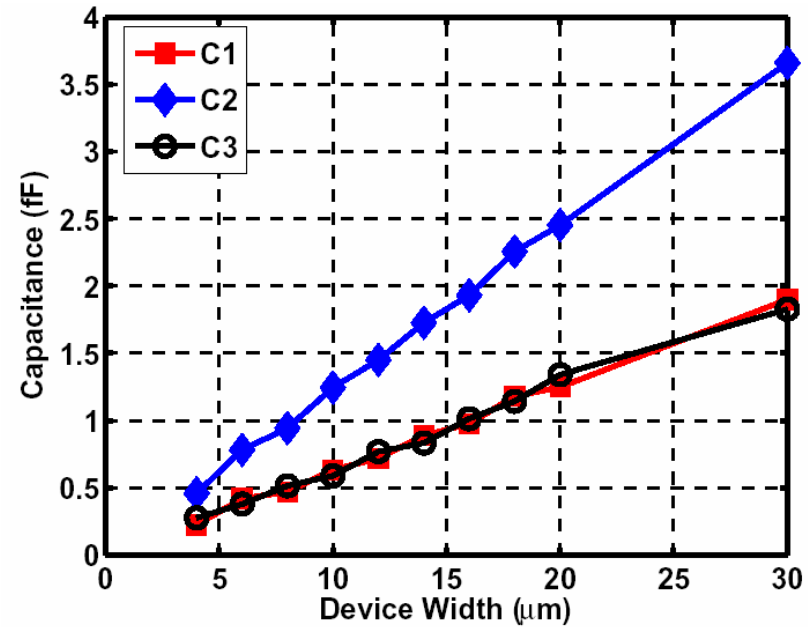
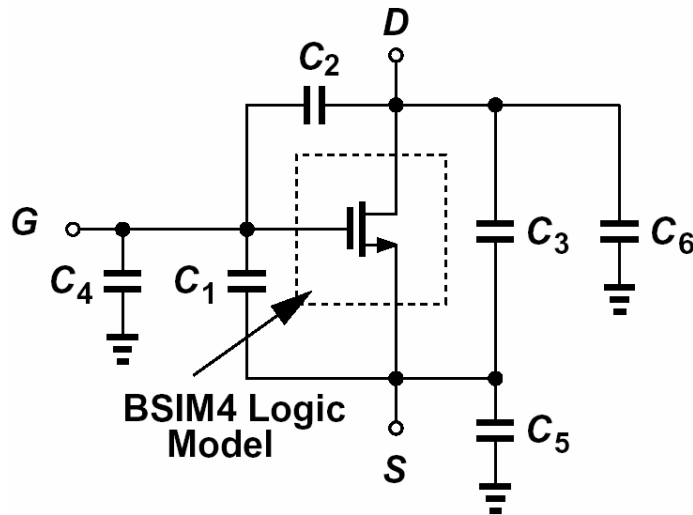
$$V_1 = -V_3, V_2 = -V_4, I_1 = -I_3, \text{ and } I_2 = -I_4$$

$$\begin{aligned} I_1 &= Y_{11}V_1 + Y_{12}V_2 - Y_{13}V_1 - Y_{14}V_2 \\ &= (Y_{11} - Y_{13})V_1 + (Y_{12} - Y_{14})V_2. \end{aligned}$$

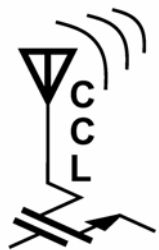
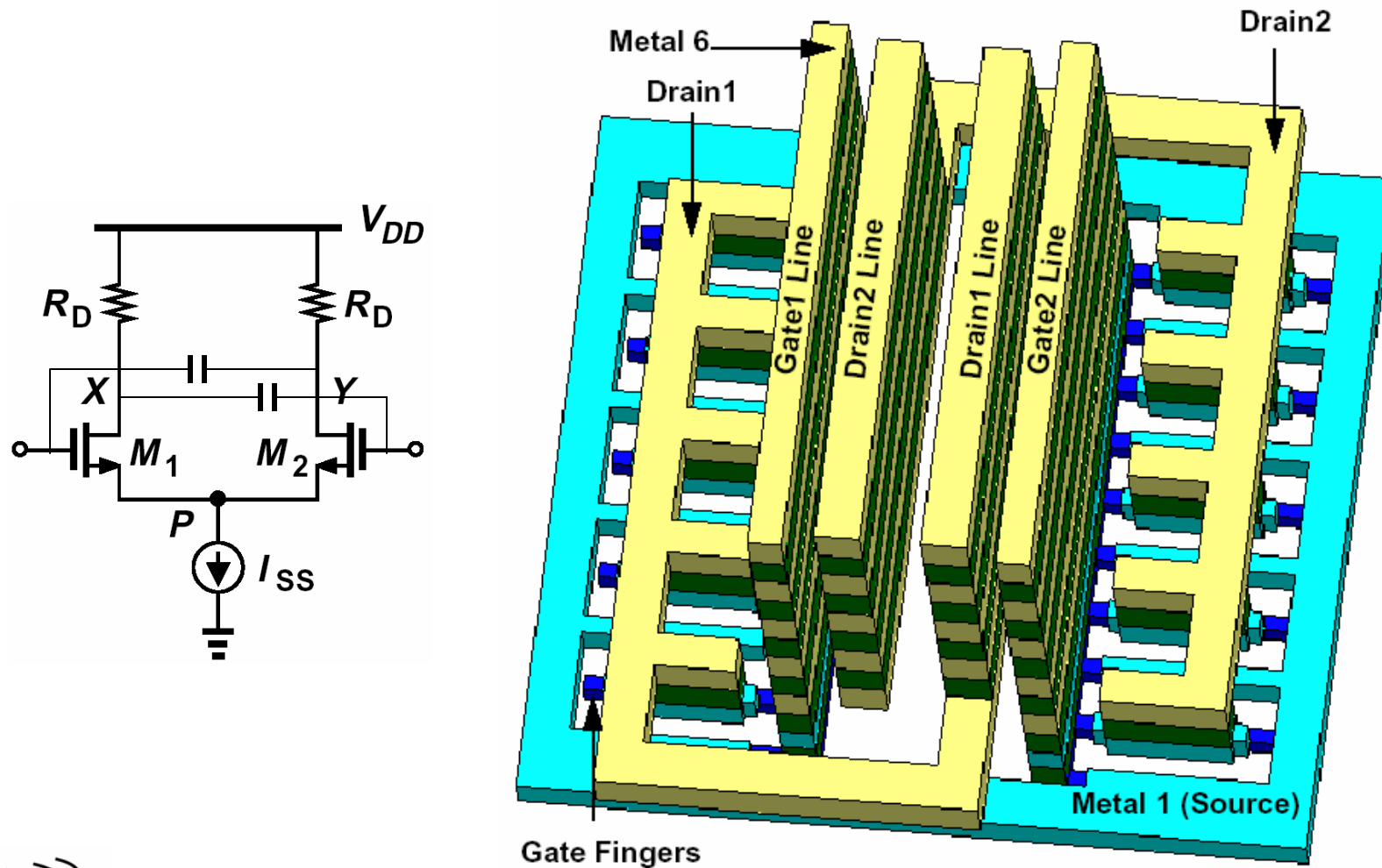
$$\begin{aligned} I_2 &= Y_{21}V_1 + Y_{22}V_2 - Y_{23}V_1 - Y_{24}V_2 \\ &= (Y_{21} - Y_{23})V_1 + (Y_{22} - Y_{24})V_2. \end{aligned}$$



# Effect of $C_{GD,ext}$

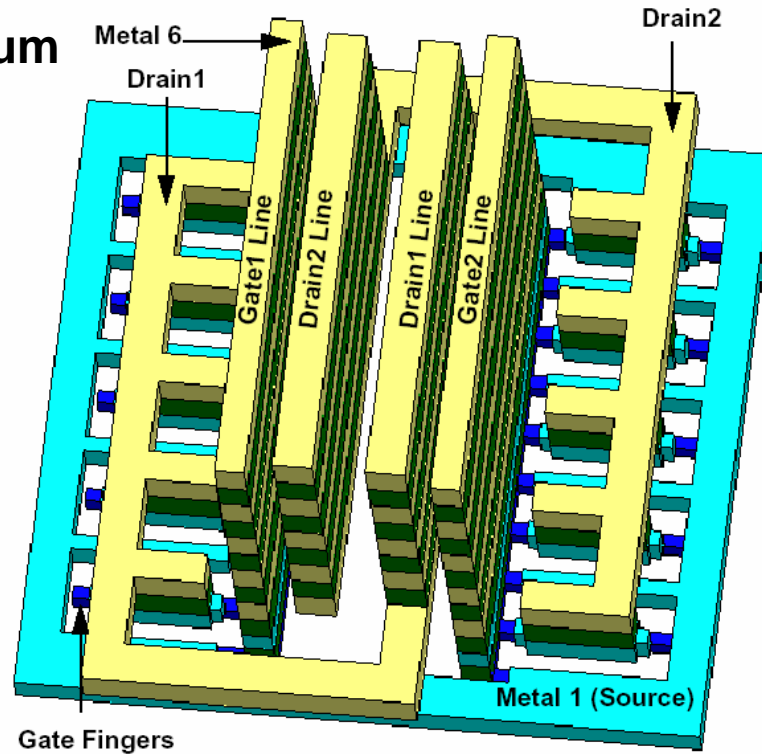


# New Layout Technique



# Capacitances

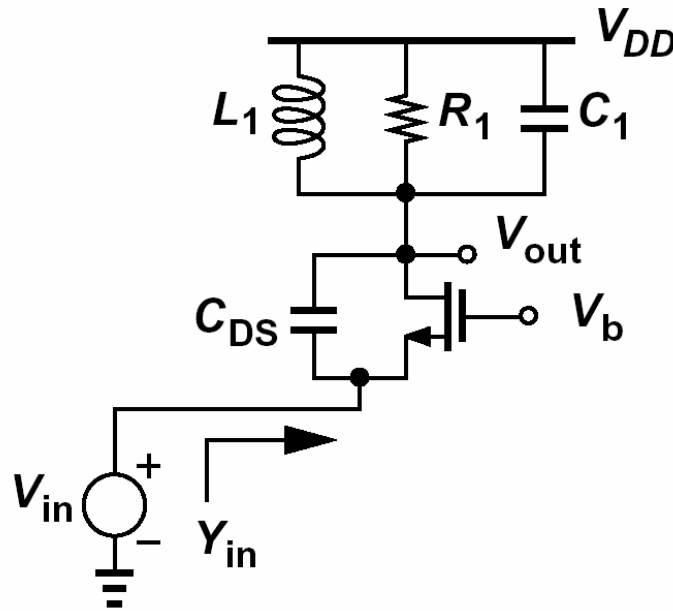
W/L=10x 1um/ 0.1um



(fF)	$C_{GD1}$	$C_{D1D2}$	$C_{D1G2}$	$C_{D2G1}$	$C_{GD2}$	$C_{G1G2}$	$C_{DS1}$	$C_{DS2}$	$C_{GS1}$	$C_{GS2}$
Standard Layout	0.68	0.02	0.032	0.032	0.67	0.98	1.1	1.1	0.62	0.62
Proposed Layout	0.87	1.03	2.01	2.01	0.87	0.09	1.15	1.15	0.67	0.67
Intrinsic Capacitances	2.75				2.75				8.4	8.4



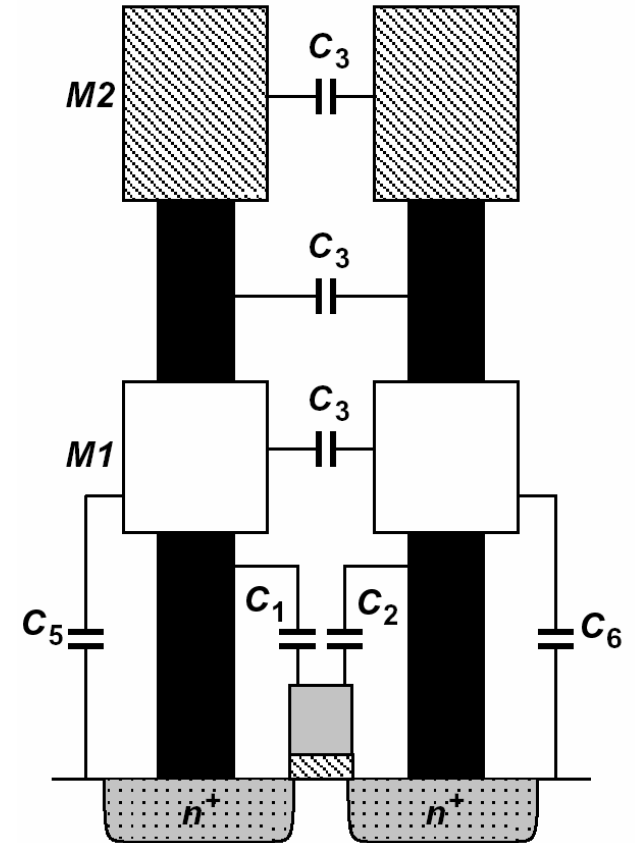
# Another Layout Technique



$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{R_1 L_1 s (g_m + g_{mb} + C_{DS} s)}{R_1 L_1 (C_1 + C_{DS}) s^2 + L_1 s + R_1}$$

$$\omega_o = \frac{1}{\sqrt{L_1 (C_1 + C_{DS})}}$$

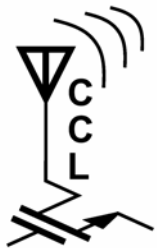
$$Y_{in}(j\omega) \approx (g_m + g_{mb}) + j\omega C_{DS} [1 - R_1 (g_m + g_{mb})]$$



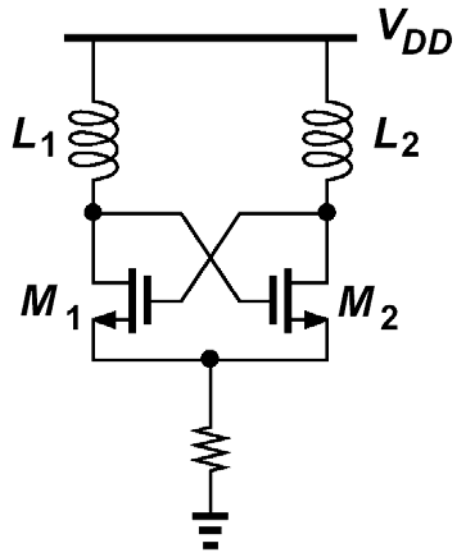
# Experimental Results

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- Among various circuits, only oscillators can be measured easily → Use oscillators to check validity of models.
- Two different oscillator topologies;  
Five oscillator designs from 40 GHz to 130 GHz

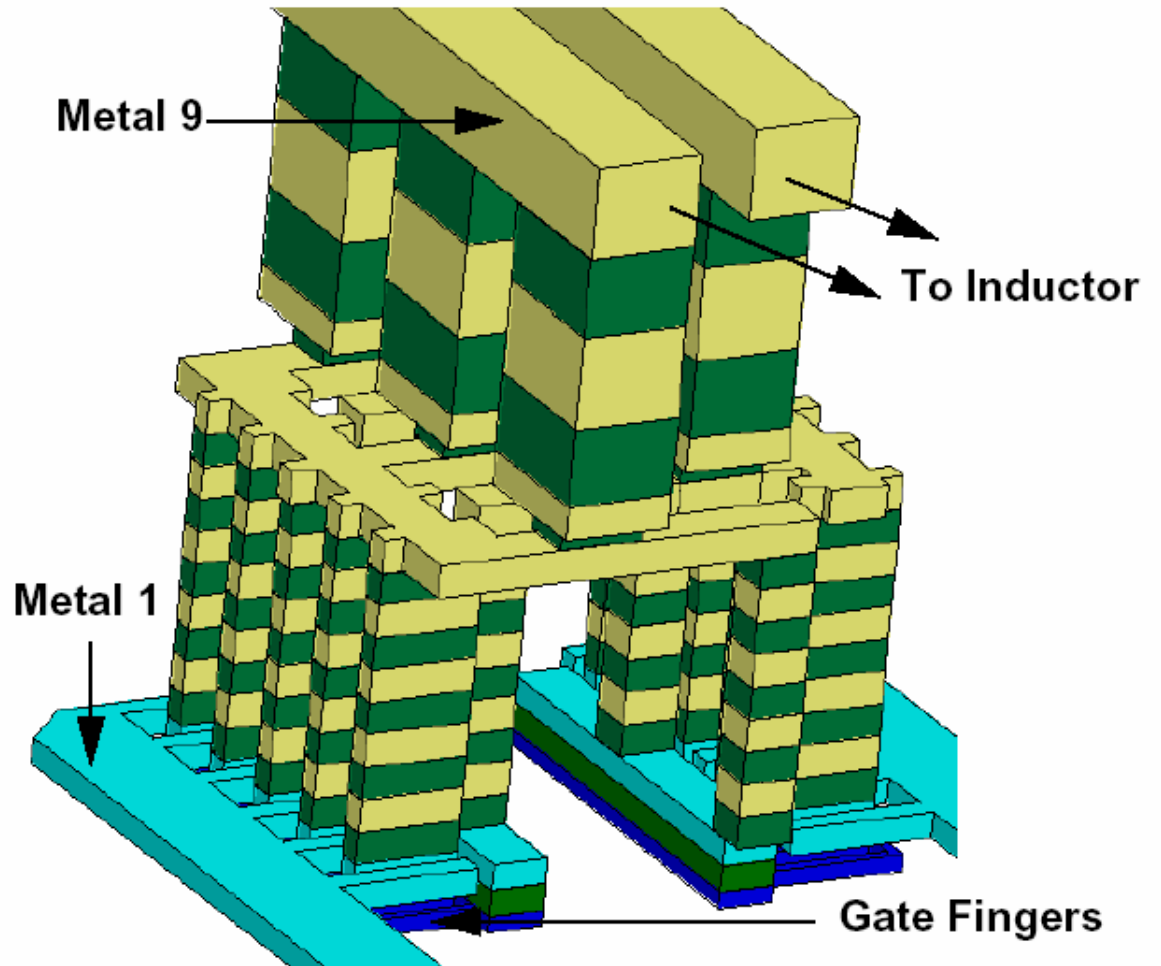


# Oscillator Type I

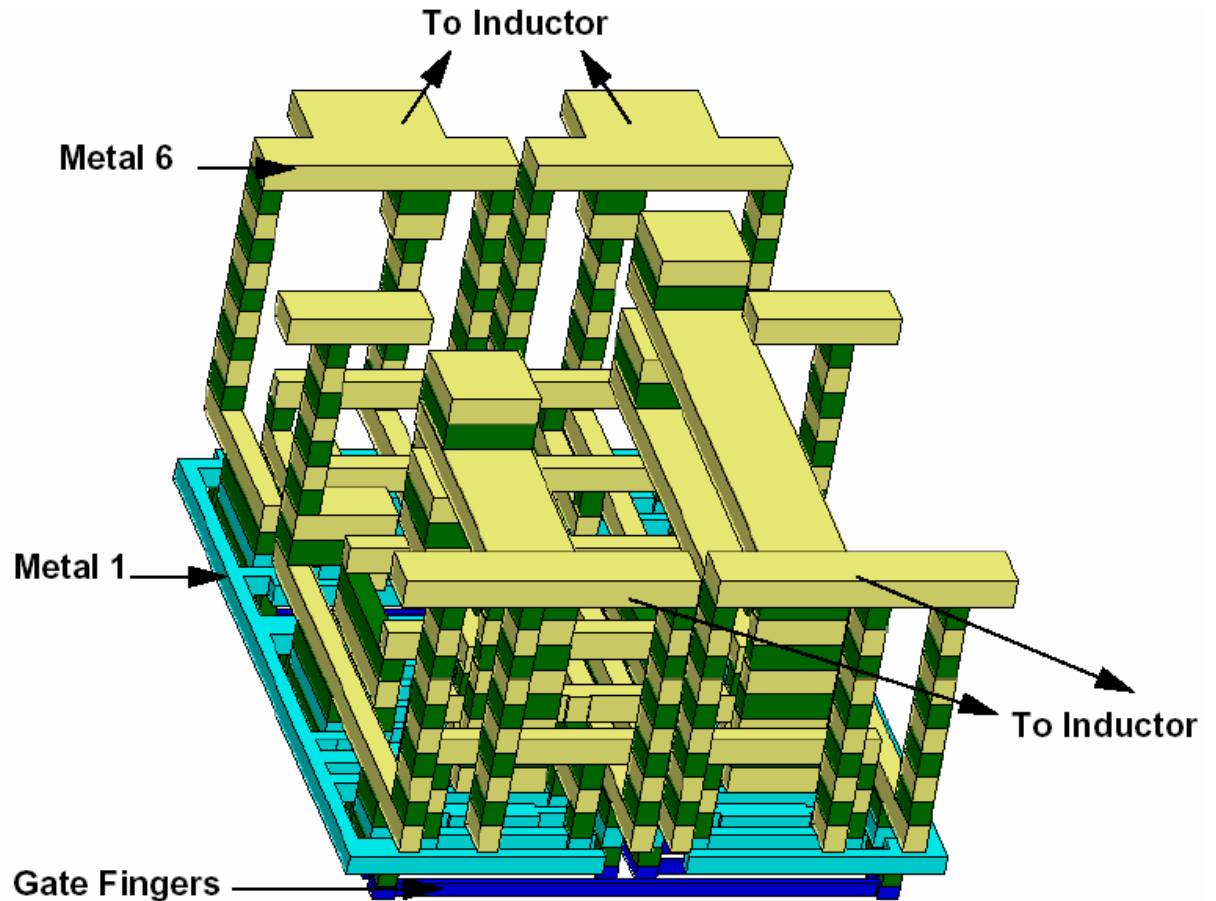
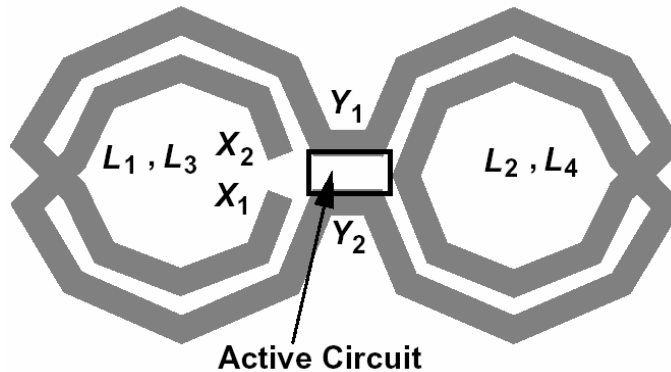
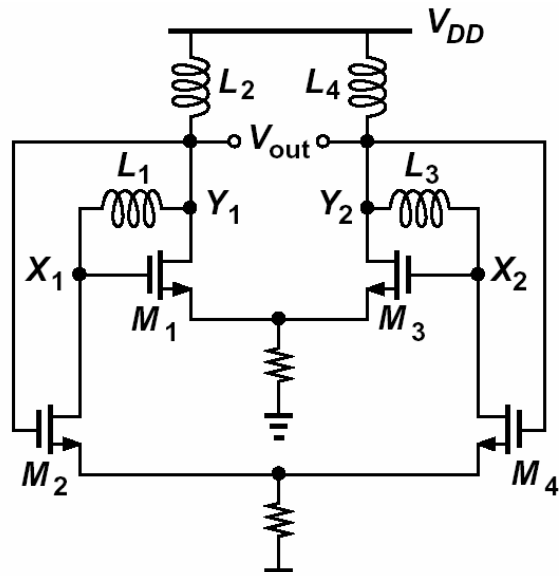


$W=10\text{ }\mu\text{m}$   
(1- $\mu\text{m}$  fingers)

$L_1+L_2=400\text{ pH}, 500\text{ pH}$

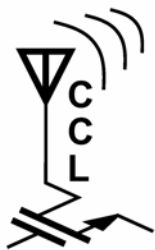


# Oscillator Type II



$W=8 \text{ um}$  (2-um fingers)

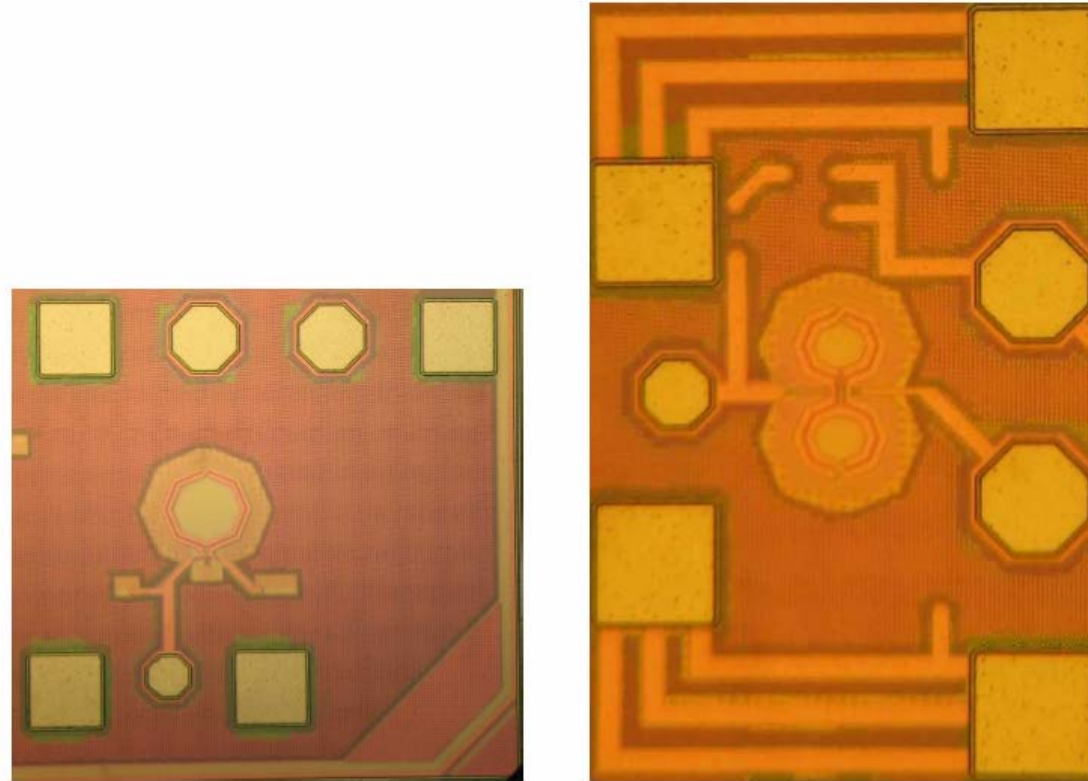
$L_1+L_2=430 \text{ pH}, 270 \text{ pH}, 200\text{pH}$



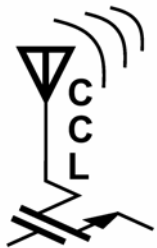
[Razavi, JSSC, March08]

# Die Photos

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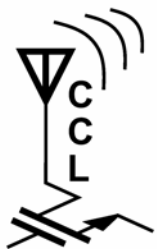
**Fabricated in TMSU's 90-nm Technology**



# Results

	Oscillation Frequency (GHz)				
	Oscillator Type I		Oscillator Type II		
	$L_1 + L_2$		$L_1 + L_3 = L_2 + L_4$		
	500pH	400pH	430pH	270pH	200pH
Measured Frequency	41.5	47.6	83	108	128
Simulation without Parasitics	44.4	50	89.3	125	150
Simulation with Calibre Extraction Tool	42.4	49.5	84.4	118	141
Simulation with S-Parameters	42.0	46.7	84.2	109	131
Simulation with Proposed Model	42.4	47.1	84.6	111	132

- Error is less than 3.2%.
- BSIM4 modeling of intrinsic capacitances of 90-nm device is accurate up to 128 GHz!



# Conclusion

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- **A systematic approach to modeling is proposed that provides insight and accuracy.**
- **The confidence afforded by the modeling leads to new layout techniques.**
- **Models predict oscillator frequencies with 3.2% error from 40 GHz to 130 GHz.**



# Acknowledgement

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- We are indebted to TSMC for chip fabrication.
- This work was supported by Realtek Semiconductor and Skyworks, Inc.

