UCLA Annual Research Review 2009

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Linear Analysis of Random Process Variability

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Motivation

- **Sources: Random dopant fluctuations, LER, quantum effects, oxide thickness variations**
- **Impact: Identically designed devices do not have the same performance**
  - Large spread in power and timing of digital circuits
  - Non-functioning analog blocks
- **Simulation Methods:**
  - Digital
    - Statistical timing analysis tool
  - Analog
    - Monte Carlo (MC) simulation, 1000+ points
    - Worst-case analysis
- **Time inefficient, little intuition**

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Designers need faster and more intuitive analysis methods

Outline

- **Variability Current Noise Source**
  - Model Derivation
- **Linear Analysis Noise Method**
  - Berkeley Spice Tool
  - Design Example
- **Conclusion**

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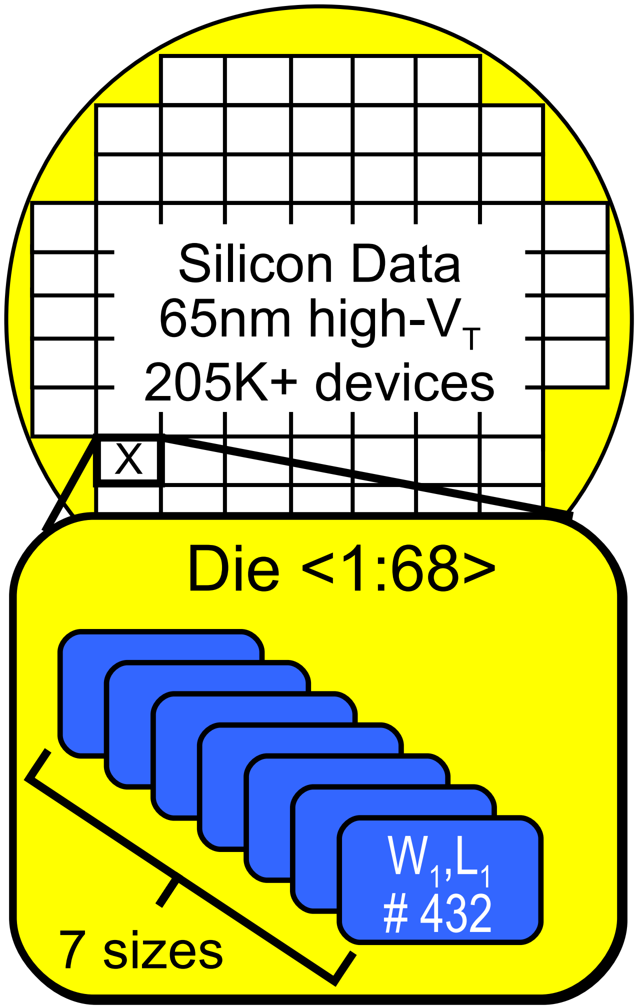
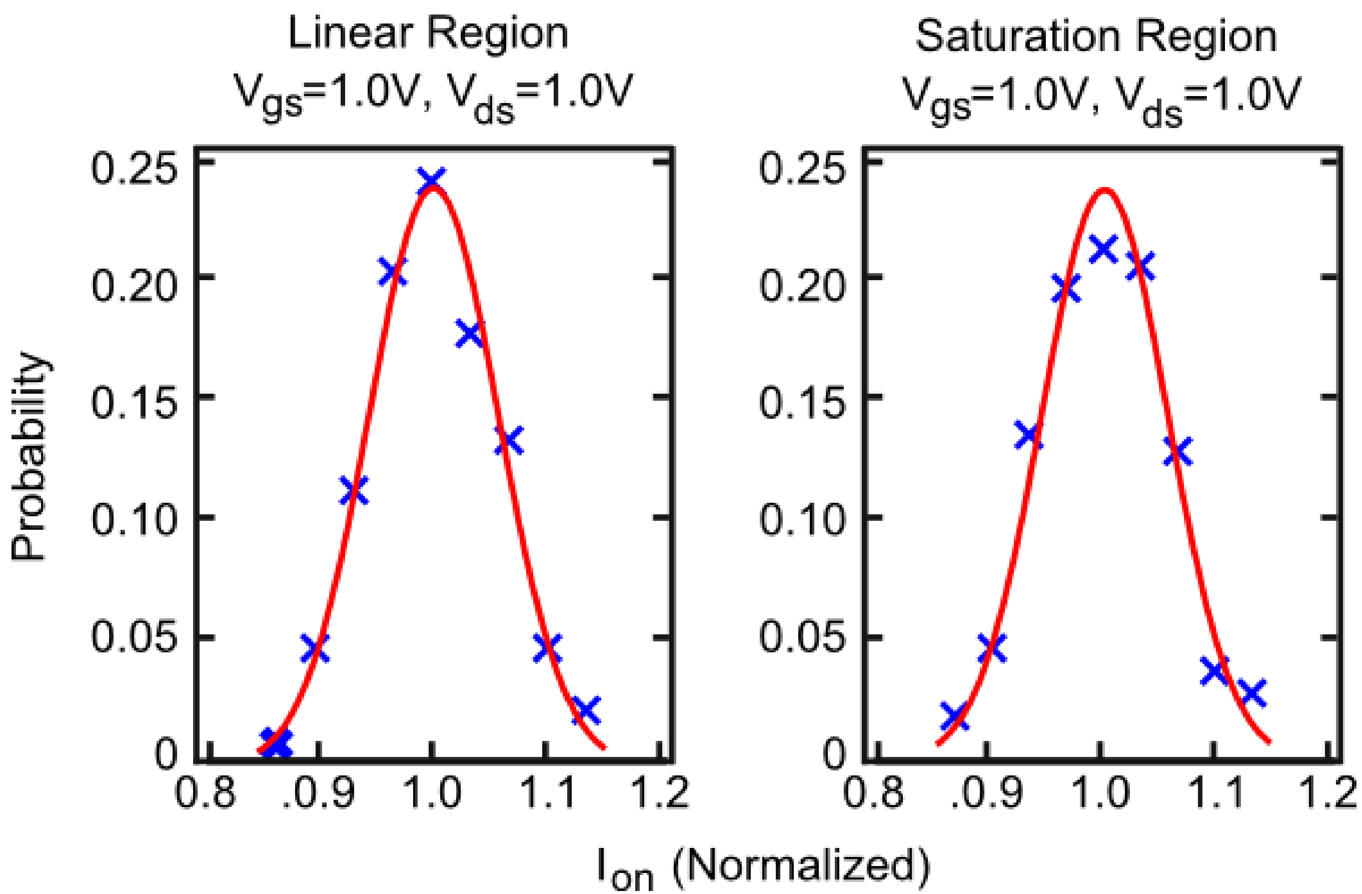
Variability Noise Model Derivation



- **Our approach**
  - Forget about curve fitting and start with the most accurate data provided: current measurements
  - Develop models for current variation with respect to actual design variables: W, L and operating points (V_{gs}, V_{ds})
- **Measured data**
  - 68 dies measured across a single wafer
  - Measured transistors vary in width from 120-500 nm and length from 60-150 nm
  - There are 7 unique W,L combinations
  - Complete I-V curves were measured for 432 devices per W,L combination per die

Current Distribution is Gaussian

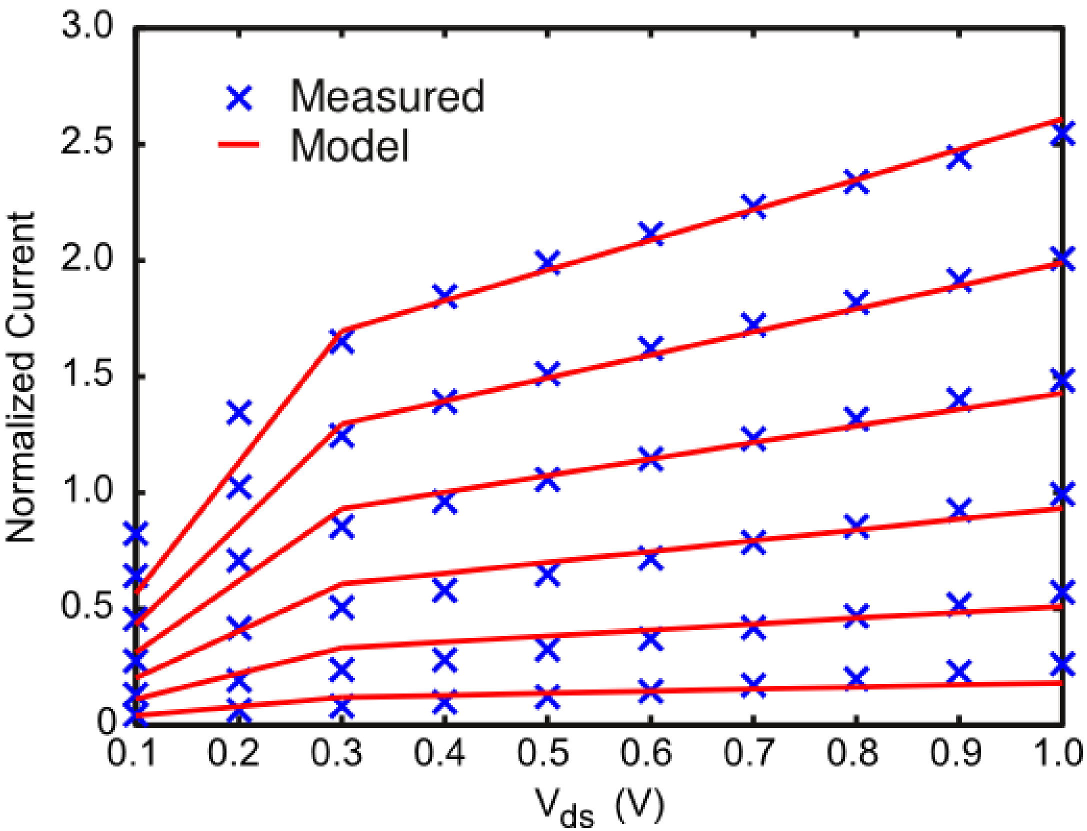


- χ^2 test for all 205K+ measured devices over all operating points has > 5% probability in the tails. Likely that current distribution is a Gaussian distribution.

Modeling Average Current, $I_{avg} = \mu(I_{on})$

- **Modified α-power law model**

$$I_{avg} = \begin{cases} C_{on} \cdot \frac{W}{L} \cdot (V_{gs} - V_{TH})^{\alpha} \cdot (1 + \lambda V_{ds}) & \text{saturation} \\ C_{on} \cdot \frac{W}{L} \cdot (V_{gs} - V_{TH})^{\alpha} \cdot V_{ds}/V_{DO} & \text{linear} \end{cases}$$



- I_{avg} can be fit to any appropriate model

RMS error, this model

- 10.5% (V_{ds} > 0.3V)
- 23.7% (V_{ds} < 0.3V)

Modeling Current Standard Deviation

- **Traditional equations**

$$\sigma^2_{\frac{\Delta I_{on}}{I_{avg}}} = \sum_i \left(\frac{1}{I_{avg}} \frac{\partial I_{avg}}{\partial P_i} \right)^2 \sigma^2_{P_i}$$

$$\sigma^2_{P_i} = \frac{A_1}{WL} + \frac{A_2}{WL^2} + \frac{A_3}{W^2L} + \frac{A_4}{W^2L^2}$$

- **Downside to traditional equations**
  - Dependence on process parameter P_i implies that the designer has very little control over the variability
  - Too many fitting variables (A_i)
  - Operating point dependence (V_{gs}, V_{ds}) not considered

- **Can we find a simpler form?**
  - Model dependent only on design variables (W,L,V_{gs},V_{ds})?

Principal Component Analysis (PCA)

- **PCA is the best orthogonal transformation for data with Gaussian noise**
  - Variables: Measured current at each operating point
  - Each transistor measurement is a unique instance

- **Our approach**
  - Normalize data by subtracting I_{avg}, then divide by I_{avg}
  - PCA shows that for every transistor size > 98% of the current variation can be described by the first principal component vector

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For a fixed (W,L):

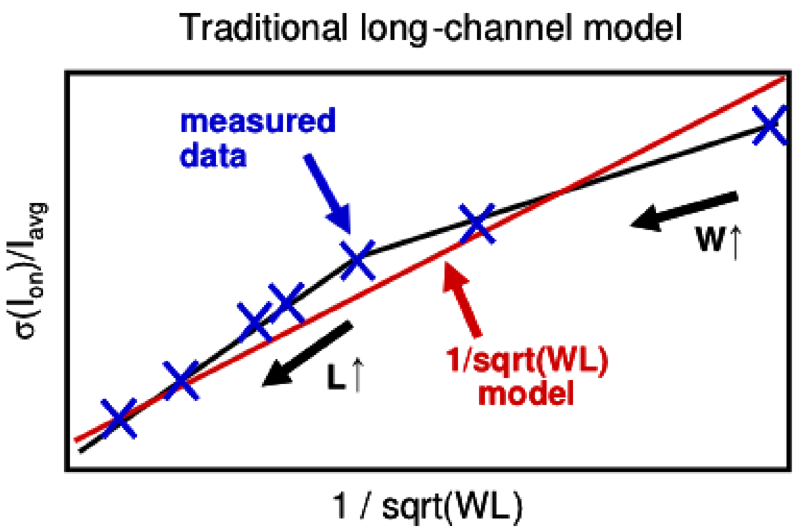
$$pdf(I_{on}) = N(1, \sigma_{\frac{\Delta I_{on}}{I_{avg}}}) \cdot I_{avg}$$

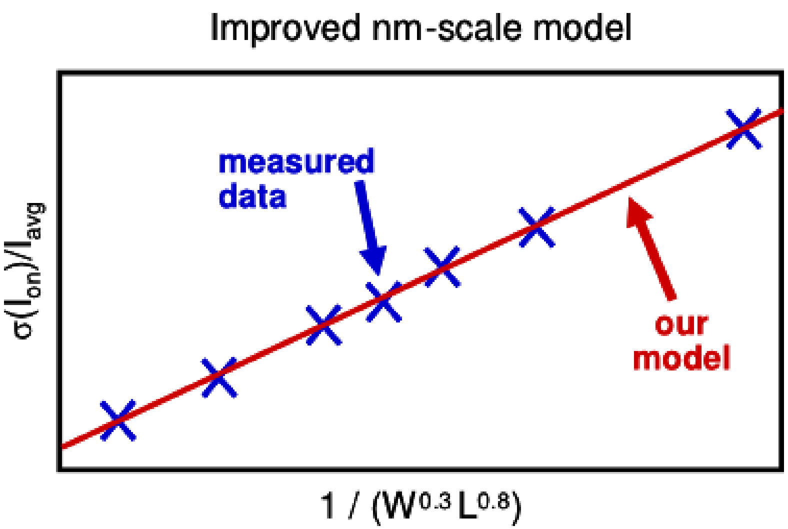
$$pdf(I_{on}) = pdf((1 + a_1 \cdot PC_1) \cdot I_{avg})$$

$$\Rightarrow \quad \sigma_{\frac{\Delta I_{on}}{I_{avg}}} = \sigma_{a_1} \cdot PC_1$$

Size Dependence of $\sigma(\Delta I_{on})$

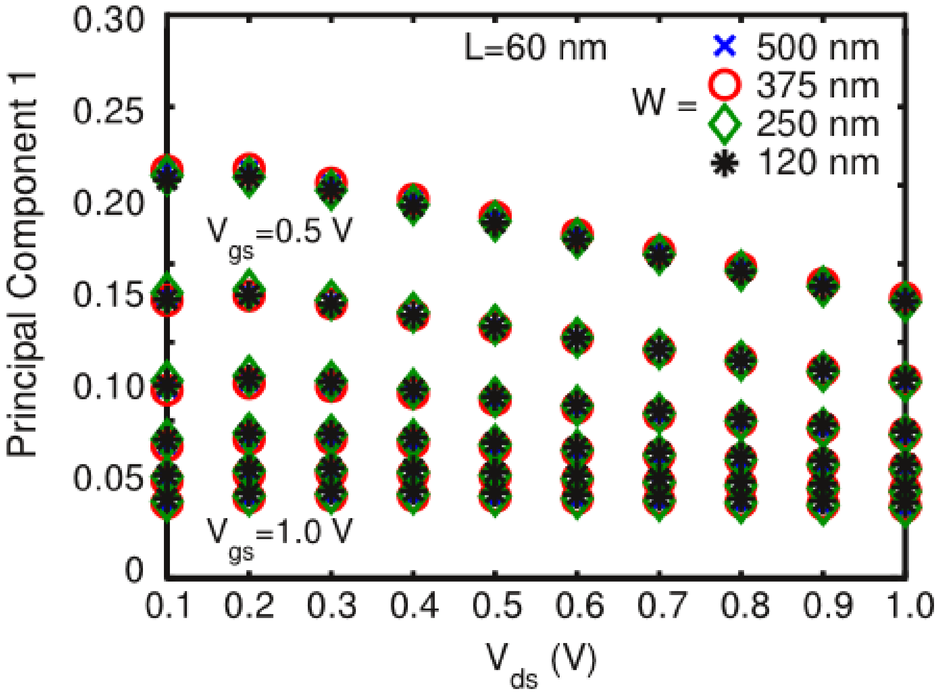
Operating point: $V_{gs} = V_{ds} = 1V$

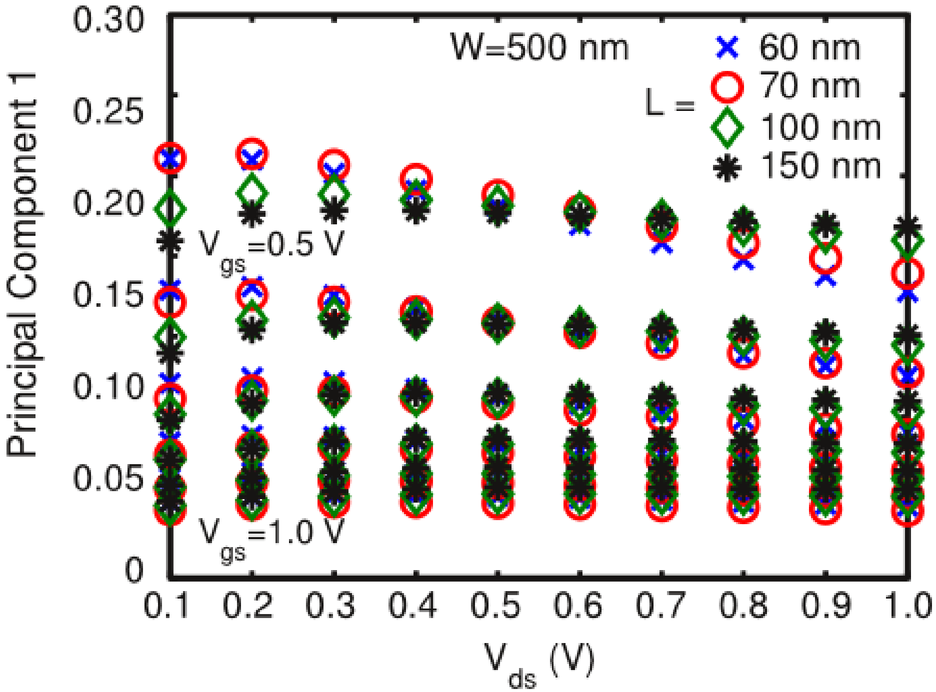




- **Plot σ_{a1} for different transistor sizes**
- **What to take away?**
  - There is a much stronger dependence on L than on W
  - $1/W^{0.3}L^{0.8}$ holds for short-L and long-L devices

Operating Point Dependence

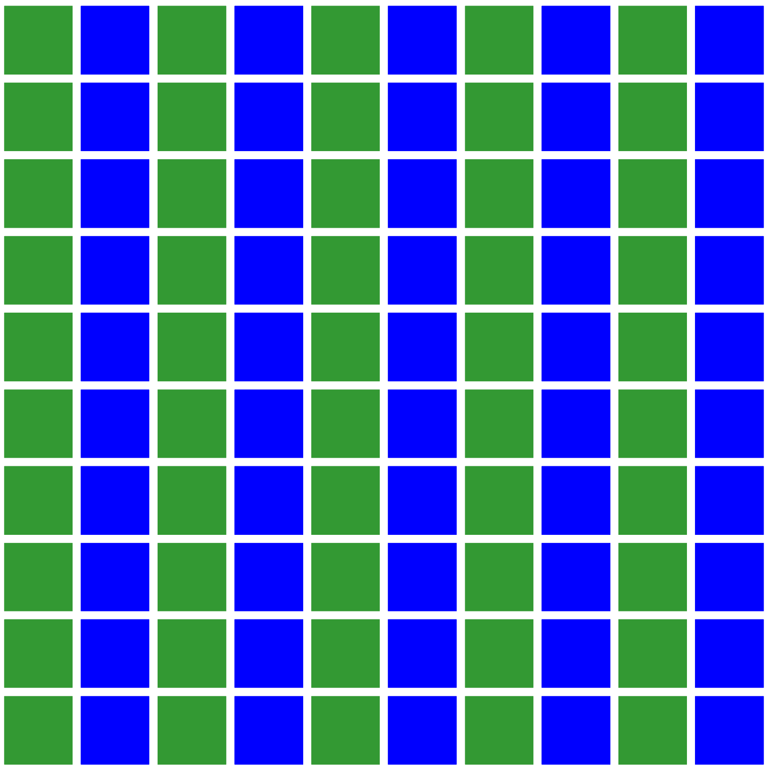




- Transistors w/ fixed L and varying W have the same PC
- V_{ds} dependence on $\sigma(\Delta I_{on})/\mu(I_{on})$ is independent of W
- Transistors w/ fixed W and varying L have different PC
- V_{ds} dependence on $\sigma(\Delta I_{on})/\mu(I_{on})$ is dependent on L

Is the Variability Independent?

Transistor grid



Set A: Transistors of size W_1,L_1

Set B: Transistors of size W_2,L_2

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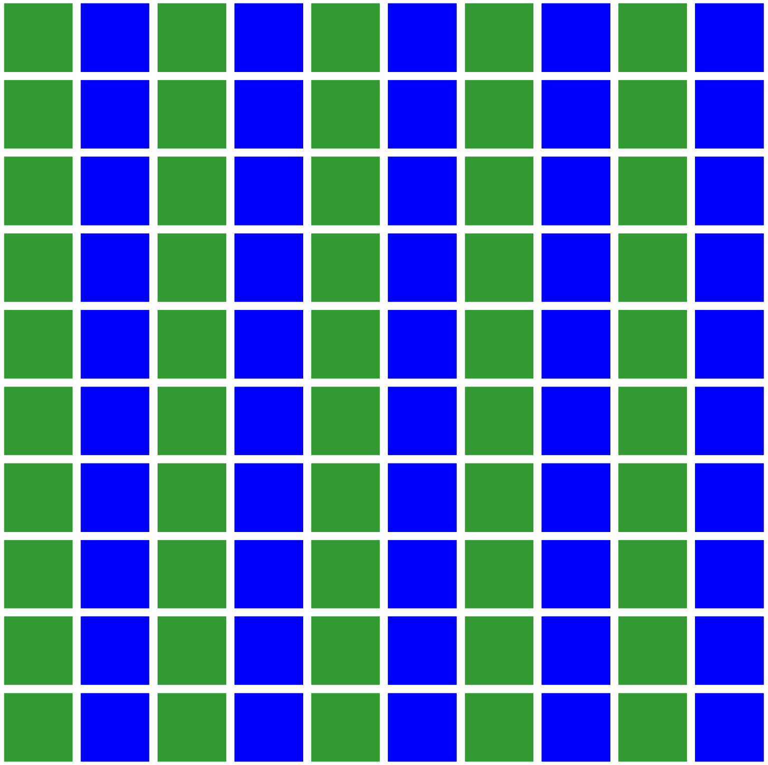

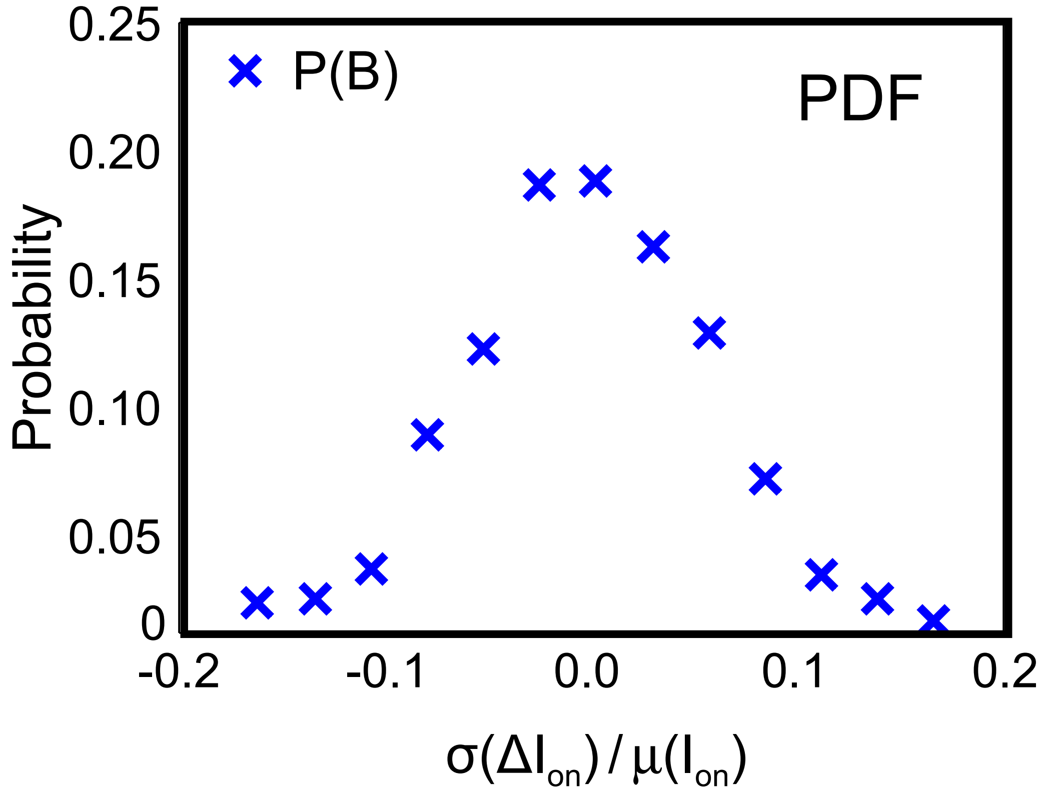

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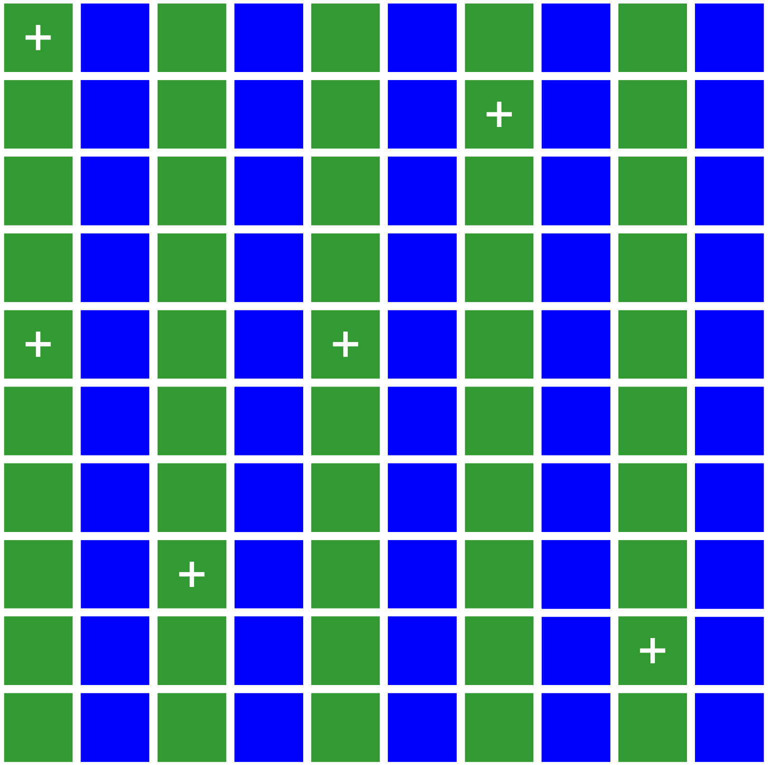
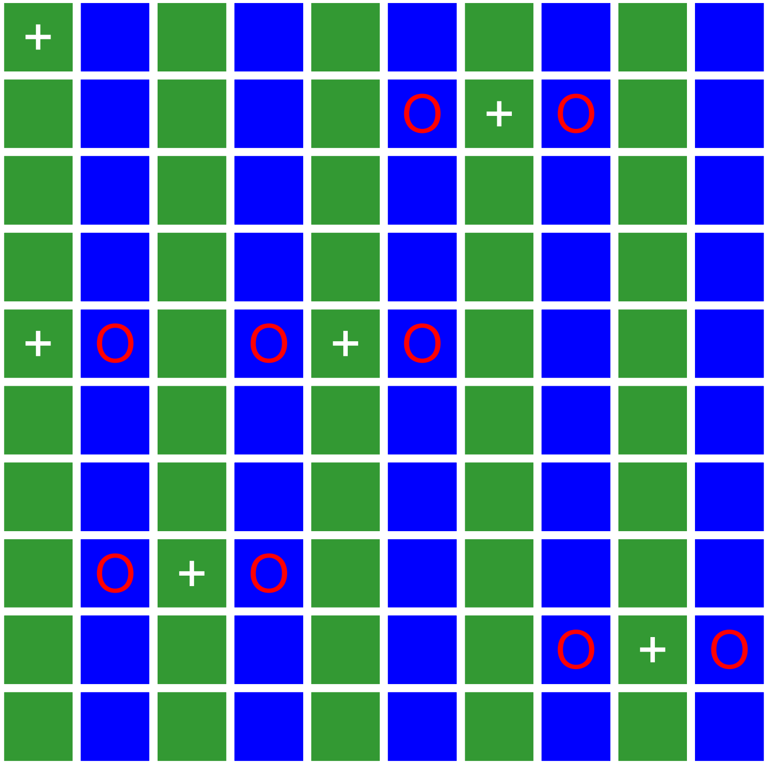


+ A devices with $I_{on} = I_{avg} + \sigma$

Is the Variability Independent?

Transistor grid



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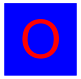

B devices distance d=1 from +

Is the Variability Independent?

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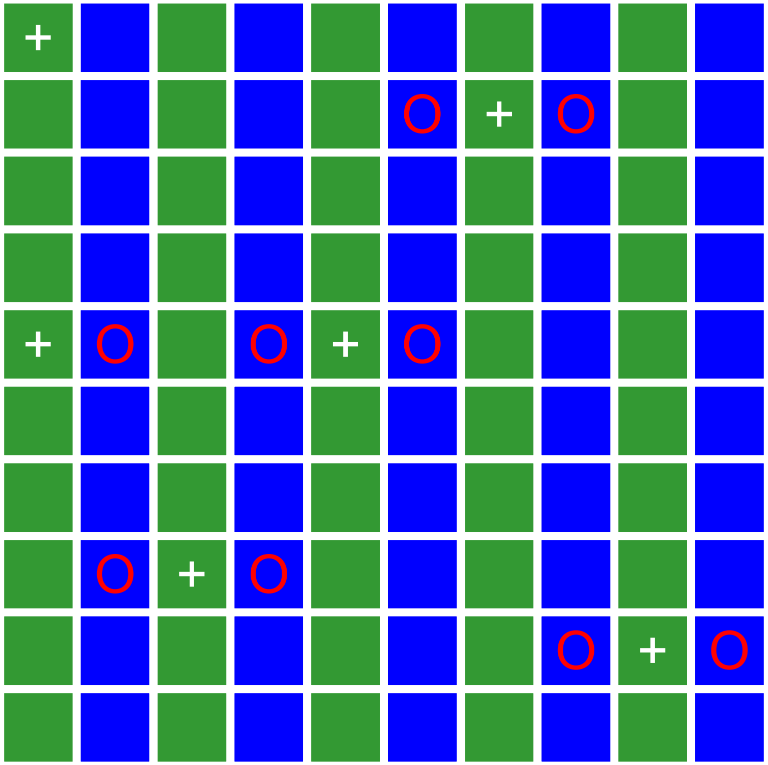

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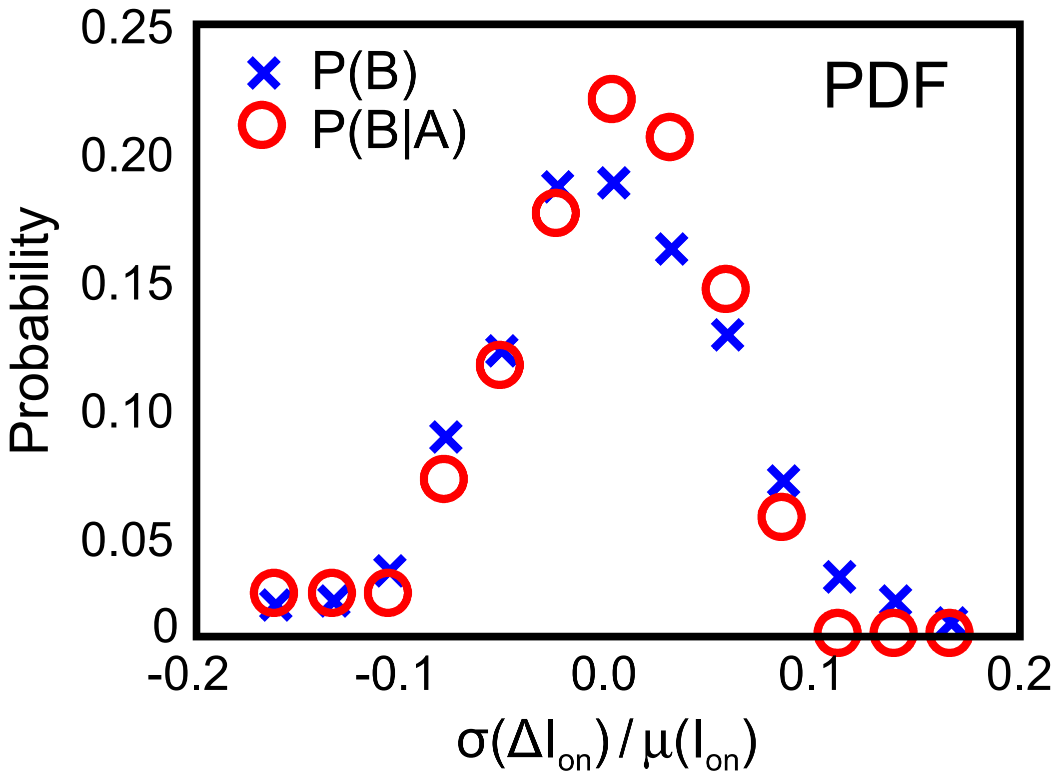


Data Analysis:

$P(A,B) = P(B|A) \times P(A)$

$P(B|A) = P(B)$ [from plot]

$P(A,B) = P(A) \times P(B)$

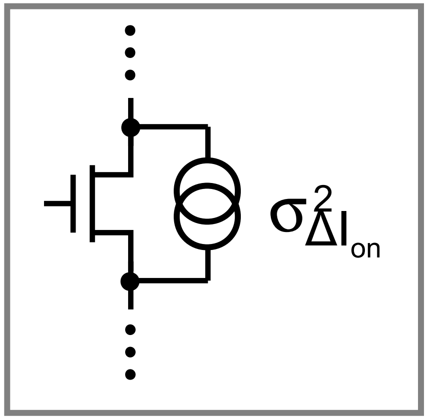
Model for Current Standard Deviation

$$\sigma(\Delta I_{on}) / \mu(I_{on}) = \frac{A}{W^{\alpha} L^{\beta} V_{gs}^{\eta} V_{ds}^{\zeta}}$$

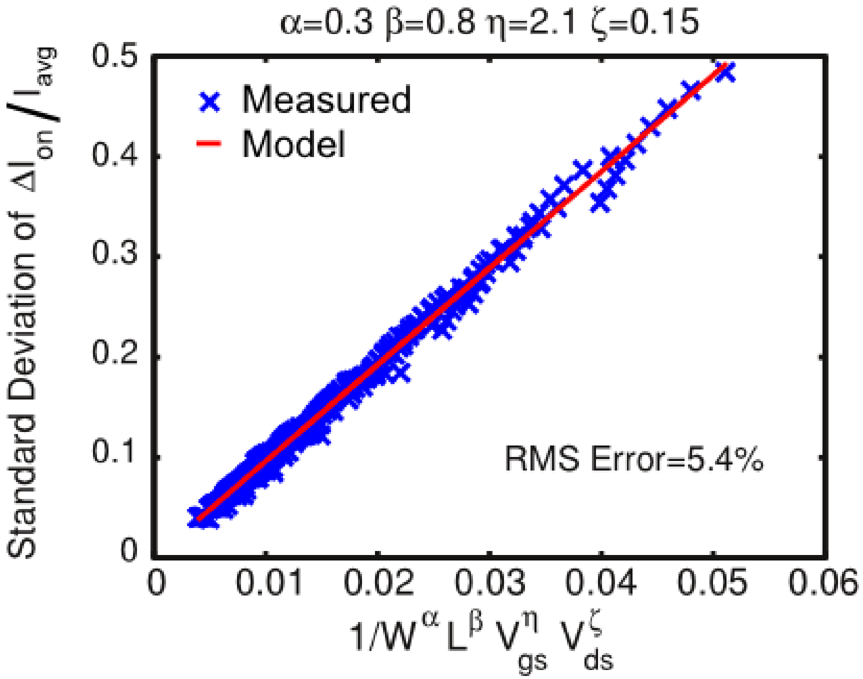
$\alpha = 0.3$ $\eta = 2.1$

$\beta = 0.8$ $\zeta = 0.15$

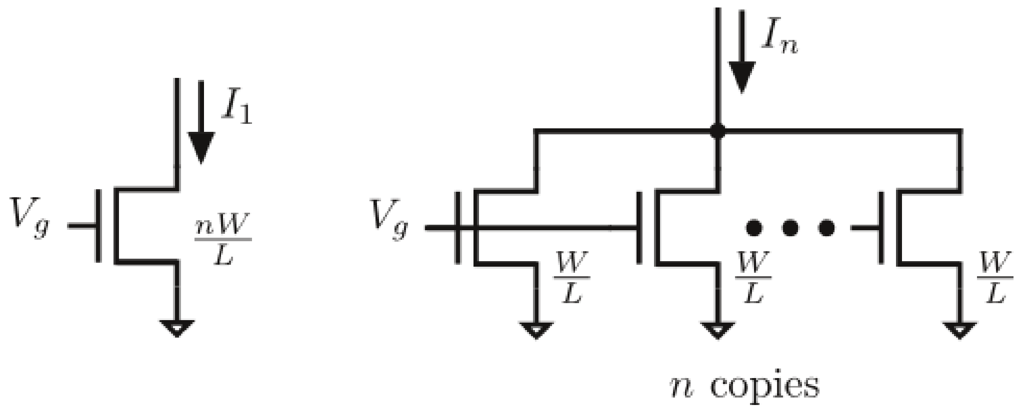
Size (α, β) Bias (η, ζ)



Var. noise model



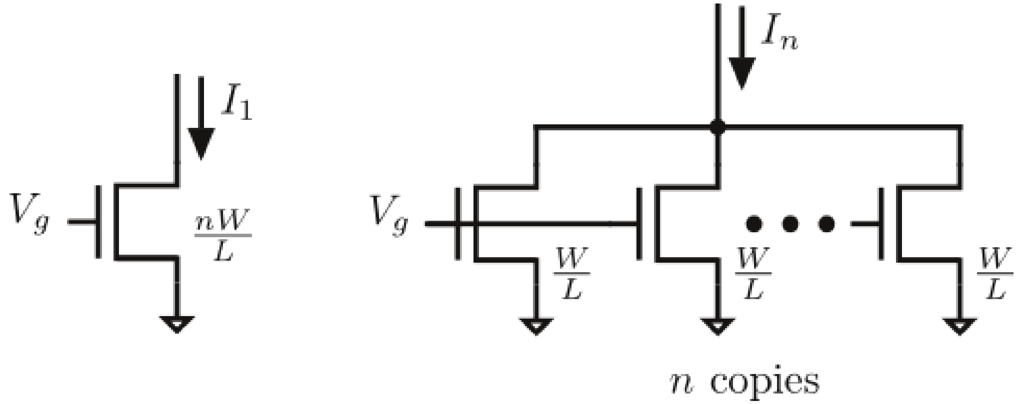
Current Sources: Fixed Length



- Variance calculations

$$\sigma_{I_1}^2 = (I_{avg})^2 \left(\frac{A}{(nW)^\alpha L^\beta V_{gs}^\eta V_{ds}^\zeta} \right)^2$$

Current Sources: Fixed Length



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$$\sigma^2_{I_1} = (I_{avg})^2 \left(\frac{A}{(nW)^\alpha L^\beta V_{gs}^\eta V_{ds}^\zeta} \right)^2$$

$$\sigma^2_{I_n} = \sum_{i=1}^{n} \left(\frac{I_{avg}}{n} \right)^2 \left(\frac{A}{W^\alpha L^\beta V_{gs}^\eta V_{ds}^\zeta} \right)^2$$

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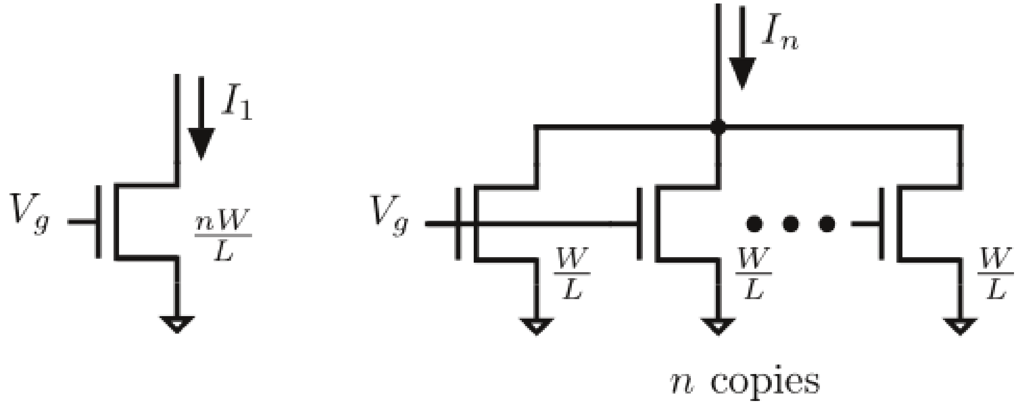


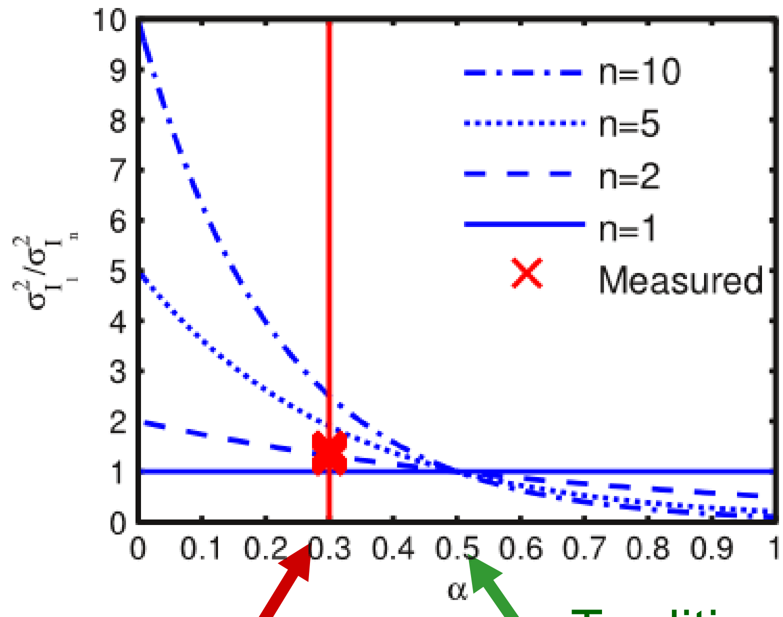
Fingered devices have less variation for tech w/ α < 0.5

- Variance calculations

$$\sigma_{I_1}^2 = (I_{avg})^2 \left(\frac{A}{(nW)^\alpha L^\beta V_{gs}^\eta V_{ds}^\zeta} \right)^2$$

$$\sigma_{I_n}^2 = \sum_{i=1}^{n} \left(\frac{I_{avg}}{n} \right)^2 \left(\frac{A}{W^\alpha L^\beta V_{gs}^\eta V_{ds}^\zeta} \right)^2$$

$$\Rightarrow \boxed{\sigma_{I_1}^2 / \sigma_{I_n}^2 = n^{(1-2\alpha)}}$$



Measured silicon α = 0.3

Traditional 1/sqrt(WL) formula

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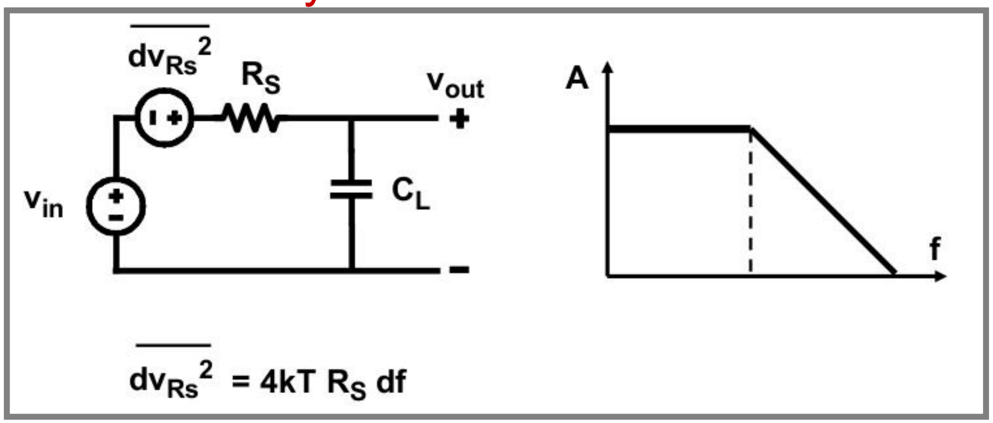
Proposed Variability Noise Model

- **Idea: Leverage electrical noise analysis methods**

Noise analysis of resistor thermal noise



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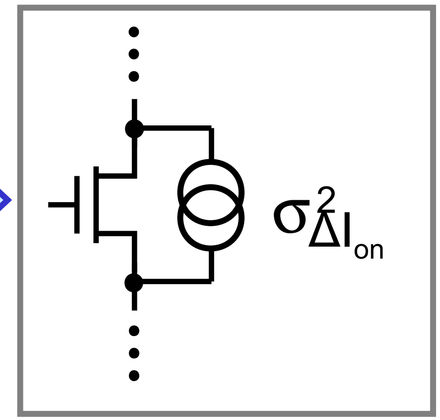
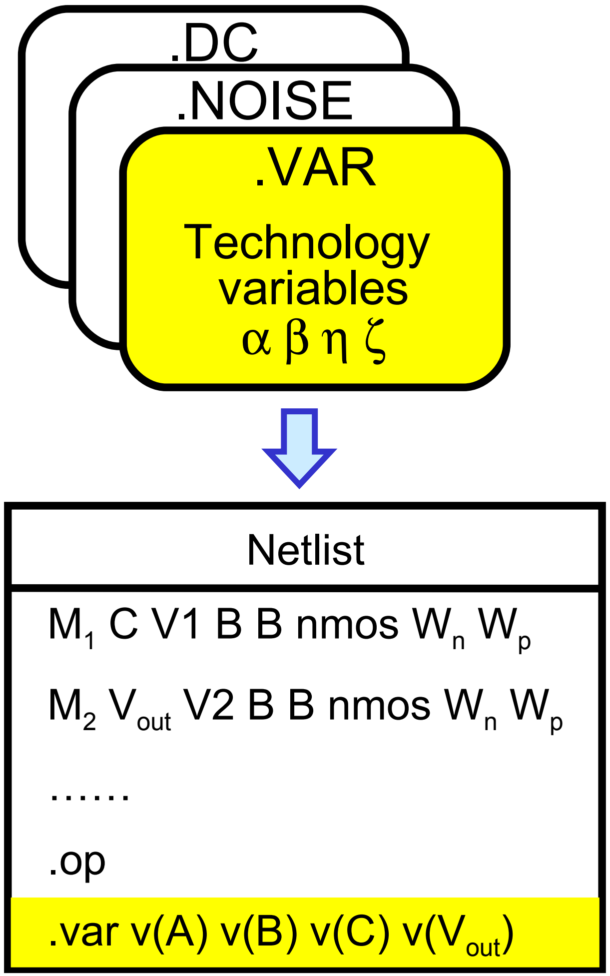
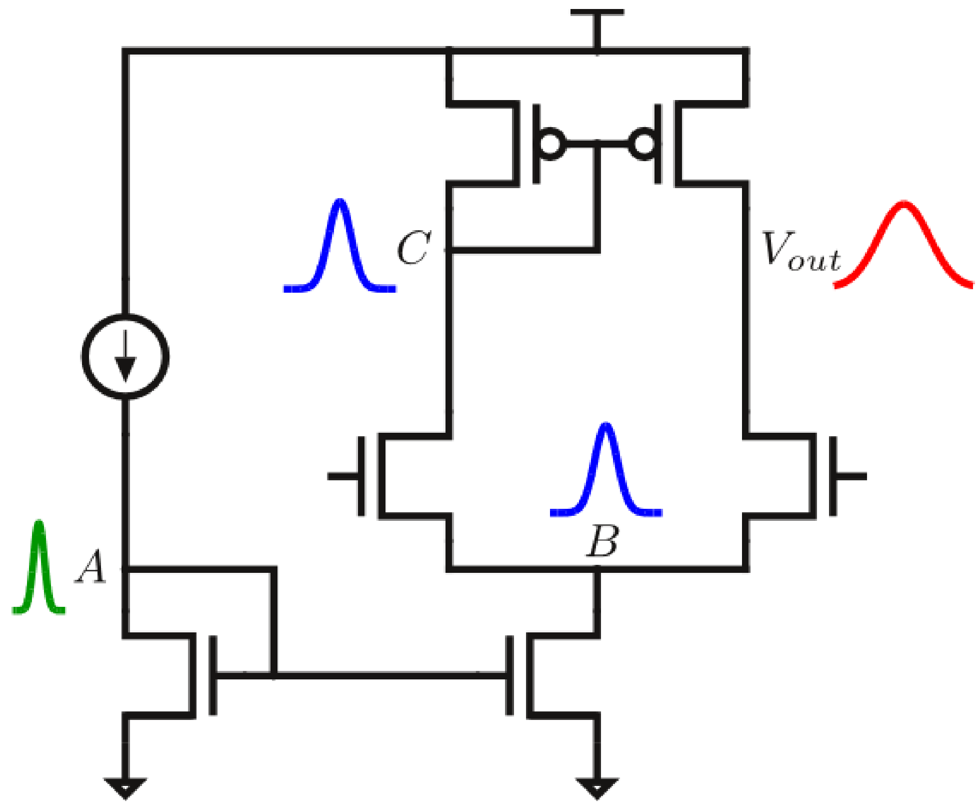


- **Model requirements:**
  – Describe RPV as a shunt current source
  – Good accuracy
  – Function of design variables for more intuition

Variability SPICE Tool

- Implemented for Berkeley SPICE
- Can be easily integrated into any simulation tool





Conclusion

- **An alternative method to Monte Carlo has been provided for computing spatial circuit variance due to RPV**
  - An analysis card for Berkeley SPICE has been written to provide this variability noise analysis functionality
  - Single simulation linear analysis improves design efficiency without sacrificing accuracy

- **Future Work:**
  - Dynamic method to linearize the circuit so that this approach is also applicable for large RMS values
  - Examine additional circuit examples