23.8 A 40Gb/s 14mW CMOS Wireline Receiver

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Reaching a power efficiency of 1mW/Gb/s has proven difficult for wireline transceivers operating at tens of gigabits per second. At 40Gb/s, recent receivers consume from 150mW [1] to 1W [2]. This paper describes a receiver that achieves a tenfold reduction in power and an efficiency of 0.35mW/Gb/s.

The proposed receiver uses a "minimalist" approach, which recognizes that every additional stage in the data or clock path consumes more power *and* limits the bandwidth. The minimalist mentality avoids multiple stages in the front-end continuous-time linear equalizer (CTLE), quadrature oscillators in the clock and data recovery (CDR) circuit, clock or data buffers, or phase interpolation. Moreover, building blocks are shared among different functions so as to reduce the number of current paths between V_{DD} and ground. Using charge-steering techniques extensively, the receiver contains only a few static bias currents adding up to about 6mA. The minimalist approach also leads to a small footprint, about 110×175μm^2, for the entire receiver, making it possible to design a multi-lane system in a small area and with short interconnects.

Figure 23.8.1 conceptually depicts the receiver architecture, where overlapping boundaries indicate hardware sharing between the functions. The receiver consists of a CTLE, a CDR circuit, a decision-feedback equalizer (DFE), a discrete-time linear equalizer (DTLE), and a deserializer. Employing a single differential pair, the CTLE consumes 2mW but provides only 5.5dB of boost at the Nyquist rate; another 5.4dB is created by the DTLE at a cost of 0.3mW [3]. The CDR runs at half rate and shares latches with the DFE and the deserializer. The CDR output clock frequency is also divided by 2 to generate the 10GHz quadrature phases necessary for the second-rank latches in the DFE and the deserializer. Figure 23.8.1 exemplifies how minimalist design produces "growing" returns. The compact architecture contains no high-speed data interconnects longer than 25μm, avoiding the need for buffers, inductive peaking (except for the CTLE), etc.

While our three principles of minimalist design, charge steering, and hardware sharing in Fig. 23.8.1 are attractive for a tenfold reduction in power, they also present their own challenges: (a) full-rate operation becomes very difficult; (b) half-rate operation doubles the load capacitance that the CDR and DFE present to the CTLE; (c) the merged CDR/DFE topology in [1] cannot operate with charge steering or without quadrature oscillator phases; (d) the bufferless VCO frequency shifts if the DFE is turned off during lock acquisition, and (e) the CDR phase detector (PD) cannot be placed after the (charge-steering) DFE summer because the summer output is precharged to V_{DD} for half of the clock cycle. These considerations require that the receiver be specifically architected to accommodate our three design principles.

The fifth issue, namely, the return-to-zero nature of the summer output, complicates hardware sharing between the CDR and the DFE. Noting that a half-rate charge-steering phase detector must take three samples of the full-rate data by means of six latches [4], we seek interfaces within the DFE that can provide such samples. The proposed circuit is shown in Fig. 23.8.2, where the blocks in gray belong to the DFE. For half-rate operation, $DMUX_1$ and the summing circuits also operate as sampling elements. Thus, only two more latches, L_a and L_b, are necessary for unambiguous phase detection. As shown in Fig. 23.8.2, the XOR of D_{odd} and D_{even} provides the phase error information, V_{err}, between the full-rate data and the 20GHz clock but with dependence on the data pattern. On the other hand, the XOR of samples X_1, X_2, Y_1, and Y_2 generates a fixed-width reference pulse on V_{ref} for every data transition, eliminating the data dependence from the final output, I_{out}. Note that the G_m stage measures the areas under V_{err} and V_{ref} and need not operate at high speeds.

The PD topology of Fig. 23.8.2 faces an issue arising from the limited boost factor of the CTLE. Since a lossy channel yields heavily attenuated 1010 swings in D_{odd} and D_{even}, and since $DMUX_1$ must be sufficiently linear for the equalization operation, XOR_3 can produce an output inconsistent with those of XOR_1 and XOR_2, which are driven by large data swings. To resolve this difficulty, two limiters realized as single differential pairs precede XOR_3. Owing to the voltage gain provided by $DMUX_1$ (≈6dB), each differential pair can act as a limiting amplifier at 20Gb/s with a tail current of 0.2mA.

Figure 23.8.3 shows the proposed half-rate/quarter-rate CDR and DFE details. Highlighted in gray, the CDR loop consists of $DMUX_1$, the summers, latches L_a and L_b, the XOR gates, the loop filter and the VCO. The DFE comprises $DMUX_1$, the summers and the feedback taps formed by $DMUX_{2,3}$ and $MUX_{1\text{-}4}$. The DTLE injects delayed and scaled copies of D_{odd} and D_{even} into the summers, realizing a transfer function given by $1 - \alpha z^{-1}$ and hence a boost factor of $(1 + \alpha)/(1 - \alpha)$ [3].

The intertwined CDR and DFE loops in Fig. 23.8.3 can fight and fail to converge. The operation thus begins by setting the DFE and DTLE tap coefficients to zero and the CTLE boost factor to its maximum value. The gray path detects the phase error between the data and the VCO output, delivering a proportional current to the loop filter and driving the oscillator toward 20GHz. Despite the heavy intersymbol interference at the CTLE output, the CDR locks because data patterns having several consecutive ONEs or ZEROs make full transitions and provide sufficient phase information. Moreover, with about 10.6dB of voltage gain through $DMUX_1$ and the limiters, the transitions presented to XOR_3 become sharp enough to produce proper phase error. The CDR takes approximately 100ns to lock, after which the CTLE boost and the DFE and DTLE tap coefficients are adapted to complete the equalization. (In this prototype, the adaptation is done manually through a serial bus.) Note that the adaptation negligibly alters the phase of the CDR loop as V_{err} is computed outside the DFE feedback loops.

The DFE in Fig. 23.8.3 demultiplexes the half-rate data at X_1 (or Y_1) by another factor of 2 using L_1-L_4 (or L_5-L_8), multiplexes the results and injects a fraction thereof into the summers, thus realizing the first and second feedback taps. Interestingly, the data eyes at X_1 and Y_1 are nearly closed during the initial lock acquisition but open up after the adaptation is completed.

The CDR loop bandwidth can be varied from 4MHz to 20MHz by means of programmable loop filter components. It is desirable to maximize the bandwidth so as to both suppress the VCO phase noise and improve the jitter tolerance, but the upper bound is dictated by the data-dependent jitter resulting from the ripple on the control voltage. With a 20MHz bandwidth, this jitter is still negligible compared to the VCO contribution.

The overall receiver is fabricated in TSMC 45nm digital CMOS technology and tested with a 1V supply on a probe station. Figure 23.8.7 shows the die photograph. Of the total power of 14mW, 2mW are consumed by the CTLE, 5.3mW by the PD, the summers, the DTLE, and the latches, 2.8mW by the VCO, 3.4mW by the divide-by-2 circuit, and 0.53mW by the RZ-NRZ conversion stages in the 10Gb/s data paths. All measurements have been carried out with a channel loss of 18.6dB at Nyquist with a PRBS length of 2^7–1.

Figure 23.8.4 shows the measured channel output, the recovered data eye and the spectrum and waveform of the recovered clock. The 20GHz clock exhibits an rms jitter of 1.3ps. Figure 23.8.5 plots the measured jitter transfer and tolerance for three different CDR loop bandwidths, revealing a tolerance as high as 0.45UI at 5MHz. Also plotted is the measured equalizer bathtub curve (with no CDR action and with an external clock). It is important to note that the PRBS generator and the external clock contribute about 8ps$_{pp}$ in this measurement.

Figure 23.8.6 summarizes the performance of our prototype and compares it with that of the state of the art.

Acknowledgments:
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References:

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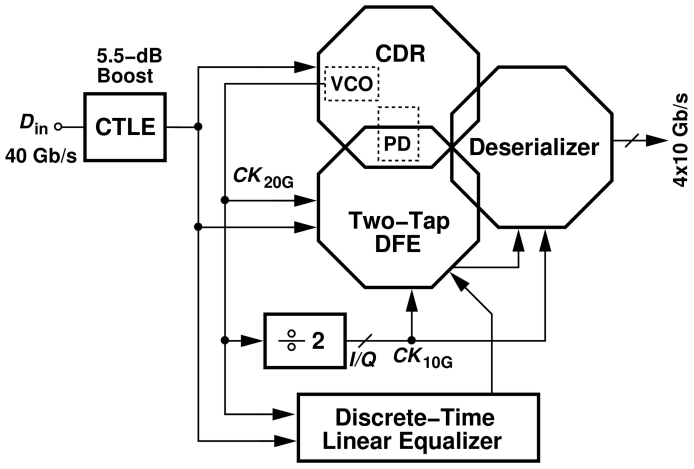

Figure 23.8.1: Conceptual receiver architecture.

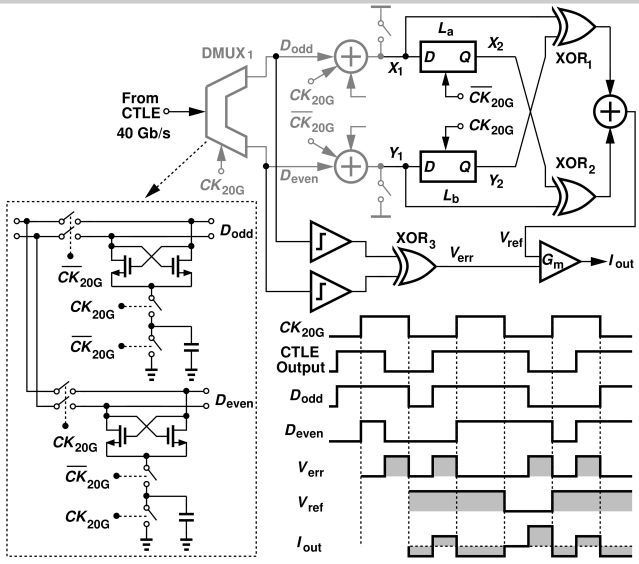

Figure 23.8.2: Proposed phase detector topology.

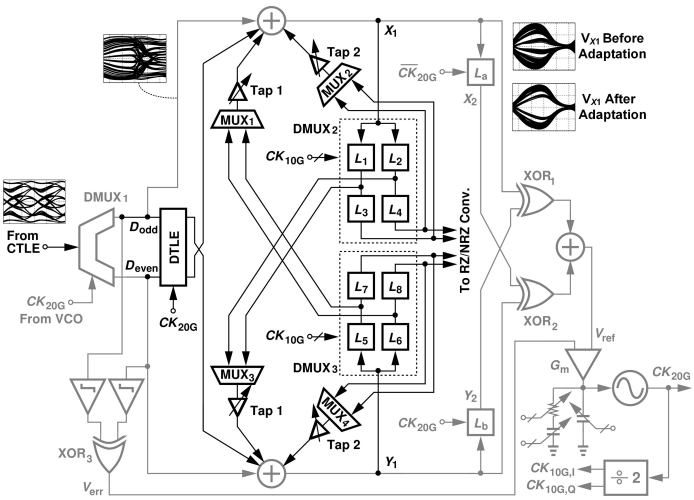

Figure 23.8.3: Proposed receiver architecture with half-rate/quarter-rate CDR and DFE.

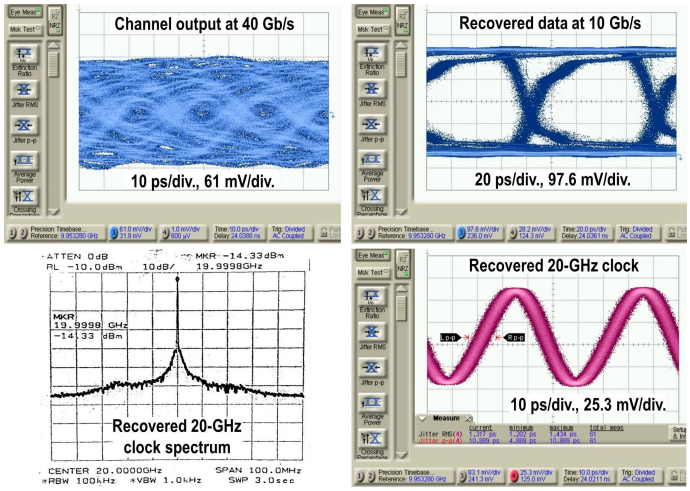

Figure 23.8.4: Measured eye diagrams of the receiver input, output, and recovered clock spectrum and its waveform.

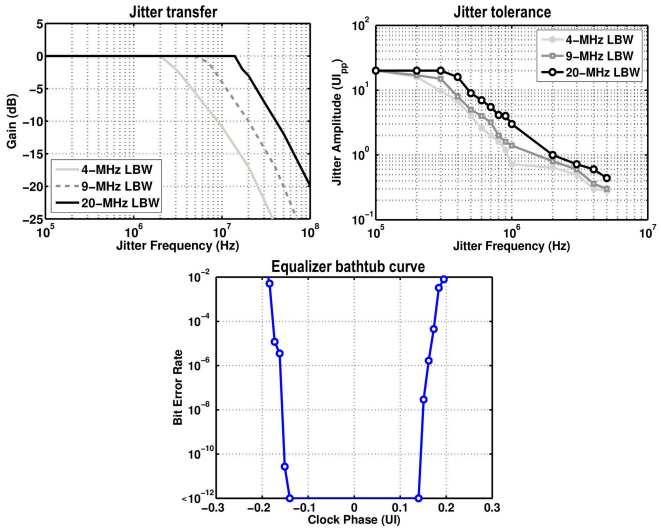

Figure 23.8.5: Measured jitter transfer, jitter tolerance and bathtub curve for 40-Gb/s data.

	This Work	Hsieh [VLSI 2011]	Chen [JSSC Mar. 2012]	Raghavan [JSSC Dec. 2013]
Data Rate (Gb/s)	40	40	40	40
Supply (V)	1	1.2 for DFE/CDR, 1.5 for CTLE	1.6	1
Channel Loss at Nyquist (dB)	18.6	23.5	19	>21
Bit Error Rate	10^{-12}	10^{-12}	10^{-12}	10^{-9}
Power Consumption (mW)	14	150	520	1050
Power Efficiency (pJ/bit)	0.35	3.75	13	26.25
Recovered Clock Jitter (ps)	1.3 rms	6.8 pp	0.319 rms at 10 GHz	-
Jitter Tolerance	0.45 UI_{pp} at 5 MHz	-	≈ 0.65 UI_{pp} At 10 MHz	0.95 UI_{pp} at 9 MHz
Area (mm^2)	0.019	0.278	1.1475*	3.9*
Technology	45-nm CMOS	65-nm CMOS	65-nm CMOS	40-nm CMOS

* Includes pads

Figure 23.8.6: Performance summary and comparison to prior art.

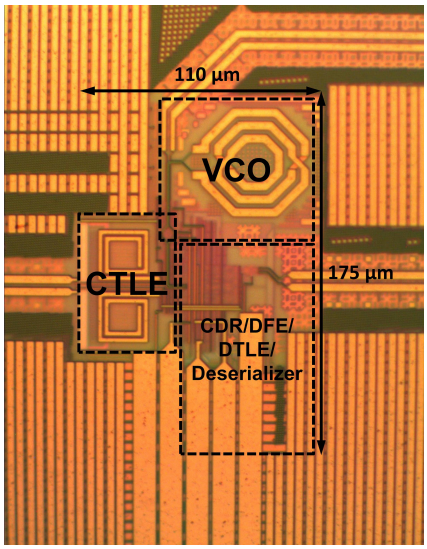

Figure 23.8.7: Receiver die photograph.

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