A 5-GHz 11.6-mW CMOS Receiver for IEEE 802.11a Applications

Aliakbar Homayoun and Behzad Razavi
Electrical Engineering Department
University of California, Los Angeles

Abstract

A direct-conversion receiver employs a 1-to-6 transformer as a low-noise amplifier along with passive mixers and non-invasive baseband filters. Realized in 65-nm CMOS technology, the receiver provides an average noise figure of 5.3 dB and a sensitivity of −70 dBm at a data rate of 54 Mb/s. The prototype draws 11.6 mW from a 1-V supply and occupies an active area of 0.18 mm^2.

I. Introduction

While advances in the art have considerably reduced the power consumption of RF oscillators, frequency dividers, and analog-to-digital converters, the main receiver (RX) chain in 5-GHz systems draws a disproportionately high power, e.g., about 46 mW in [1]. It is therefore desirable to develop low-power RX front ends and baseband filters for WiFi applications.

This paper introduces a complete 5-GHz CMOS receiver that meets the 11a sensitivity, blocking, and filtering requirements while consuming 11.6 mW. This fourfold reduction in power is achieved through the use of a transformer as a low-noise amplifier (LNA), passive mixers, and "non-invasive" baseband filtering [2].

Section II introduces the receiver architecture and Section III elaborates on the design of the transformer. Section IV deals with the interface between the transformer and the mixers and its effect on the RX input matching. Section V describes the baseband channel-select filters and Section VI presents the experimental results.

II. Receiver Architecture

With the choice of passive mixers in a receiver, the power consumption arises from three other building blocks: The LNA, the local oscillator (LO) buffers, and the baseband filters, with the last typically dissipating the most [1]. As shown in Fig. 1, we implement the LNA by means of a transformer, thus obtaining voltage gain and ensuring input matching. The small passive mixer devices require an LO buffer power of 0.4 mW (Section IV). We also exploit non-invasive filtering to realize a fourth-order elliptic response with a more relaxed power-linearity-noise trade-off than that of conventional filters.

By virtue of its high turns ratio, the transformer in Fig. 1 exhibits a relatively high output impedance, approximating a current source. Operating with 25%-duty-cycle LOs, the switches can therefore be viewed as current-driven mixers, thus contributing less noise than voltage-driven topologies [3].

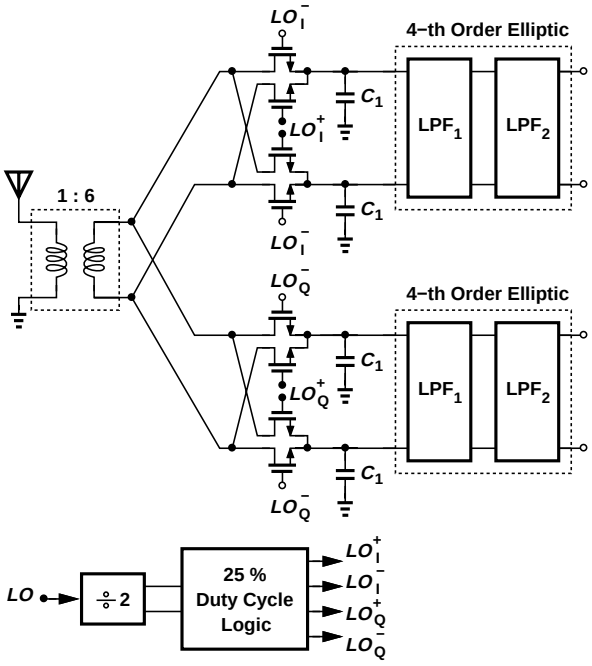

Fig. 1. Receiver architecture.

We should highlight two advantages of our approach over the LNA-less receiver in [4]. First, the input matching inherent in our receiver provides a robust interface with the antenna in the presence of long external traces. Second, in addition to saving power, our front end benefits from a higher linearity.

III. Transformers as LNAs

A low-noise amplifier provides voltage gain and proper input matching but it need not draw supply current. This work explores the possibility of using a high-turns-ratio transformer for this purpose and co-designing it with passive mixers so as to achieve an acceptable noise figure.

The 1-to-6 transformer is realized as shown in Fig. 2, with a one-turn primary in metal 8 and a six-turn secondary in metal 9. Different from planar [5] or other stacked [6] structures, this geometry exhibits a more favorable trade-off between the insertion loss and the loaded voltage gain. As the number of turns in the secondary increases, the voltage gain rises but

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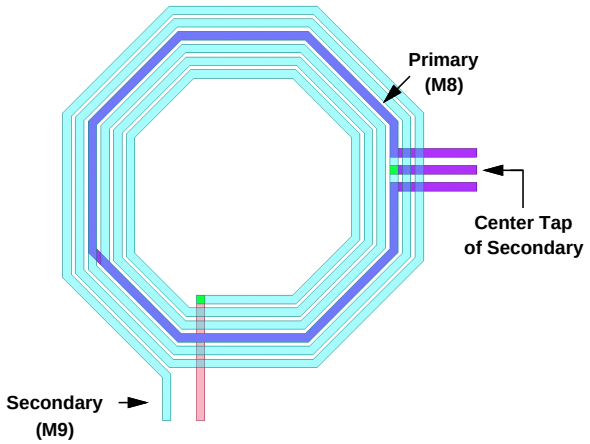

Fig. 2. Transformer geometry.

flattens out because the outer turns begin to have negligible coupling with the primary. The choice of the geometry also depends on the input impedance of the passive mixers and is thus finalized in conjunction with their design.

According to HFSS simulations, the above transformer has an insertion loss of 2.4 dB and a loaded voltage gain of 12 dB at 5.5 GHz. The outer diameters of the primary and the secondary are 146 μm and 170 μm, respectively.

IV. Mixer Design

Driven by a 50-Ω antenna, the transformer presents an output impedance of 800 Ω. Thus, the quadrature passive mixers in Fig. 3 must be designed for an overall input resistance equal to this value. Since the input impedance of current-driven mixers depends on the source impedance [7], we model the interface as shown in Fig. 3, where I_T and Z_T represent the

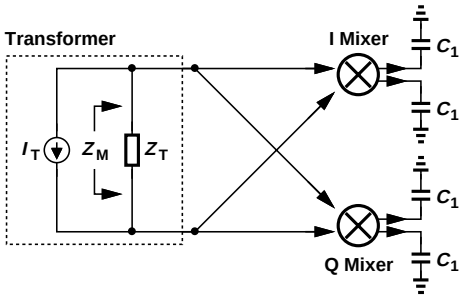

Fig. 3. Transformer-mixer interface.

transformer over a wide bandwidth and Z_M denotes the composite impedance resulting from Z_T and the input impedance of the I and Q mixers. With a baseband capacitive load of C_1, Z_M can be simplified to [7]:

$$Z_M(\omega) = R_{sw} || Z_T(\omega) + \left[\frac{Z_T(\omega)}{Z_T(\omega)+R_{sw}}\right]^2 \div \sum_{k=-\infty}^{\infty} \frac{1}{(4k+1)^2[Z_T(\omega+4k\omega_{LO})+R_{sw}]}, \quad (1)$$

where R_{sw} is the switch on-resistance. Due to the bandpass nature of Z_T, the summation on the right-hand side must be carried out for about 14 terms. Ideally, in the range of 5 to 6 GHz, we must have $Re\{Z_M(\omega)\} \approx Z_T(\omega)/2 \approx 400\ \Omega$ and $Im\{Z_M(\omega)\} \approx 0$. With a choice of W/L =10 μm/ 60 nm for the switches, we obtain an S_{11} of -12 dB in this band. The LO buffers driving eight such switches draw a total power of $fCV_{DD}^2 \approx 0.4$ mW at 6 GHz.

Simulations indicate that the "zero-power" RF front end consisting of the transformer and the mixers exhibits a noise figure of 4.5 dB and an input P_{1dB} of -5.2 dBm at 5.5 GHz. For a target RX NF of less than 6 dB, all of the subsequent stages must contribute no more than 1.5 dB, demanding additional circuit techniques.

V. Filter Design

In the 11a standard, the adjacent and alternate adjacent channels can be higher than the desired channel by 16 dB and 32 dB, respectively. The baseband filters must therefore provide a sharp roll-off to reduce these channels to well below the desired signal level – unless the baseband ADCs offer a dynamic range wide enough and a sampling rate high enough to handle partially-attenuated blockers.

Figure 4 shows the realization of the fourth-order elliptic filter. The circuit consists of two second-order sections, each

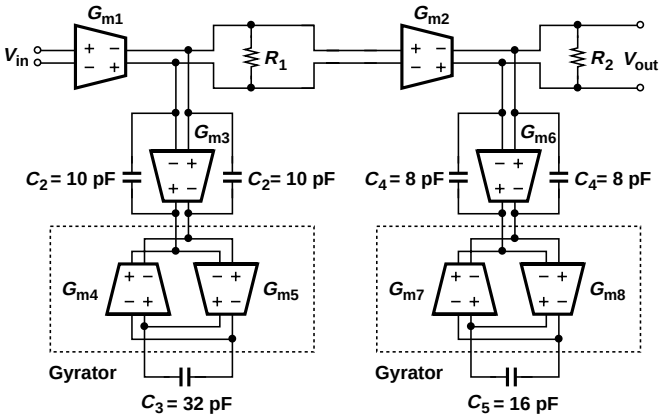

Fig. 4. Fourth-order elliptic low-pass filter.

formed as a G_m cell and a frequency-selective load [2]. Created by G_{m3}-G_{m5}, G_{m6}-G_{m8}, and the capacitors, the loads remain *open* in the passband, contributing small noise and nonlinearity to the desired signal, and act as a short circuit in the stopband. This stands in contrast to conventional filters that process the desired signal and the blockers in the same stage and hence add considerable noise and nonlinearity.

The gyrators in Fig. 4 transform their load capacitors to an inductor, which then creates a resonance in each integrator. Proper choice of these resonance frequencies shapes the frequency response of the overall filter, including its passband ripple and stopband rejection. The fourth-order filter exhibits an input-referred noise voltage of 2 nV/$\sqrt{\text{Hz}}$ at 5 MHz, an in-channel IIP_3 of 193 mV_{rms} and a voltage gain of 39 dB while consuming 4.3 mW. The filter voltage gain is programmable in steps of 2 to 3 dB for a total range of 43 dB.

VI. Experimental Results

The receiver of Fig. 1 has been fabricated in 65-nm digital CMOS technology. Figure 5 shows the die photograph. The

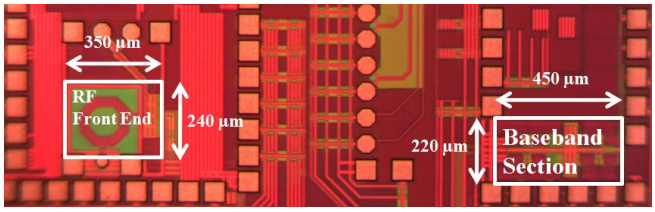

Fig. 5. Die photograph.

RF section occupies 350 μm $\times$ 240 μm and the baseband section 450 μm $\times$ 220 μm.[1] The circuit has been characterized in a chip-on-board assembly with a 1-V supply.

Figure 6 plots the measured noise figure of the complete receiver as a function of the baseband frequency. The average noise figure is about 5.3 dB.

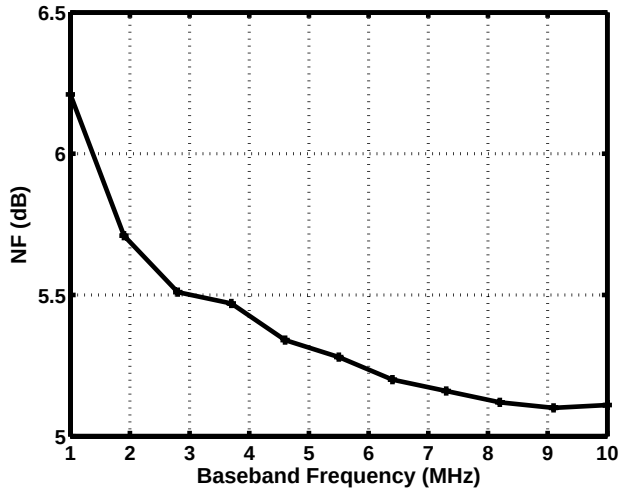

Fig. 6. Measured noise figure.

The sensitivity of the receiver is measured with the aid of Agilent's N5182 MXG vector signal generator and N9020A MXA signal analyzer, which respectively apply a 64-QAM signal and sense the baseband outputs to construct the signal constellation. Figure 7 shows the results for a -65-dBm 5.7-GHz input. The error vector magnitude (EVM) is equal to -28 dB, exceeding the 11a specification. (For an input level of -70 dBm, an EVM of -23.4 dB is measured.)

Figure 8 plots the S_{11} from 5 to 6 GHz, measured at each input frequency, while the mixers switch at the corresponding LO frequency. It is expected that a slightly larger transformer can yield $S_{11} = -10$ dB at the lowest 11a frequency, 5.15 GHz.

Figure 9 plots the measured receiver transfer function, revealing a passband peaking of 1 dB and a rejection of 22 dB at 20 MHz and 43 dB at 40 MHz.[2] Owing to the finite output

[1] Due to limited silicon area, the receiver layout is decomposed and placed within other unrelated circuits, but all of the connections are present on the chip.

[2] In this measurement a first-order RC section follows each output on the PCB.

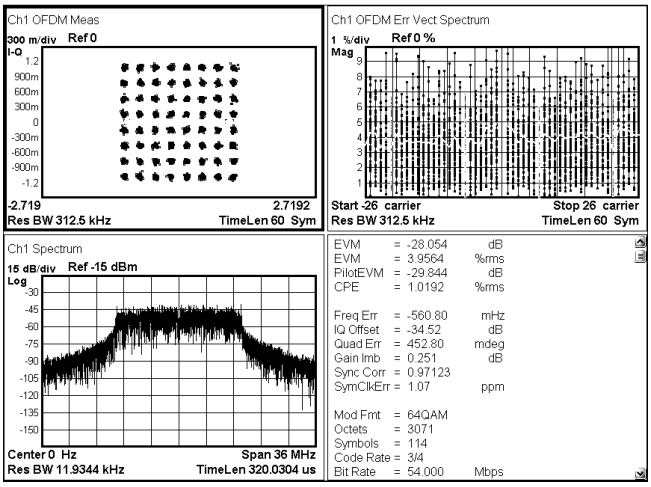

Fig. 7. Measured EVM at $P_{in} = -65$ dBm.

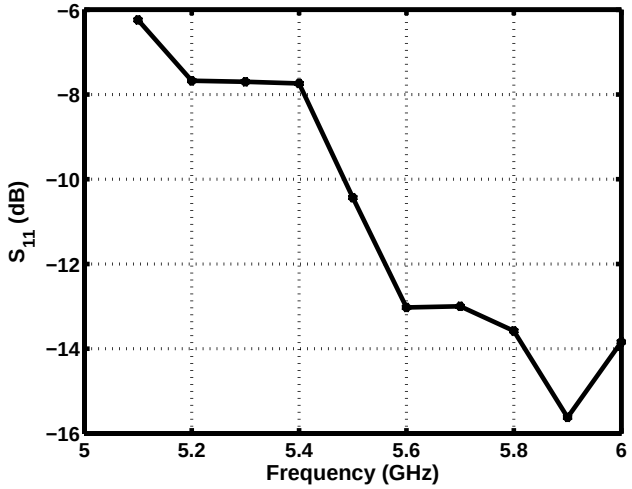

Fig. 8. Measured input return loss.

resistance of the G_m cells, the filter does not exhibit the deep notches that are characteristic of elliptic transfer functions. The

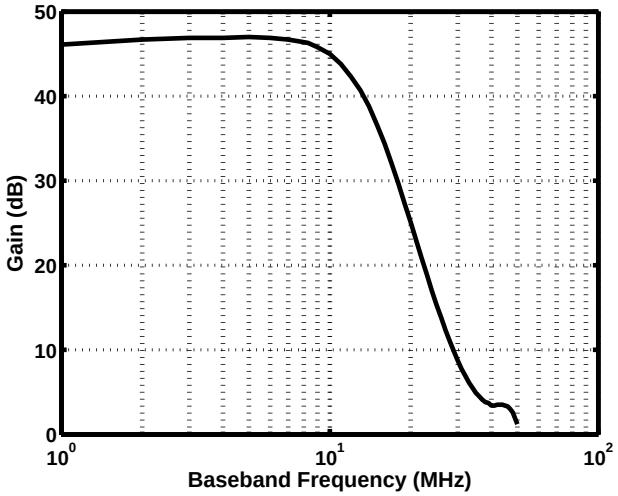

Fig. 9. Measured receiver transfer function.

performance of the baseband filter is ultimately tested when a large blocker accompanies a small desired signal. In such a case, the filter must remain sufficiently selective and linear so that the desired signal does not experience compression. Figure 10 plots the measured passband gain as a function of the power of an RF blocker in the adjacent or alternate adjacent channel.

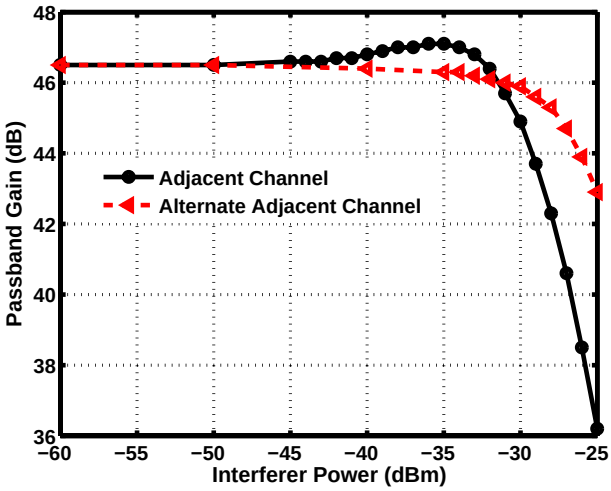

Fig. 10. Measured passband gain in the presence of a blocker.

The filter nonlinearity resulting from a blocker may also corrupt the 11a 64-QAM OFDM signal by creating cross modulation among the sub-channels. This effect is characterized by setting the RF input signal level 3 dB above the sensitivity, applying a blocker, and raising its level until the EVM falls to −23 dB. Figure 11 plots the relative blocker level as a function of the frequency offset with respect to the desired signal center frequency.

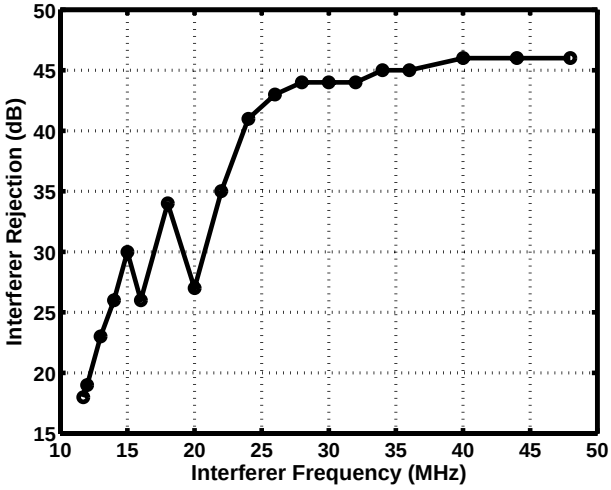

Fig. 11. Measured interferer rejection.

Table 1 summarizes the receiver performance and compares it to that of prior art.

Table 1. Comparison with state-of-the-art.

	This Work	[1]	[8]	[9]
Frequency (GHz)	5.1 − 5.9	5.15 − 5.35	4.9 − 5.95	5.1 − 5.9
NF (dB)	5.3	8.0	4.4	5.5
IIP_3 (dBm)	+ 2.6	−11.2	+ 5	+ 16
Gain (dB)	5 − 48	14 − 94.5	8 − 74	19 − 89
Sensitivity (dBm) at 54 Mb/s	−70	NA	NA	−75.5
Power (mW)	11.6	46	108*	72.7**
LNA	0	11.7		
Mixers	0	9.8		
LO Buffers	0.4	10.8		
Filters, VGAs	10	13.7		
Divider/ 25% Logic	1.2			
CMOS Process	65 nm	0.18 μm	0.18 μm	0.13 μm
Area (mm^2)	0.183	NA	NA	NA

* Including ADC.

** Without LO Buffer.

Acknowledgment

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