A 300-GHz Fundamental Oscillator in 65-nm CMOS Technology[1]

Behzad Razavi

Electrical Engineering Department

University of California, Los Angeles, CA 90095

Abstract—Magnetic feedback from a differential pair to the core of a cross-coupled oscillator reduces the effect of device losses, raising the oscillation frequency. Three prototypes using one-turn nested inductors and including on-chip downconversion mixers operate at 205 GHz, 240 GHz, and 300 GHz while drawing a power of 3.5 mW.

A common approach to obtaining high oscillation frequencies is to employ "superharmonic" oscillators, i.e., to "sift" second or higher harmonics by techniques such as edge combining [1] or push-push action [2, 3]. By contrast, "fundamental" oscillators operate at the first harmonic, offering two advantages: (a) they demonstrate the ability to achieve gain at the frequency of interest, paving the way for the design of other critical RF blocks such as amplifiers, mixers, and dividers; (b) they provide differential and even quadrature outputs, greatly simplifying the design of dividers and quadrature upconverters and downconverters.

This paper proposes a fundamental oscillator topology that tolerates greater device nonidealities than does the conventional cross-coupled configuration, thus achieving in 65-nm technology a speed nearly 50% higher than the fundamental frequency of the prior art in 45-nm technology [3] and at half the bias current.

As the oscillation frequency approaches the f_{max} of the transistors, several device nonidealities begin to introduce loss, equivalently reducing the Q of the tank to well below that of the inductor(s). For example, in the conventional cross-coupled topology shown in Fig. 1(a), each of the nodes X and Y is loaded by five resistive components: the parallel equivalent resistance of the inductor (R_P), the gate resistance, the resistance due to the feedback from the drain to the gate through C_{GD}, the output resistance of each MOSFET, and the input resistance of the following stage, e.g., a buffer. As the load inductance and hence R_P are reduced, the oscillation frequency increases, reaching the limit when the loss due to R_P and other components yields a power gain less than unity. We surmise that the oscillation frequency can be increased if (a) one or more of these components can be distributed onto one or more nodes, and/or (b) the output impedance driving these components can be lowered. We thus decompose the load inductor into two with the same mutual coupling and insert a differential pair to drive the disengaged inductor [Fig. 1(b)].

In the proposed circuit, M_3 and M_4 serve two functions: they isolate the core from the input capacitance and resistance of the buffer, and they return an in-phase current to the core by virtue of the mutual coupling between L_1 and L_2. The startup condition can be derived if all of the losses are lumped in parallel with L_1

and L_2, revealing that W_1-W_4 must be *larger* here than W_1-W_2 in the conventional cross-coupled topology. Nonetheless, the loss compensation afforded by M_3 and M_4 outweighs the larger node capacitances, thus yielding a higher oscillation frequency.

The cross-coupled and proposed topologies shown in Fig. 1 can be compared along several axes so as to demonstrate the speed advantage of the latter. For example, the value or Q of the inductors or the width of the transistors can be varied to reach the maximum achievable frequency. Plotted in Fig. 2 are the simulated oscillation frequencies as L_1 and L_2 are varied and their mutual coupling factor, k, is kept at 0.4. Here, $W_1 = W_2 = 0.4$ μm in the former and $W_1 = \cdots = W_4 = 1.6$ μm in the latter. The buffer input transistors have a width of 0.4 μm. Each transistor includes a gate resistance (30 Ω for a 0.4-μm finger). The proposed oscillator topology can operate at a higher frequency if the polarity of k is reversed or the gate connections of M_3 and M_4 are swapped. While not practical at frequencies of interest here, this property has been exploited in the range of tens of gigahertz [4].

In order to minimize the gate resistance, each transistor incorporates a finger width of 0.4 μm with metal contacts on both ends. Such a width, however, accommodates only two contacts in the source/drain areas. The small size of contacts and vias in deep submicron technologies leads to a series resistance that becomes comparable with that of small spiral inductors. Figure 3(a) illustrates a case where the current flowing through a metal-9 spiral must descend through eight vias and one contact to reach the drain of a transistor. If the gate of the next stage's input device senses the voltage at node X_0, then R_{via1} (the sum of all via resistances) appears in series with the inductor. On the other hand, as shown in Fig. 3(b), if the gate senses the voltage at node X, albeit through another resistance, R_{via2}, we expect the effect of R_{via1} to vanish. Simulations suggest that the "force and sense" (Kelvin) arrangement in Fig. 3(b) achieves 3% higher speed than the topology in Fig. 3(a).

The direct measurement of frequencies in the range of hundreds of gigahertz proves extremely difficult [2, 3]. In this work, the oscillator is followed by an on-chip mixer driven by an external W-band generator. Figure 4 shows the test setup. Here, M_5 and M_6 mix the oscillator output with a harmonic of f_{ext}, generating an intermediate frequency (IF) of a few tens of gigahertz. The IF output is then monitored on a spectrum analyzer. To determine which harmonic of f_{ext} produces the observed IF, f_{ext} is varied by Δf and the change in IF, ΔIF, is measured. The ratio ΔIF/Δf gives the harmonic order.

The proposed oscillator has been realized with three different designs for L_1 and L_2. Implemented as single-turn octagonal metal-9 structures, the inductors are nested so as to sustain a coupling factor of about 0.4. The diameter of L_1 varies from

24 μm to 40 μm and that of L_2 from 32 μm to 48 μm.

The three designs have been fabricated in 65-nm digital CMOS technology and tested on a probe station while running from a 1-V supply and drawing 3.7 mA. Figure 5 shows a magnified photograph of the active area, which measures about 200 μm×100 μm. The three prototypes oscillate at 205 GHz, 240 GHz, and 300 GHz. Based on the methodology described in [5], the simulation predicts these frequencies with less than 1% error, suggesting that the intrinsic BSIM4 capacitances are accurate even at frequencies approaching f_{max}. The slight supply dependence of the oscillation frequency also helps distinguish between the desired output and other mixing components and reveals that the oscillator is not injection-locked to the input. Figure 6 shows the IF spectrum when the fastest oscillator output is mixed with the third harmonic of an 88-GHz external input. The circuit operates at 300 GHz (or as a push-push oscillator at 600 GHz if node P in Fig. 1(b) is viewed as the output).

References

[1] B. Razavi and J. Sung, "A 6-GHz 60-mW BiCMOS Phase-Locked Loop," *IEEE JSSC*, pp. 1560-1565, Dec. 1994.

[2] D. Huang et al, "A 324GHz CMOS Frequency Generator Using a Linear Superposition Technique," *ISSCC Dig. Tech. Papers,* pp. 476-477, Feb. 2008.

[3] E. Seok et al, "A 410GHz CMOS Push-Push Oscillator with an On-Chip Patch Antenna" *ISSCC Dig. Tech. Papers,* pp. 472-473, Feb. 2008.

[4] B. Razavi, "Multi-Decade Carrier Generation for Cognitive Radios," *VLSI Circuits Symp. Dig. Tech. Papers*, pp. 120-121, June 2009.

[5] C.K. Liang and B. Razavi, "Systematic Transistor and Inductor Modeling for Millimeter-Wave Design," *IEEE JSSC*, pp. 450-457, Feb. 2009.

Fig. 3. Connection of inductor to drain and gate through (a) one set of vias, and (b) two independent sets of vias.

Fig. 4. Oscillator test setup.

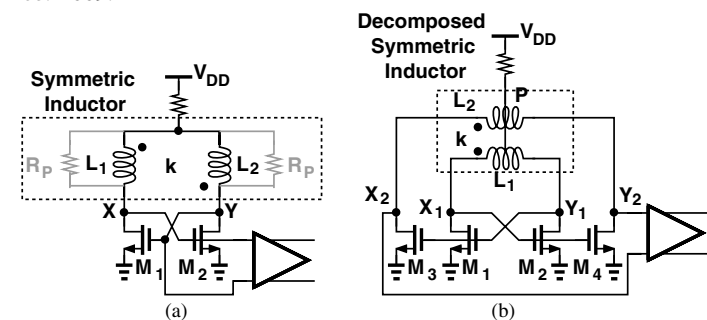Fig. 5. Oscillator die photograph.

Fig. 1. (a) Conventional cross-coupled oscillator, (b) proposed oscillator topology.
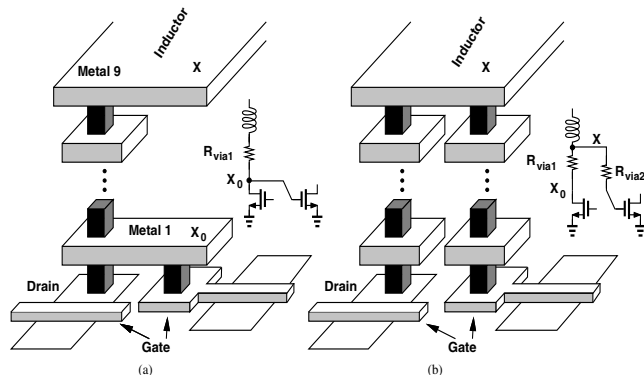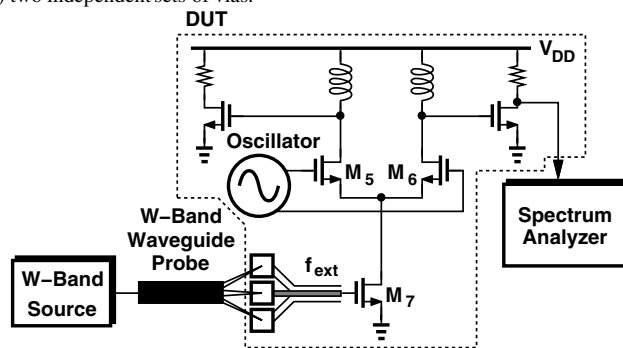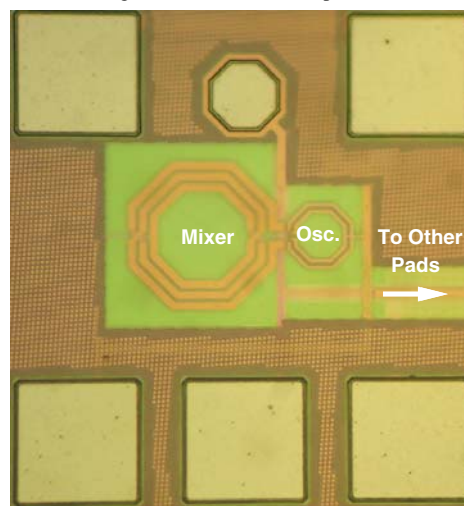

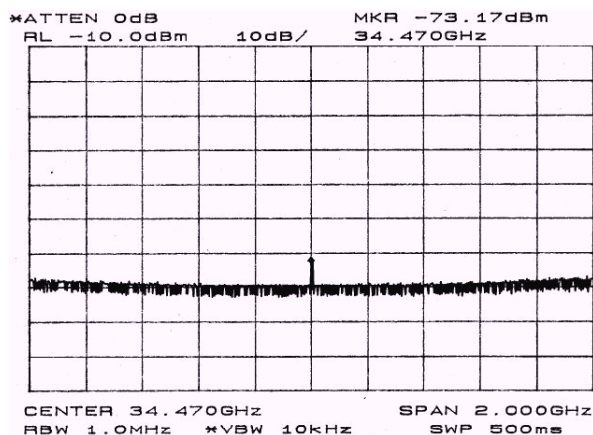Fig. 2. Comparison of speed of cross-coupled and proposed oscillators for differerent inductance values.

Fig. 6. Measured IF with an external frequency of 88 GHz.