Problem of Timing Mismatch in Interleaved ADCs

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Abstract

Time interleaving can relax the speed-power trade-off of analog-to-digital converters but at the cost of sensitivity to interchannel mismatches. This paper addresses the problem of timing mismatch, its detection, and its correction. A new frequency-domain analysis gives insight into the impact of the mismatch on random input signals and quantifies the resulting noise. A number of timing error calibration techniques are reviewed and a new approach is proposed.

I. Introduction

Time-interleaved analog-to-digital converters (ADCs) have traditionally been used for high-speed implementations. However, it has been recognized recently that interleaving can also lower the power consumption for a given resolution. This is because as the sampling rate of single-channel ADCs approaches the limits of the technology, their speed-power trade-off becomes nonlinear, making interleaving attractive. If a sufficient number of ADC channels are interleaved, then each bears a linear speed-power trade-off and hence reaches an optimum design. Of course, the overhead associated with interleaving must also be taken into account in assessing the overall performance. Additionally, for resolutions of roughly 8 bits and above, the mismatches among the channels must be removed by means of foreground or background calibration.

This paper deals with mismatches in interleaved ADCs with moderate to high resolutions, e.g., 8 to 12 bits, focusing on calibration techniques for timing errors. Section II presents the interleaving environment and its general issues. Section III illustrates the effect of interchannel mismatches from a new perspective and identifies the sources of timing errors. Section IV describes timing mismatch calibration techniques using digital filters, zero crossings, or correlations. A new detection and calibration method is also introduced.

II. Interleaving Environment

Figure 1 shows a general interleaved ADC consisting of N channels, each having a dedicated front-end sample-and-hold circuit. The required sampling clock phases are generated by a phase-locked loop (PLL) or a delay-locked loop (DLL). The digital outputs of the channels may be multiplexed to obtain an output at the full rate, but except for testing purposes, this is often unnecessary or even undesirable as the subsequent digital processing prefers the low-speed, parallel data, D_1-D_N.

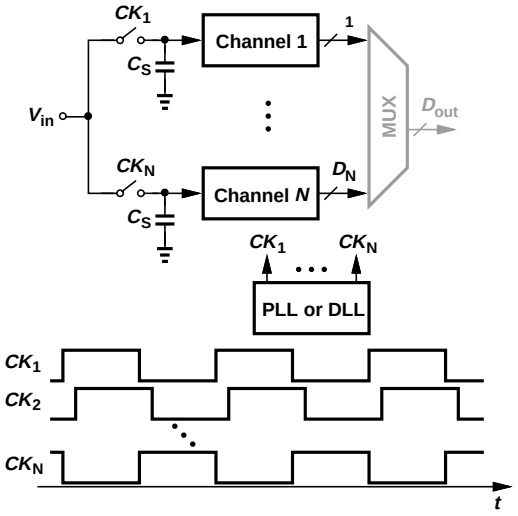


Fig. 1. Generic time-interleaved ADC environment.

In addition to raising the conversion speed, interleaving also reduces the metastability rate. Since each channel is given a longer time for conversion, the probability of metastability drops exponentially.

The interleaving overhead in the architecture of Fig. 1 contains several components. (1) As evident from the clock waveforms, the input sees a capacitance of $(N/2)C_S$, with the minimum value of C_S dictated by kT/C noise. The design of the *preceding* stage therefore becomes more difficult as N increases. (2) The PLL/DLL design, the routing of the phases to the channels, and the buffers necessary for each phase complicate the system. (3) The multiplexer may require a full-rate clock or a multi-phase implementation.

The performance of interleaved ADCs is ultimately limited by mismatches among the channels. Gain, offset, and timing mismatches heavily impact the overall signal-to-(noise + distortion) ratio (SNDR) [1] at resolutions of 8 bits or higher. As explained below, the timing mismatch is the most difficult to calibrate because it does not easily lend itself to detection or correction.

In order to avoid the problem of timing mismatch, the per-channel samplers in Fig. 1 can be replaced with one front-end sampler. This approach nonetheless demands an N-fold

978-1-4673-1556-2/12/$31.00@2012 IEEE

increase in the sampler's settling speed and is hence attractive for only moderate conversion rates.

III. Effect of Mismatches

The effect of interchannel mismatches can be analyzed in the time or frequency domains for sinusoidal or random inputs [1, 2, 3, 4]. We present a frequency-domain analysis that provides insight into the operation of interleaved ADCs and the mechanisms by which mismatches corrupt the analog input signal. We assume two channels and a random baseband input signal with a bandwidth of $\pm f_{sig}$. The signal is subjected to interleaved sampling, quantization, and multiplexing, but we ignore the effect of quantization here.

Suppose the input signal, $x(t)$, is sampled by two matched channels, with the outputs expressed as

$$y_1(t) = x(t)\sum_k \delta(t - kT_{CK}) \quad (1)$$

$$y_2(t) = x(t)\sum_k \delta\left(t - kT_{CK} - \frac{T_{CK}}{2}\right), \quad (2)$$

where T_{CK} denotes the clock period. In the frequency domain,

$$Y_1(f) = \frac{1}{T_{CK}}X(f) * \sum_k \delta(f - kf_{CK}) \quad (3)$$

$$Y_2(f) = \frac{1}{T_{CK}}X(f) * \sum_k \delta(f - kf_{CK})e^{-j\pi fT_{CK}} \quad (4)$$

where $f_{CK} = 1/T_{CK}$ is the clock frequency. As shown in Fig. 2, each channel's output experiences heavy aliasing. It is the

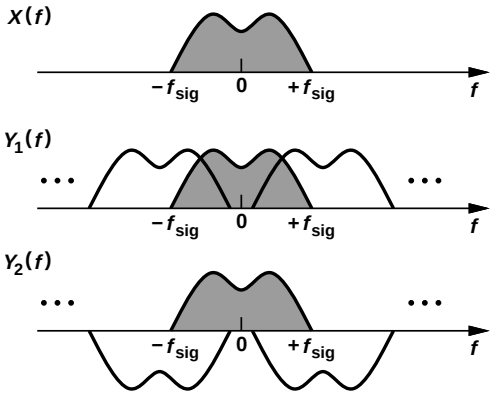


Fig. 2. Input and output spectra of a two-channel interleaved ADC.

back-end reconstruction (e.g., multiplexing) that undoes this effect. For discrete-time signals, multiplexing is equivalent to addition, causing the spectral copies centered around $\pm f_{sig}$ in $Y_1(f)$ and $Y_2(f)$ to cancel each other. The cancellation of the shifted replicas is similar to image rejection in RF receivers, underscoring the precise matching necessary for acceptably low corruption.

A. Offset and Gain Mismatch

In the absence of the input signal, the two ADCs digitize their own DC offsets. Thus, the multiplexed output toggles between the two offsets with a period equal to T_{CK}, introducing a tone at f_{CK} (and others at $3f_{CK}$, etc.). The power of this tone is typically included in the overall interleaved ADC noise power computation [3], but, as an unmodulated sinusoid, it may not be objectionable. Moreover, it can be removed by a digital notch filter.

The effect of gain mismatch can be readily seen from the spectra in Fig. 2. As shown in Fig. 3, the shifted replicas

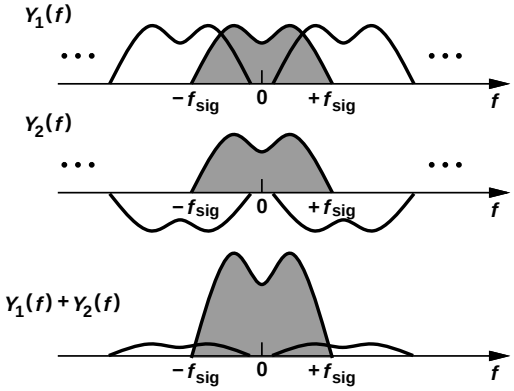


Fig. 3. Effect of gain mismatch in an interleaved ADC.

centered around $\pm f_{sig}$ in $Y_1(f)$ and $Y_2(f)$ do not cancel completely, corrupting the baseband signal. For example, for a gain mismatch of α, the signal-to-noise ratio (SNR) is limited to $10\log(4/\alpha^2)$, where the factor of 4 accounts for the two copies of $X(f)$ around $f = 0$ in $Y_1(f) + Y_2(f)$ in Fig. 3.

B. Timing Mismatch

The effect of timing mismatch in interleaved samplers is somewhat different from that of phase mismatch in RF receivers. Since the sampling error is proportional to the *slope* of the analog input waveform, a (small) skew of ΔT between the channels translates to an additive term equal to $\Delta T dx/dt$. In the frequency domain,

$$Y_1(f) = \frac{1}{T_{CK}}X(f) * \sum_k \delta(f - kf_{CK}) \quad (5)$$

$$Y_2(f) = \frac{1}{T_{CK}}[X(f) + j2\pi f\Delta TX(f)] * \sum_k \delta(f - kf_{CK})e^{-j\pi fT_{CK}}. \quad (6)$$

We observe that $Y_2(f)$ contains the following errors: (1) for $k = 0$, the error is equal to $j2\pi f\Delta TX(f)$; i.e., a first-order shaped spectral copy of $X(f)$ with a 90° phase difference is superimposed on $X(f)$; this error is illustrated in Fig. 4(a), where $X(f)$ is assumed flat for ease of illustration; (2) for $k = \pm 1$, the error is given by $-j2\pi(f \pm f_{CK})\Delta TX(f \pm f_{CK})$, i.e., it is similar to the first component but centered around $\pm f_{CK}$ [Fig. 4(b)]. It is important to note that the first error found above is not readily identified with a *sinusoidal* input. As shown in Fig. 5, the error coincides with the input and hence may appear benign even though our analysis reveals that the signal is corrupted by its own derivative. In order to

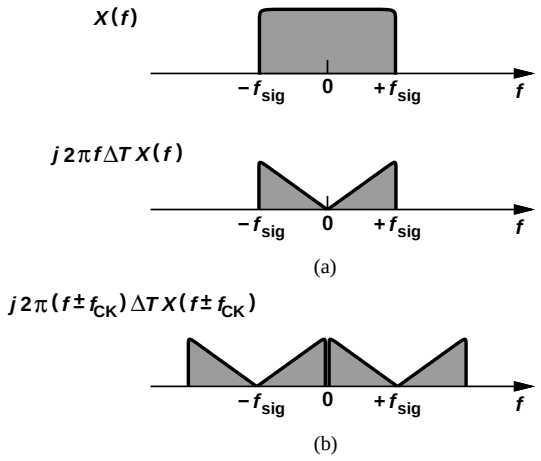


Fig. 4. Effect of timing mismatch: first-order shaped spectra (a) centered around zero, (b) translated to $\pm f_{CK}$.

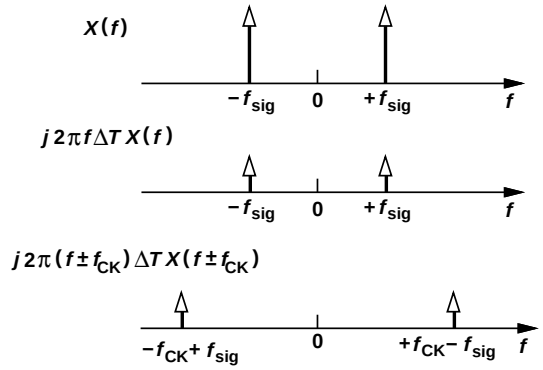


Fig. 5. Effect of timing mismatch with a sinusoidal input.

compute the corruption due to the two foregoing components, we denote the input signal power spectral density by $S_X(f)$ and write the noise in the final output as:

$$P_n = 2\int_0^{+f_{sig}} (2\pi f\Delta T)^2 S_X(f)df + 2\int_0^{f_{sig}} [2\pi(f-f_{CK})\Delta T]^2 S_X(f-f_{CK})df. \quad (7)$$

For example, if $S_X(f)$ is flat and equal to $\eta/2$ from $-f_{sig}$ to $+f_{sig}$, then

$$P_n = 4\frac{\eta}{2}(4\pi^2\Delta T^2)\int_0^{+f_{sig}} f^2 df \quad (8)$$

$$= \frac{8}{3}\pi^2\Delta T^2\eta f_{sig}^3. \quad (9)$$

The signal power at the output is equal to

$$P_{sig} = 4\int_{-f_{sig}}^{+f_{sig}} \frac{\eta}{2}df, \quad (10)$$

where the factor of 4 accounts for the two spectral copies centered around $f = 0$ in $Y_1(f)$ and $Y_2(f)$ in Fig. 2. It follows that

$$\text{SNR} = \frac{3}{2\pi^2\Delta T^2 f_{sig}^2}. \quad (11)$$

Figure 6 plots the maximum tolerable value of ΔT as a function

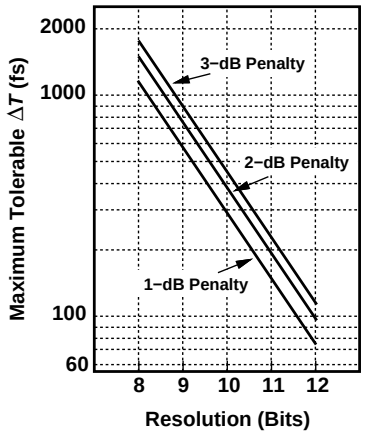


Fig. 6. Maximum tolerable timing mismatch for different SNR penalties.

of the nominal resolution for different amounts of SNR penalty. An input frequency of 500 MHz is assumed to underscore the extremely tight phase matching necessary in today's designs. Such demanding margins complicate the design of the correction circuitry, requiring long digital filters or finely-adjustable analog delay lines.

C. Sources of Timing Mismatch

A number of mismatch components displace the interleaved sampling instants from their ideal position. For two channels, the sampling clock path consists of a voltage-controlled oscillator (VCO), a buffer, a bootstrap circuit, and a differential sampling network. Figure 7 conceptually illustrates this path,

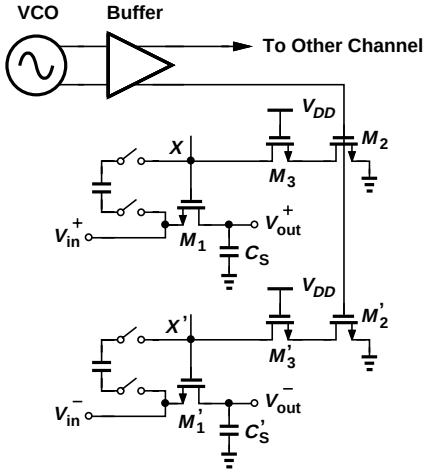


Fig. 7. Typical clock path in a two-channel ADC.

including only the relevant sections of the bootstrap circuit [5]. Here, transistor M_2 turns off the main sampling switch, M_1, and M_3 shields M_2 as V_X rises above the supply voltage [5]. (The lower path with the primed device labels operates in the same manner.) The other phase of the clock drives the second channel. The timing error in this case arises from the departure of the VCO duty cycle from 50% and the mismatches in the clock path.

In addition to the asymmetries in the VCO and its buffer, the bootstrap devices introduce significant timing errors. This can be seen from Fig. 7 by noting that (a) the branch consisting of M_2, M_3, the total capacitance at node X, and M_1 contributes mismatches, and (b) the standard deviation of these mismatches is multiplied by 2 because the two differential interleaved ADCs incorporate *four* such branches.

For a large number of interleaved channels, the clock path becomes more complex and hence prone to larger mismatches. Figure 8 shows an example for four channels. A divide-by-two circuit generates quadrature phases of the clock but also contributes additional mismatches.

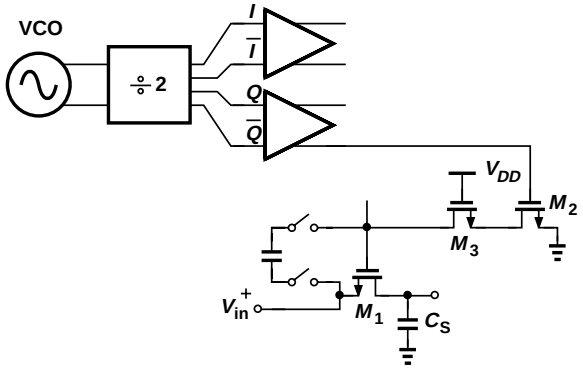


Fig. 8. Clock path for interleaving by a factor of 4 or higher.

It is possible to remove the phase mismatches caused by the VCO and the divider through the use of gating [6]. Consider the two-channel example depicted in Fig. 9(a), where "predictive" waveforms V_{even} and V_{odd} gate the master clock such that its falling edges are alternately applied to each channel [6]. So long as each pulse on V_{even} and V_{odd} encloses the falling edge of CK_{master}, the exact position or width of these pulses is immaterial. This scheme is insensitive to the duty cycle distortion of CK_{master} and other mismatches preceding switches S_1 and S_2. That is, the timing error arises from only these switches and the sampling transistors, M_1 and M_2.

The narrow predictive waveforms shown in Fig. 9(a) may suggest insufficient acquisition or hold time. This issue is resolved by means of the topology illustrated in Fig. 9(b) [6]. Here, the two channels' sampling commands, CK_1 and CK_2, are derived from CK_{master} and $\overline{CK_{master}}$ as follows. A pulse on V_{odd} routes the falling edge of CK_{master} to CK_1 and the rising edge of $\overline{CK_{master}}$ to CK_2. After this pulse subsides, CK_1 and CK_2 retain their values (as in dynamic logic) until the next pulse on V_{even} arrives. As a result, CK_1 and CK_2 provide about 50% of the clock cycle for acquisition. Note that the critical timing mismatches still stem from only S_1-S_2 and M_1-M_2 pairs. This scheme can be generalized to more than two channels so as to remove errors due to frequency dividers, phase interpolators, etc.

IV. Timing Mismatch Calibration

The calibration of timing errors in interleaved ADCs consists of two steps, namely, detection and correction. Table I summarizes the possible combinations of these tasks: the detection and correction can be performed in the analog or digital domain, and the calibration can run in the foreground or background. Analog detection of timing mismatches is difficult because the phase error measurement circuit (e.g., a mixer) itself suffers from finite mismatches.

Various timing mismatch calibration techniques have been proposed by the circuits community [7, 8, 9, 10, 11, 12] and the signal processing community [13, 14, 15]. We deal with the former in this paper.

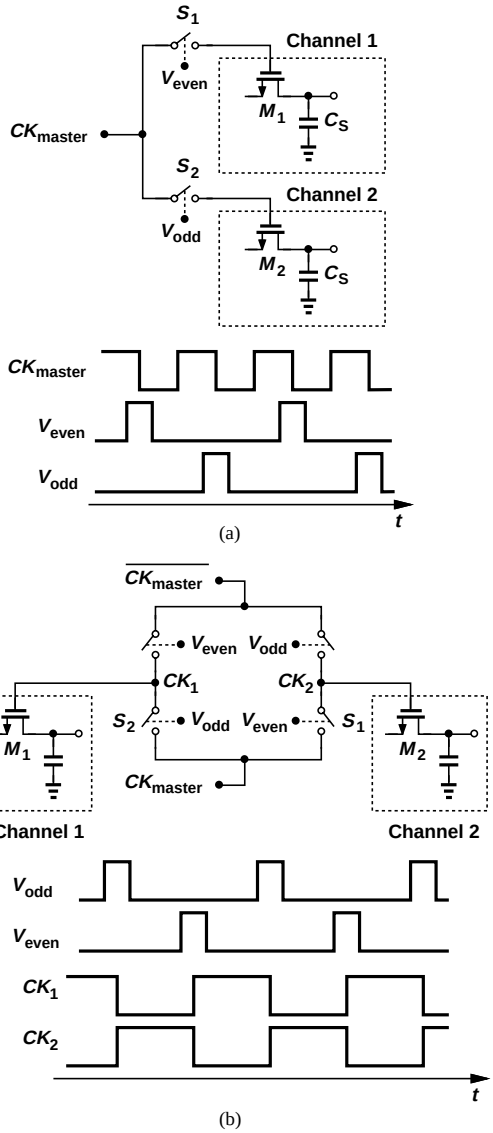


Fig. 9. (a) Gating of falling clock edges to reduce timing mismatches, (b) actual implementation to allow roughly 50% duty cycle for acquisition and hold.

Analog Detection	**Analog Correction**	**Background Calibration**
Digital Detection	**Digital Correction**	**Foreground Calibration**

Table 1. Various combinations of timing calibration techniques in interleaved ADCs .

A. Calibration Using Digital Filters

Perhaps the first timing mismatch background calibration was proposed by Jamal et al [7]. In this work, both the detection and the correction occur in the digital domain.

The phase error detection in [7] seeks to generate a dc quantity in proportion to the timing mismatch. For a sinusoidal input, $x(t) = A\cos(2\pi f_{sig}t)$, the mismatch creates an error given by $\Delta T dx/dt = -\Delta T A(2\pi f_{sig})\sin(2\pi f_{sig}t)$, which, upon sampling at f_{CK}, emerges as $\Delta T A(2\pi f_{sig})\sin[2\pi(f_{CK}-f_{sig})t]$ [Fig. 10(a)]. If the signal and this "image" are mixed

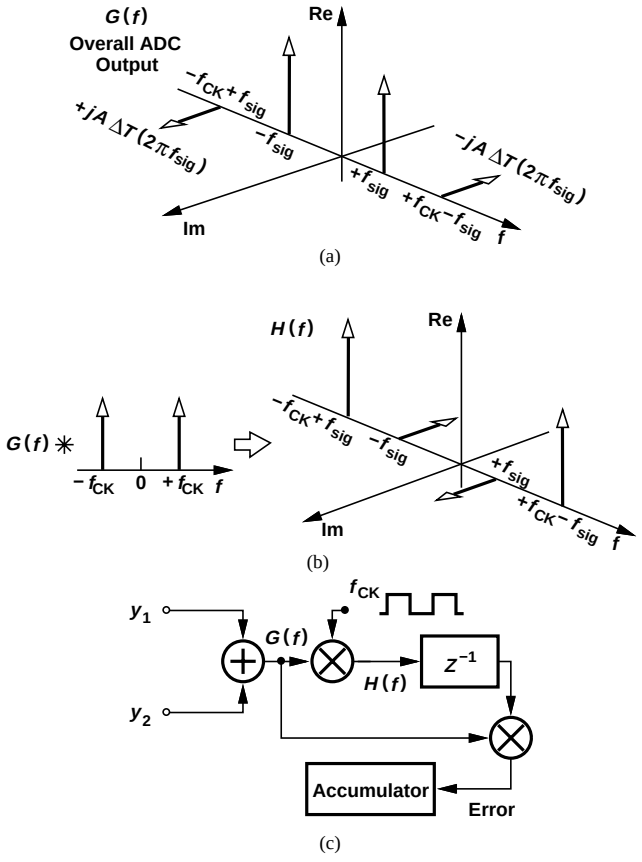


Fig. 10. (a) Effect of timing mismatch on sinusoidal input, (b) mixing with clock, (c) realization of timing error detection.

with a tone at a frequency of f_{CK}, then the image is translated to $\pm f_{sig}$ and the signal to $\pm(f_{CK} - f_{sig})$ [Fig. 10(b)]. How do we create a dc value proportional to ΔT? Since the image is 90° out of phase, mixing of $G(f)$ and $H(f)$ does not yield a dc component. Thus, one of the two must be shifted, preferably by 90°. The design in [7] employs a delay equal to one clock cycle to shift the frequency components around $f_{CK}/4$ in $H(f)$ by 90°. Nonetheless, other frequency components also produce some dc and hence a finite output representing the timing mismatch. Figure 10(c) illustrates the overall phase detection scheme [7].

The correction of the timing mismatch also presents challenging issues. As evident from Fig. 6, a 10-bit 1-GHz ADC requires a phase resolution of better than 250 fs for the timing error penalty not to exceed 1 dB. In order to remove the phase mismatch, one can simply shift either of the channels' output phase by the proper amount ($+\Delta T$ or $-\Delta T$). An all-pass digital filter suited to this task has the following transfer function [7]:

$$F(\omega) = \exp(-j\omega\Delta T)\exp\left[j\frac{\Delta T}{T_{CK}}2\pi\,\mathrm{sgn}(\omega)\right] \qquad (12)$$

This transfer function can be approximated by an FIR filter. For example, [7] incorporates a 21-tap topology with 10-bit coefficients for input frequencies up to $0.9f_{CK}$. The digital output of the accumulator shown in Fig. 10(c) adjusts the filter's coefficients so as to minimize the error.

The above approach places certain restrictions on the input signal if Nyquist-rate operation is desired. Suppose, for example, the input contains two tones at $f_{CK}/4$ and $3f_{CK}/4$. Then, the overall output exhibits images at $f_{CK} - f_{CK}/4 = 3f_{CK}/4$ and $f_{CK} - 3f_{CK}/4 = f_{CK}/4$, which are indistinguishable from the input components. The subsequent operations therefore fail to generate a proper dc value [16]—unless the input signal bandwidth is limited to $f_{CK}/2$.

The foregoing technique entails a trade-off between the length of the FIR filter and the back-off from Nyquist operation. For example, if input frequencies up to $0.95f_{CK}$ must be handled, then a larger number of taps is necessary, increasing the power consumption and the latency. Also, this approach is limited to only two channels [8]. The extension to four channels is described in [8].

B. Calibration Using Zero Crossings

It is possible to detect the timing error by counting the input zero crossings between the samples [9]. Consider two matched channels sampling an input sinusoid f_{in} that is asynchronous with respect to the clock, i.e., f_{in}/f_{CK} is irrational [Fig. 11(a)]. We count the input zero crossings between the

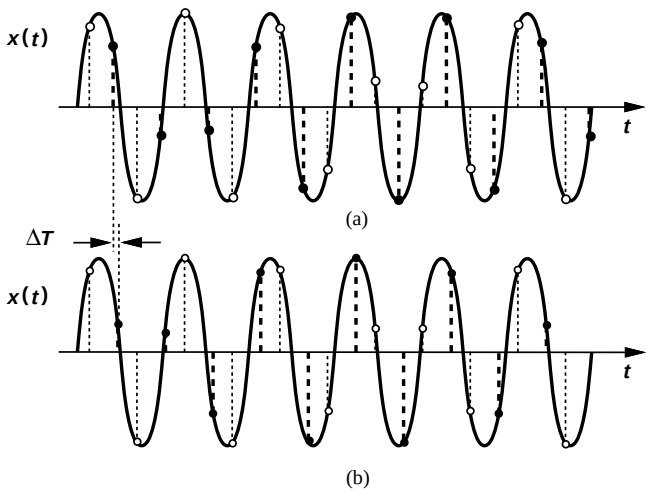


Fig. 11. Zero crossings observed between even and odd samples and between odd and even samples with (a) no timing mismatch, and (b) finite timing mismatch.

odd samples and the even samples and compare the result with the number of zero crossings between the even samples and the odd samples. In this case, these two counts have equal

averages. Now, suppose a timing error has shifted all of the odd samples to the right by ΔT [Fig. 11(b)]. Since f_{in}/f_{CK} is irrational, the samples slide along the sinusoid, and the input zero crossings occur more frequently between odd and even samples than between even and odd samples. The reverse occurs if ΔT changes sign. Thus, the average *difference* between the two zero crossing counts represents the timing mismatch [9].

The zero crossings between the samples can be detected using two comparators as shown in Fig. 12 [9], where the

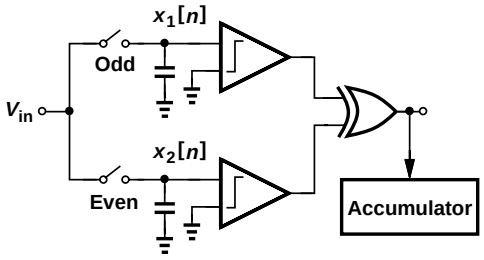


Fig. 12. Simple zero crossing detector.

XOR gate produces a logical ONE if the consecutive samples, $x_1[n]$ and $x_2[n]$, exhibit different signs. The offset of the comparators, however, introduces an error in the timing mismatch calculation. For this reason, the comparator outputs can be first subjected to first-order high-pass shaping [9].

The design in [9] corrects the timing mismatch in the analog domain. Each clock phase propagates through a variable-delay line whose delay is adjusted according to the output of the accumulator in Fig. 12.

The principal drawback of the above approach is that it can measure the timing mismatch only with certain input waveforms [9] and must therefore operate in the foreground. For example, a sinusoid near the Nyquist limit may lead to erroneous results because of the aliasing that occurs within each channel [9], as exemplified by the spectra in Fig. 4.

The zero-crossings-based detection can also be utilized with background calibration, but at a cost. Figure 13 shows an example [17] where each channel incorporates an additional sampler, M_a, and a comparator. Driven by the same clock phases as the main path, these samplers sense a periodic waveform provided by an on-chip oscillator. The comparators then count the inter-sample zero crossings as depicted in Fig. 12. Since the additional sampling and comparison paths operate independently of the main path, the timing mismatches can be measured in the background. Unfortunately, however, the mismatch between M_a and M_0 in each channel leads to a residual timing error. For linearities of 8 bits and higher, the switches must employ bootstrapping, exacerbating this issue.

C. Calibration Using Cross Correlation

It was recognized in [4] that the SNR of an interleaved ADC with an input signal power of P_{sig} is given by

$$\text{SNR} = \frac{N^2 P_{sig}^2}{N^2 P_{sig}^2 - [\sum_{k=0}^{N-1} R(\Delta T_k)]^2}, \qquad (13)$$

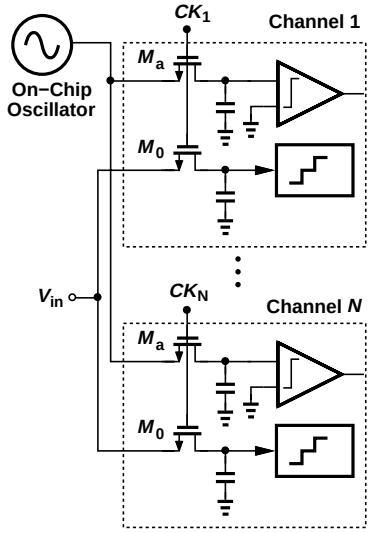


Fig. 13. Background calibration using zero crossings and an asynchronous clock.

where N denotes the number of channels and $R(\Delta T_k)$ the autocorrelation of the input signal evaluated at the interchannel timing mismatch, ΔT_k. That the SNR falls as $R(\Delta T_k)$ decreases is to be expected [4]: the autocorrelation function is narrower for faster signals, incurring a sharper roll-off for a given ΔT_k (Fig. 14). In other words, faster signals or greater

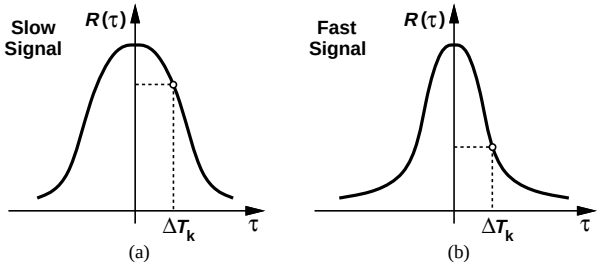


Fig. 14. Autocorrelation of slow and fast signals.

timing mismatches produce a smaller $R(\Delta T_k)$ and hence a lower SNR.

The foregoing observation suggests that the autocorrelation of each channel's output signal can serve as a measure of the timing mismatch; i.e., if the clock phases are adjusted so as to *maximize* the autocorrelation, then the SNR is maximized and, inevitably, the timing errors are minimized [10]. Rather than compute the individual channel autocorrelations, [10] determines the *cross correlation* between each main channel and an auxiliary channel [Fig. 15(a)]. The average product of Y_1 and Y_{cal} is a function of the timing mismatch between Channel 1 and the auxiliary path, reaching a maximum if ΔT goes to zero. The auxiliary channel in fact can have a resolution as low as 1 bit [10]. The phase correction in [10] is performed in the analog domain and realized by a variable-delay line.

The above timing error detection technique requires that the auxiliary channel be sampled by an asynchronous clock, CK_{cal} [10]. This is because the auxiliary samples must slide against and periodically coincide with the other channels' sam-

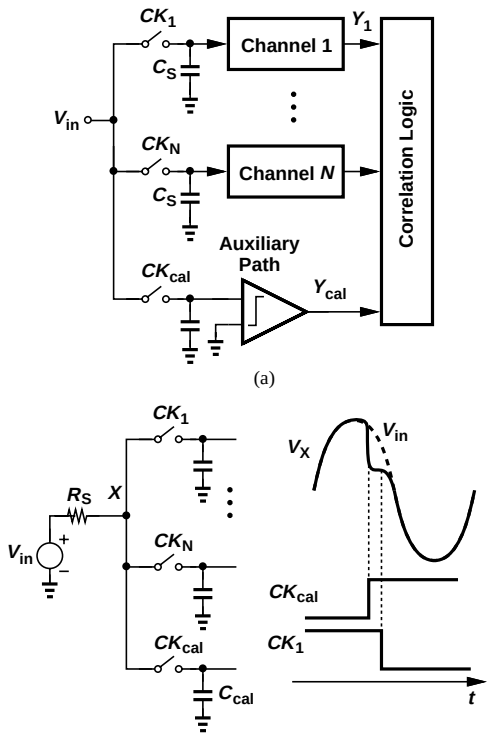


Fig. 15. (a) Background calibration using an auxiliary channel driven by an asynchronous clock, (b) disturbance of input due to asynchronous sampling.

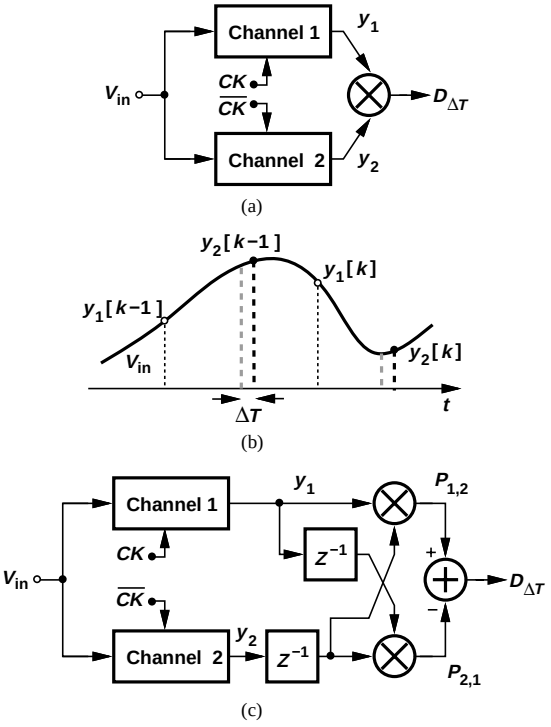


Fig. 16. (a) Attempt to compute timing error by mixing, (b) waveform showing effect of timing error, (c) background timing error detection using two products.

ples. Thus, some additional means of generating CK_{cal} is necessary.

While applied successfully to a 5-bit ADC [10], the asynchronous operation of the auxiliary channel may prove problematic for higher resolutions if the *source impedance* is finite. Figure 15(b) illustrates the issue. Suppose CK_{cal} rises at $t = t_1$, causing C_{cal} to draw a large transient current from R_S. The sudden drop in V_X is inherited by, say, the first channel, if CK_1 falls soon thereafter. This periodic amplitude and phase modulation of V_X by CK_{cal} leads to unwanted tones in the overall ADC output.

D. Proposed Technique

In analogy with phase detection in PLLs and RF circuits, we may contemplate digital *mixing* as a means of computing the timing error. Depicted in Fig. 16(a), the idea is to multiply the channels' outputs and utilize the dc component of the product, $D_{\Delta T}$, as a measure of the mismatch. However, a closer look reveals a serious issue in this approach. Suppose the two channels are matched and the input is a sinusoid at f_{CK} (half of the overall sampling rate). Then, the consecutive samples are uncorrelated, yielding a zero average for $D_{\Delta T}$. On the other hand, if the input contains frequency components below f_{CK}, the samples become correlated and $D_{\Delta T}$ assumes a *finite* average. That is, a realistic signal produces a dc component at the output even if the channels are matched, making detection of the timing mismatch difficult.

The above issue can be resolved if *two* products are formed. Consider the waveform shown in Fig. 16(b), where the y_2 samples are offset by ΔT. We recognize that the time difference between samples $y_1[k-1]$ and $y_2[k-1]$ is greater than that between $y_2[k-1]$ and $y_1[k]$. Thus, if $y_1[k-1]$ is delayed and multiplied by $y_2[k-1]$, the product exhibits a finite average that is slightly "skewed" due to ΔT. Similarly, if $y_2[k-1]$ is delayed and multiplied by $y_1[k]$, the product's average is skewed in the opposite direction. We therefore expect that the difference between the two products has a dc component in proportion to ΔT. Figure 16(c) shows the complete digital back end for timing error detection.

The proposed timing mismatch measurement technique has been simulated with a random input whose bandwidth is limited to $\pm f_{CK}$. Figure 17 plots the average value of $P_{1,2} -$

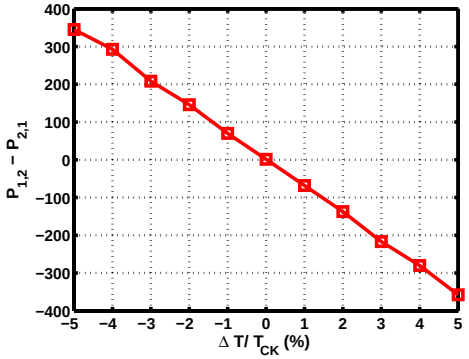
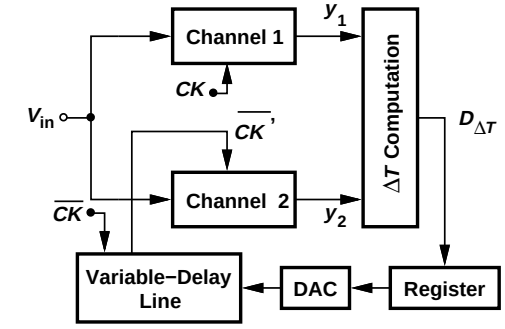


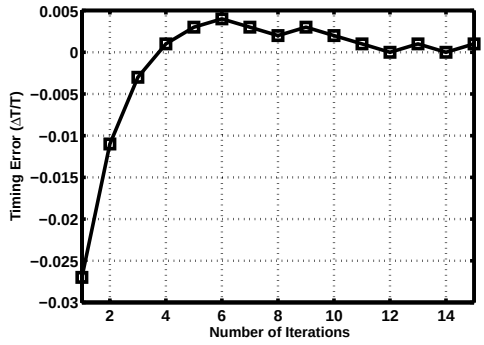
Fig. 17. Simulated average difference between the two products as a function of timing error (arbitrary vertical unit).

$P_{2,1} = D_{\Delta T}$ as a function of $\Delta T/T_{CK}$. The behavior of $P_{1,2}$ and $P_{2,1}$ depends on the input statistics, but the difference varies monotonically and changes sign as ΔT crosses zero, serving as a measure of the mismatch. The scheme can readily be extended to more than two channels.

If operating at full speed, the two digital multipliers in Fig. 16(c) may consume substantial power. Fortunately, the two products, $P_{1,2}$ and $P_{2,1}$, need not be updated at full rate. That is, the multiplications can be repeated much less frequently than the clock speed, minimizing the power consumption of the logic. This approach is realized in Fig. 18(a), where a behavioral model includes a timing mismatch between CK and $\overline{CK}$, the proposed ΔT computation scheme, a register, a DAC, and an analog variable-delay line (VDL). The ΔT computation proceeds for 8,000 clock cycles at full speed, driving the VDL with negative feedback, and then rests for 10^6 cycles. This operation is repeated, producing the behavior shown in Fig. 18(b), where the mismatch between CK and $\overline{CK'}$ is plotted. (The time difference between iterations is 10^6 cycles.) We observe that the loop drives the mismatch toward small values and can correct for slow changes, e.g., due to temperature variations.



(a)



(b)

Fig. 18. (a) Proposed background calibration method, and (b) its convergence behavior.

Acknowledgment The author wishes to thank Wood Chiang and Hegong Wei for their contributions to the proposed calibration technique.

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