The Future of Radios

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Abstract

The average smart phone user picks up the device 1,500 times a week. Wireless communication appears to be taking over our lives but it also presents interesting challenges to RF designers. This paper contends that the mobile terminal will emerge as a central command post for most of our daily affairs and will therefore sustain an increasingly heavier load in terms of speed, power dissipation, and cost. Low-voltage, low-power universal radios will thus become an essential component to meet future communication demands.

I. Introduction

It is a cold morning. You get into your car and mutter, "Office." While the car begins to navigate the road, you remember today is your spouse's birthday, whip out your iPhone15, and order a gift, knowing that a drone will drop it off in the afternoon. Now you can catch up with the day's news during the 30-minute drive to your office, watching videos streaming down from microsatellites up in the heavens. It is the year 2025. Isaac Asimov would have been proud.

Whether or not technology giants such as Google, Apple, and Amazon will bring this vision to reality, they and most other elements of our civilization will increasingly rely on wireless communication. This paper offers perspectives on how the radios in our wireless world will evolve and what challenges they will present to RF designers.

Section II ponders the reasons for the integral role of the mobile terminal in our daily lives and Section III describes trends in universal receiver (RX) design. Section IV deals with the problem of high-efficiency transmitter (TX) design and reviews possible solutions for future systems. Section V is concerned with phase noise in RF synthesizers.

II. Mobile Terminal as Central Command

The mobile terminal is likely to further widen its role in our lives and serve as a central command post. It will pay our bills, control our homes, direct our vehicles, communicate our vital signs, and possibly transmit our thoughts.

A fairly clear trend in wireless technology is that it will allow us to speak less and text more; to read less and watch more. That is, the general user will shy away from the spontaneous production of speech and its associated nuances in favor of calculated text, and from the taxing task of *reading* to the less demanding alternative of watching videos.[1] We can therefore predict that the mobile terminal will require exceedingly faster links.

While attractive (and frightening), the omnipotent mobile terminal must come to fruition with negligible increase in cost or power consumption. The task of integration thus assumes new dimensions. Today's mobile phones must accommodate up to 15 frequency bands, employing off-chip filters and duplexers whose cost and form factor far exceed those of the radio chip; tomorrow's phones will more severely face such issues.

These observations suggest three trends in mobile terminal design: (1) the use of "universal radios," radios that seamlessly accommodate many bands with minimal overhead and operate with higher data rates; (2) omission of off-chip filters through architecture innovations; and (3) greater emphasis on low power consumption. The migration of networks toward picocells and the wider availability of WiFi as a supplement to cellular links will particularly help reduce the mobile's transmitter (TX) power drain, but low-power techniques are still needed for the remainder of the transceiver.

III. Universal Radio Receivers

The universal radio can be viewed as the pinnacle of RF design, a transceiver that subsumes cognitive and software-defined radios and operates from tens of megahertz to about 10 GHz - possibly even up to millimeter-wave frequencies. Additionally, it would provide concurrent reception of multiple channels (carrier aggregation) as well. The feasibility of such a system is dictated by primarily the cost, power consumption, and form factor. For example, the number of on-chip inductors must be minimized and preferably reduced to zero. In this section, we examine several receiver architectures as potential candidates for universal radios.

A. Translational Receivers

The resurgence of "translational" circuits (also known as "commutated" networks or N-path filters) in recent years has dramatically changed the RF design landscape. Dating back

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[1] Of the 6 billion hours of video watched on Youtube every month, 40% are downloaded by mobile devices [youtube.com].

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to the 1940s [1] and the 1950s [2, 3], these circuits offer three critical properties that were considered impossible to achieve in the 1990s and early 2000s: bandpass filtering with a *precise*, *programmable* center frequency and an *arbitrarily high* Q.

Translational circuits have shifted the RF design paradigm in several directions: (1) in a manner similar to software-defined radios, they provide great flexibility in band and channel selection; (2) they allow channel-selection filtering near or at the antenna, relaxing the linearity of subsequent stages; and (3) they can suppress large blockers near or at the antenna. Of particular interest in mobile terminal design is this last attribute as it obviates external front-end filters, thus reducing the cost and form factor considerably.

A translational circuit can be modeled as shown in Fig. 1, where input X is downconverted, applied to a transfer function, and subsequently upconverted to produce Y. As a result, $Y/X = H(s - 2\pi f_{LO})$, i.e., $H(s)$ is translated to a center frequency of f_{LO}. Interestingly, X and Y need not appear at different ports. In Fig. 1(b), for example, I_{in} is downconverted, applied to the capacitors, and upconverted through the same switches, thereby generating V_{out}. One can also view such an operation as translation of impedances rather than transfer functions.

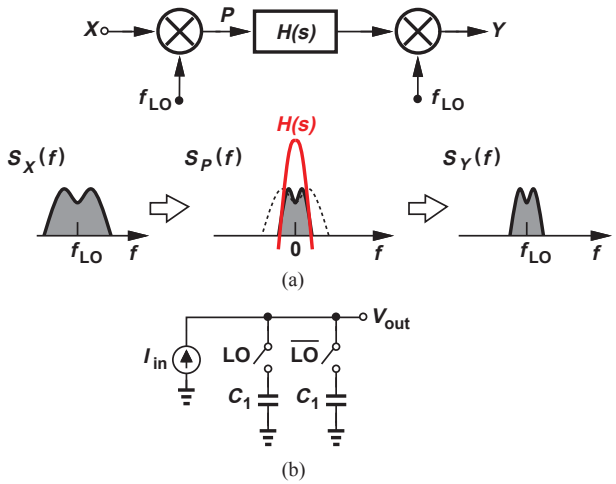

Fig. 1. (a) General translational system, and (b) simple implementation.

The topology of Fig. 1(b) exemplifies "current-driven" mixers [4], but translation properties only require that the time constant associated with the charge and discharge of the capacitors be much longer than the LO period, $T_{LO} = 1/f_{LO}$. In other words, the transformation depicted in Fig. 2 produces a significant translated response around f_{LO} filter if $R_S C_1 \gg T_{LO}$. This condition ensures that the voltage at node X changes by a small amount each time one switch turns on, thus creating a harmonically-rich voltage waveform at this node. From another perspective, if $R_S \rightarrow 0$, then $V_{out} \approx V_{in}$ and no translation occurs.

Three properties of the circuit shown in Fig. 2(b) are of interest. First, the two-sided -3-dB bandwidth of $|V_{out}/V_{in}|$ around f_{LO} is approximately equal to $(\pi N R_S C_1)^{-1}$, where N denotes the number of capacitor branches (driven by nonoverlapping LO phases) [3]. Second, as the frequency departs

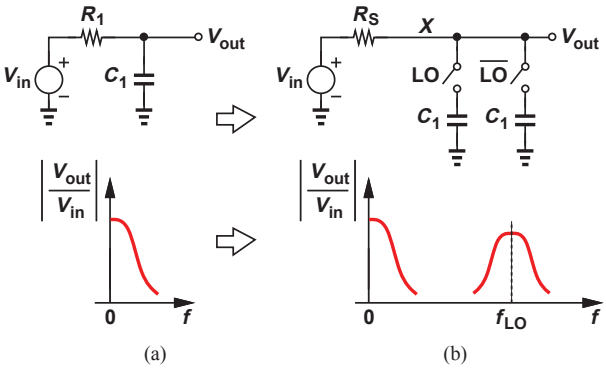

Fig. 2. Transformation of low-pass filter to band-pass filter using commutated capacitors.

significantly from f_{LO}, $|V_{out}/V_{in}|$ asymptotically approaches $R_{sw}/(R_{sw} + R_S)$, where R_{sw} is the on-resistance of each switch. That is, the out-of-channel rejection is limited by R_{SW}. Third, in the presence of large blockers, the switches exhibit substantial nonlinearity, introducing intermodulation products or amplitude demodulation.

In order to appreciate the challenges that we face in pushing the performance of translational circuits, let us assume, hypothetically, that the circuit of Fig. 2(b) is designed to perform channel selection and blocker rejection *at the antenna*. In GSM, for example, a channel bandwidth of 200 kHz must be achieved and a 0-dBm blocker at 20-MHz offset tolerated. With an antenna impedance of 50 Ω, we have $NC_1 \approx 32$ nF and for 20-dB rejection of the blocker, we obtain $R_{sw} \approx 5\ \Omega$. Such a low switch resistance translates to very wide devices and hence substantial power consumption in the LO distribution network. Moreover, a 0-dBm blocker (corresponding to a Thevenin antenna voltage of 1.264 V_{pp}) creates substantial nonlinearity in the switches.

A key observation here is that small-signal channel-selection filtering does not necessarily imply blocker tolerance and vice versa. The former requires large capacitors and wide switches and the latter, sufficient linearity.

Figure 3 depicts an example of channel-selection filtering by means of translational circuits [5]. By means of four nonoverlapping LO phases, the downconverted signal is amplified, converted to current, applied to a high-pass filter (HPF), and upconverted. The circuit achieves a bandwidth of 5 MHz at

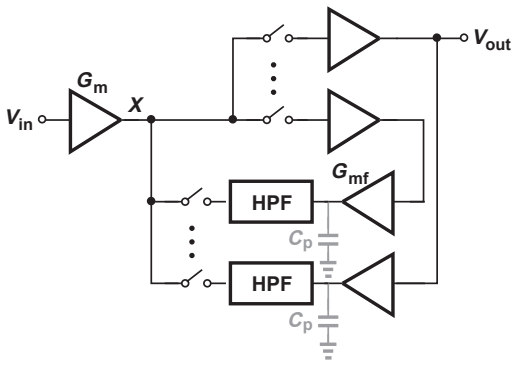

Fig. 3. Example of translational circuit with narrow channel bandwidth.

node X through the use of large capacitors in the HPF, but their parasitics introduce a pole at the output of each G_{mf} stage, potentially causing instability or unwanted peaking in the frequency response. This issue necessitates a high G_{mf} and translates to an overall power dissipation of 62 mW [5]. The loop amplifiers may also saturate in the presence of a large blocker.

An example of blocker rejection using translational circuits is shown in Fig. 4 [6]. Here, two such networks are attached in

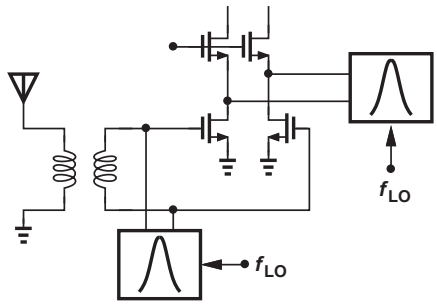

Fig. 4. Example of receiver with RF blocker rejection filtering.

parallel with the signal path, one at the LNA input and one at the cascode nodes. With the aid of the translated impedances (and N-path filters at the output), the circuit exhibits a channel bandwidth of 14 MHz and a noise figure of 11.4 dB in the presence of a 0-dBm blocker at 80-MHz offset [6].

In order to arrive at another receiver architecture, let us consider the continuous-time integrator shown in Fig. 5(a), where

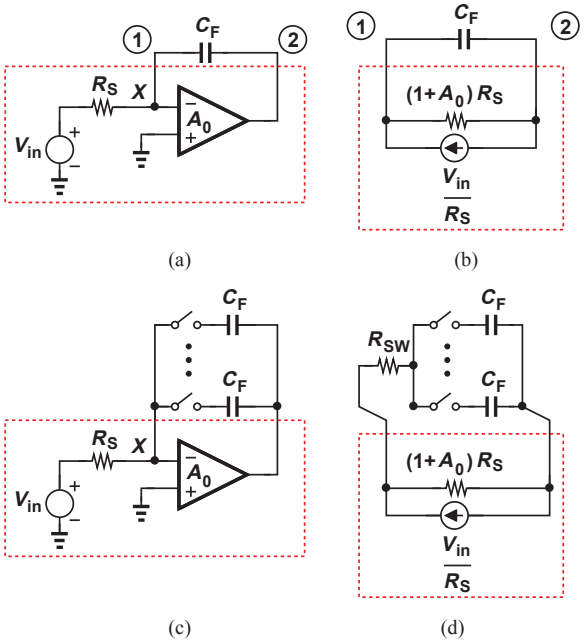

Fig. 5. (a) Integrator, (b) equivalent circuit, (c) use of commutated capacitors in feedback, and (d) equivalent circuit.

R_S sees a capacitance equal to $(1 + A_0)C_F$. An alternative viewpoint here is to replace the circuit in the dashed box with its Norton equivalent [Fig. 5(b)] and recognize that C_F sees a source resistance equal to $(1 + A_0)R_S$. This new view of the Miller effect proves useful in our front end design.

We now replace C_F in Fig. 5(a) with commutated capacitors as shown in Fig. 5(c). The circuit in the dashed box is a linear, time-variant system and still lends itself to a simple Norton equivalent [Fig. 5(d)]. Compared to the arrangement in Fig. 2(b), this topology benefits from a higher source impedance by a factor of $1 + A_0$, thereby providing a proportionally narrower channel bandwidth, $[\pi N(1 + A_0)R_S C_F]^{-1}$, and greater far-out suppression, $R_{sw}/[R_{sw} + (1+A_0)R_S]$ [7]. Consequently, the total area consumed by the capacitors and the width of the switches can be reduced by a factor of $1 + A_0$.

Figure 6(a) shows an implementation of the foregoing "Miller

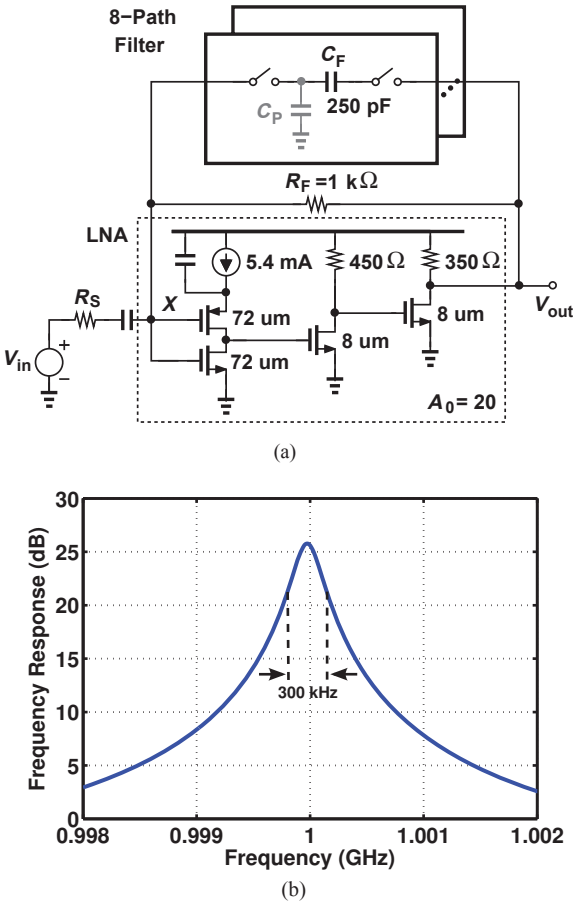

Fig. 6. (a) Use of double-switch translated notch filter in feedback around LNA ($L = 65$ nm for all transistors), (b) resulting frequency response.

bandpass filter" using a three-stage LNA. With an LNA gain of about 20, the eight commutated capacitors add up to about 2 nF for a channel bandwidth of a few hundred kilohertz. Since the parasitics of the capacitors, C_p, can load the RF signal significantly, they are upconverted by means of the switches on the left. The feedback resistor, R_F, establishes input matching with negligible noise contribution. The frequency response plotted in Fig. 6(b) reveals a -3-dB bandwidth of 300 kHz and a far-out rejection of more than 25 dB.

We must now examine the above front end for blocker rejection purposes. If the LNA input acts as a virtual ground at the blocker frequency, the large blocker current (e.g., 632 $\text{mV}_p/50\ \Omega = 12.64\ \text{mA}_p$ for a 0-dBm blocker) must flow

through the feedback network and be absorbed by the last stage of the LNA. This current level, however, is far too high for this stage. Consequently, the LNA experiences large input voltage swings, the last two stages saturate, the equivalent loop gain falls dramatically, and the noise figure rises from 2.1 dB to 12 dB.

Figure 7 depicts the modified front end for tolerance of

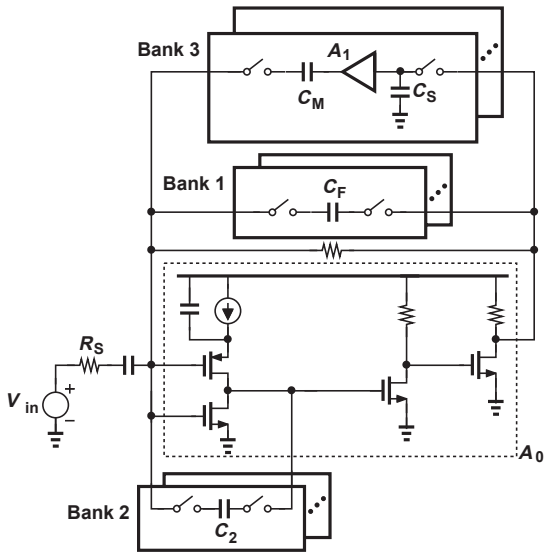

Fig. 7. (a) Use of Miller bandpass filter to increase apparent value of capacitors and shape the response, (b) implementation of zeros within A_1.

blockers [7]. A second bank of commutated capacitors around the first stage attenuates the blocker so as to avoid compressing the last two. The third bank incorporates an amplifier to further increase the Miller effect of C_M's and hence achieve the desired channel bandwidth with a total capacitance of 2 nF. Note that the receive path needs no inductors.

Figure 8(a) shows the measured characteristics of the receiver developed above [7]. Programmable capacitor arrays permit configurability for GSM (with $f_{LO} = 1$ GHz), WCDMA (with $f_{LO} = 2$ GHz), and IEEE802.11b/g ($f_{LO} = 2.5$ GHz). It is observed that the receiver provides at least 16 dB of rejection in the alternate adjacent channel. Figure 8(b) plots the measured noise figure as a function of the power of a blocker at 20-MHz offset. The NF rises from 2.9 dB to 5.1 dB.

Since commutated networks produce translated responses at harmonics of the LO, they can downconvert blockers at these frequencies and corrupt the baseband signal. An interesting approach to harmonic blocker rejection employs in the baseband signal path a tank resonating at $4f_{LO}$ (Fig. 9) [8]. Viewed from the RF port, this impedance creates resonances at $3f_{LO}$ and $5f_{LO}$, thus reducing the current carried by the switch at these frequencies and hence suppressing the downconversion of harmonic blockers. In addition to requiring an inductor, this method also faces difficulties if a wide range of input and LO frequencies must be accommodated.

An alternative technique is illustrated in Fig. 10(a) [9]. Seeking to raise the input impedance at $3f_{LO}$ to infinity, the 120° phases ensure that the total charge delivered to each ca-

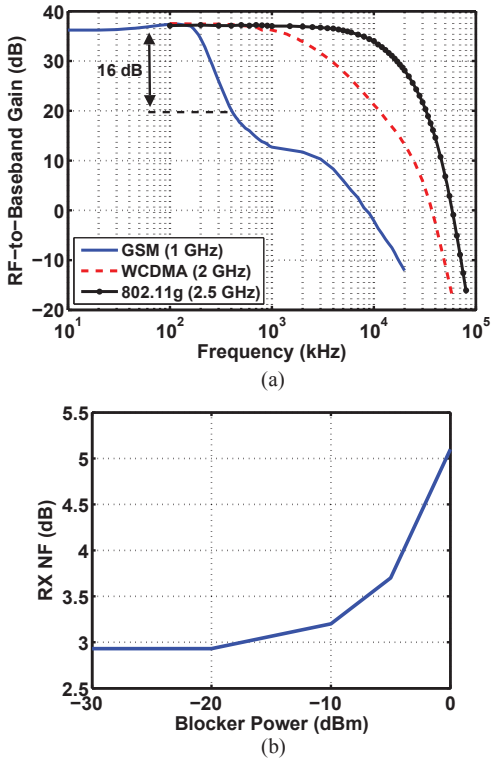

Fig. 8. (a) Measured frequency response of receiver with different capacitor settings, (b) measured noise figure as a function of blocker level at 20-MHz offset.

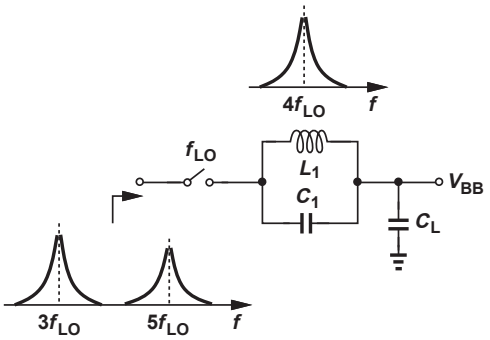

Fig. 9. Receiver with rejection of harmonic blockers.

pacitor for a sinusoidal input at this frequency is equal to zero. Depicted in Fig. 10(b), the first and third harmonic responses exhibit a suppression of about 46 dB at $3f_{LO}$. The LO phases can be generated by injection-locking a ring oscillator to the main oscillator in a manner similar to [10] or by interpolation between quadrature phases.

B. Digitization Near Antenna

A holy grail in RF receiver design has been to place the A/D interface near the antenna, aiming for a "software radio," one where the received signal is digitized before downconversion. Unfortunately, the very demanding requirements of wireless standards have not allowed this approach to compete with other receiver designs—at least not yet. Baseband ADCs can achieve a wide dynamic range but face additional issues if they are moved to the RF domain: (1) noise folding and spurious

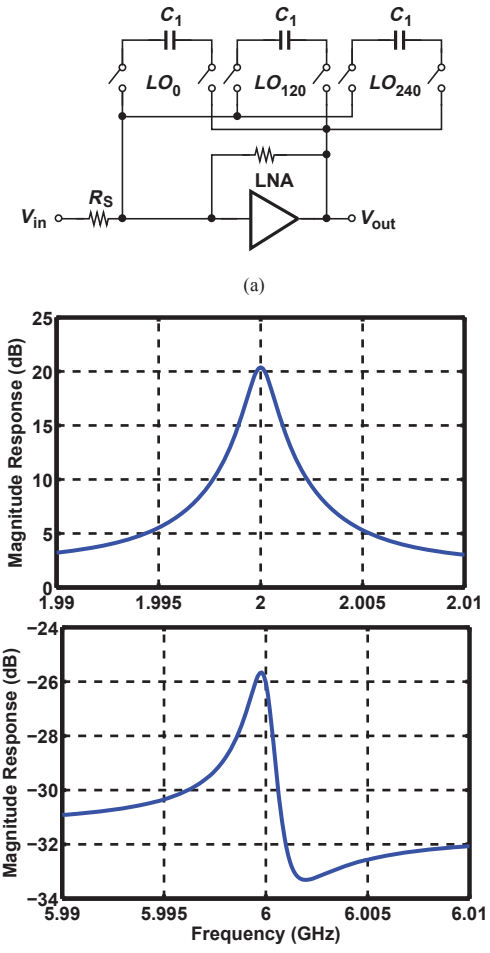

Fig. 10. (a) LNA using harmonic-rejection translational circuit, (b) simulated responses around first and third harmonics.

components in the case of undersampling, (2) high power consumption in the case of oversampling, and (3) thermal noise floor andd blocker tolerance in all cases.

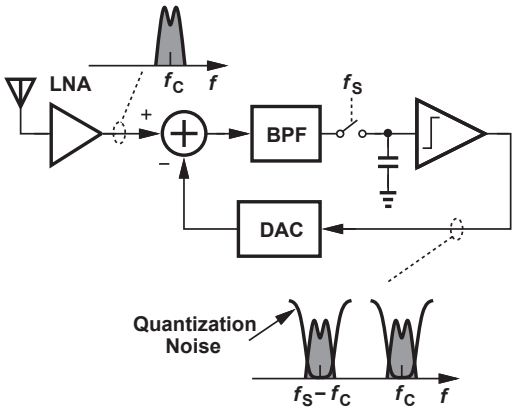

Fig. 11. Receiver using a band-pass Σ-Δ modulator.

One approach is to employ continuous-time band-pass Σ-Δ converters to digitize the desired RF signal while rejecting other components [11, 12, 13, 14]. As depicted in Fig. 11 [12], the amplified RF signal at f_C is applied to a noise-shaping loop sampling at a rate of f_S. The digitized output therefore contains the signal around $f_S - f_C$ with the quantization noise shaped away from this frequency. The BPF bandwidth must be small enough to suppress unwanted components and has been realized using LC filters. Moreover, the filter and DAC noise must be minimized. An interesting technique draws upon the properties of translational circuits so as to implement a relatively narrowband filter [14]. Consuming 80 mW, the receiver exhibits a noise figure of 6.2 dB, which rises to 16 dB with a blocker level of −18 dBm at 80-MHz offset.

C. Low-Power Techniques

A number of general approaches to reducing the power consumption of receivers can be envisaged. First, channel-selection filtering close to the antenna—as exemplified by the front ends in Figs. 3 and 7—relaxes the RX chain linearity, affording a more favorable trade-off between noise and power dissipation. Second, with the advent of low-power, high-resolution ADCs, it is now possible to minimize the number of analog RX stages. Third, new low-power techniques can be applied to the design. An interesting example is reported in [15] and illustrated in Fig. 12. Beginning with the translational circuit in Fig. 12(a), this work recognizes that the baseband transimpedance amplifiers (TIAs) can be merged with the LNA, leading to the "recycling" topology shown in Fig. 12(b). We can also say that the downcoversion performed by the feedback switches in Fig. 12(a) produces the baseband signal at X. That is, the LNA amplifies both the RF and the downconverted signals.[2]

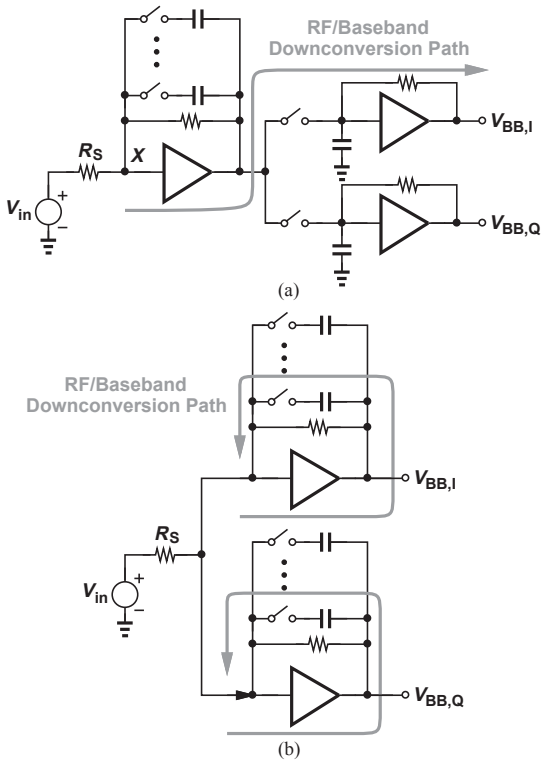

Fig. 12. (a) Band-pass front end followed by mixers and TIAs, and (b) recycling of the downconverted signal through the front end.

[2]A single amplifier can also serve this purpose as the baseband I and Q signals are available within each feedback network [7].

In applications requiring tolerance of large close-in blockers (e.g., IEEE 802.11a/b/g), the high-order analog baseband filters can draw substantial power. In order to relax the noise-linearity-power trade-offs of such filters, the concept of "non-invasive filtering" can be utilized [16, 17]. Illustrated in Fig. 13(a), the idea is to introduce the filtering components *in parallel* with the signal path so that they contribute negligible noise and nonlinearity within the channel bandwidth. Figure 13(b) shows an implementation employing an integrator and a gyrator. These two stages create a series resonance at a frequency given by $1/[2\pi\sqrt{C_F C_L/(G_{m2}G_{m3}}]$, which can be placed in the middle of the blocker channel. A fourth-order design satisfying IEEE802.11a/g requirements draws 4.3 mW while exhibiting an input-referred noise voltage of 2 nV/$\sqrt{\text{Hz}}$ [17].

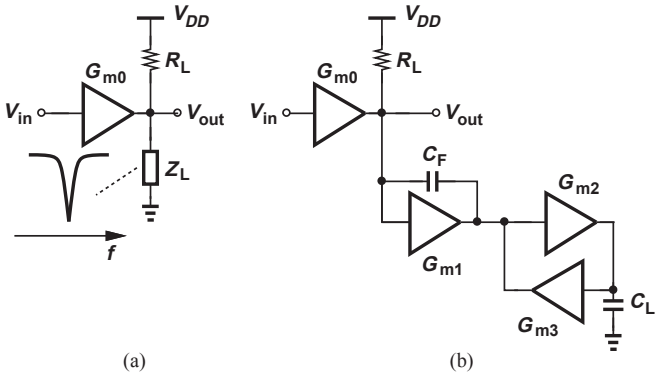

Fig. 13. (a) Gain stage with notch impedance at output, and (b) actual implementation.

IV. Transmitters

The principal challenge in transmitter (TX) design continues to lie in efficient, linear power amplification. While the gradual migration to picocells will allow smaller output power levels, the demand for high data rates will dictate higher-order modulation schemes and hence greater linearities.

Polar modulation has emerged as an attractive approach to TX linearization, but it must deal with two issues that may prove serious in future systems. First, the delay mismatch between the phase and envelope paths corrupts the reconstructed output signal [Fig. 14(a)]. For a signal of the form $V_{env}(t)\cos[\omega_0 t + \phi(t)]$, a delay mismatch of $\Delta T = T_{env} - T_{phase}$ produces an error given by $[\Delta T dV_{env}(t)/dt]\cos\omega_0 t + \phi(t)$. The corruption is therefore more pronounced if the envelope carries higher data rates. Approximating $V_{env}(t)$ by a flat spectrum with a bandwidth of f_{env}, we can estimate the normalized corruption as $\pi\Delta T f_{env}$, observing the severity of the mismatch problem in future systems.

Second, the PA output stage suffers from AM/PM conversion due to the variation of the drain capacitance, C_{DB}, with the envelope signal [Fig. 14(b)]. The PA phase variation can be approximated by $V_{env}(t)Q\omega_0^2 dC_{DB1}/dV_{env}$, where Q denotes the output matching network quality factor. This error can be reduced through the use of phase feedback [18] as shown in Fig. 14(c), but the PLL bandwidth and hence f_{REF} may need to be prohibitively large.

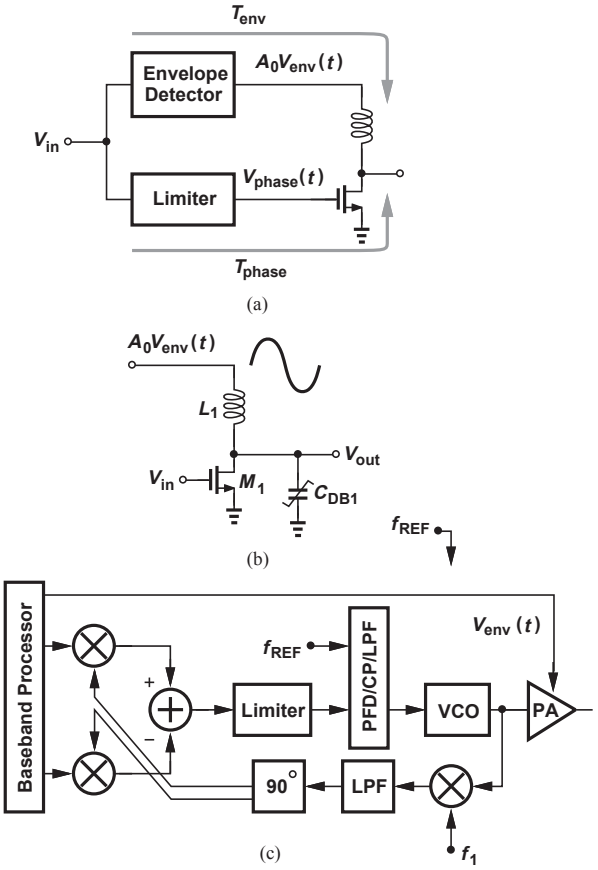

Fig. 14. (a) Problem of delay mismatch, (b) AM/PM conversion at the output, and (c) phase feedback to suppress AM/PM conversion.

The need for passive matching networks at the TX output makes it difficult to achieve wideband operation with a single PA. Nonetheless, the remainder of the TX can benefit from two trends in wideband design. This section describes these two trends.

A. Complex Predistortion

In view of the foregoing polar modulation issues, one can reevaluate other linearization techniques for wideband data. To correct for dynamic nonlinearities (e.g., AM/PM conversion), let us represent the system's memory by a delay t_1 and write, for example, $y(t) = \alpha_1 x(t-t_1) + \alpha_2 x^2(t-t_1)$; i.e., the output is corrupted by the square of the input from t_1 seconds ago. Shown in Fig. 15(a), this model simply reflects the first two terms of a Volterra series with an impulse response of $h(t) = \delta(t-t_1)$. In a more general case, we have $y(t) = \alpha_1 x(t-t_1) + \alpha_2 x^2(t-t_1) + \cdots + \alpha_n x^n(t-t_1) + \cdots + \beta_1 x(t-t_2) + \beta_2 x^2(t-t_2) + \cdots + \beta_m x^m(t-t_2) + \cdots$ [19]. Dynamic nonlinearities can therefore be corrected as shown in Fig. 15(b) [19]. Here, the signal is delayed by various values, which upon calibration, represent t_1, t_2, etc., and subsequently applied to polynomials modeling the inverse functions of $\alpha_1 x(t-t_1) + \alpha_2 x^2(t-t_1) + \cdots$, $\beta_1 x(t-t_2) + \beta_2 x^2(t-t_2) + \cdots$, etc. The work in [19] realizes these operations in the analog domain and

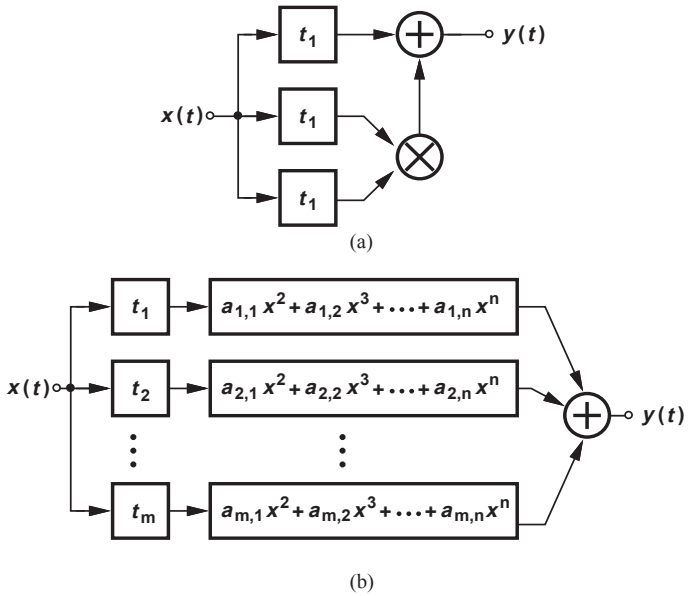

Fig. 15. (a) Simple dynamic nonlinear model, (b) predistortion to suppress dynamic nonlinearities.

must deal with issues such as signal amplitude and bandwidth expansion due to higher-order terms. However, with recent advances in DAC design, it is possible to move the operations to the digital domain.

One disadvantage of predistortion is its inability to correct for abrupt nonlinearities, e.g., those arising from a switching output stage. This issue disappears if the PA itself is realized in the digital domain! The next section ponders this possibility.

B. DAC-Based Transmitters

RF transmitters seem to be progressing toward the original software radio faster than RF receivers are. Depicted in Fig. 16(a), a software radio TX ideally consists of only a

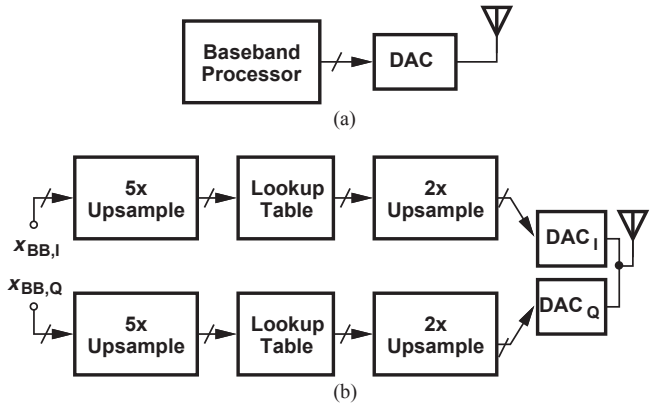

Fig. 16. (a) Ideal digital transmitter, and (b) implementation example.

baseband processor and an RF DAC that directly drives the antenna. The DAC is naturally implemented by current steering and must satisfy several requirements: (1) sufficient linearity to avoid significant intermodulation, out-of-channel emission, and harmonics, (2) fast, linear settling, (3) a large output current with minimal voltage headroom, and (4) low out-of-band thermal noise. An example of such an architecture is shown in Fig. 16(b), where a look-up table (LUT) preceding the DAC provides predistortion [20]. The transmitter upsamples the baseband signal by a factor of 5, thus reducing far-out noise, applies the result to the LUT, upsamples by another factor of 2, and delivers the signal to the I and Q DACs. The DACs have a resolution of 13 bits.

The above TX calibrates the DAC nonlinearity offline by applying a training sequence and measuring the output. Based on the error between the output and the desired value, the LUT coefficients are adjusted [20]. For an IEEE 802.11g signal, this design delivers an output power of 18.8 dBm with an efficiency of 17% [20].

It is interesting to recognize that the digital TX eliminates from the analog domain the following functions: AGC, offset correction, I/Q calibration, upconversion mixers, and PA predrivers. It also avoids the polar modulation issues.

V. Frequency Synthesis

The vast field of frequency synthesis does not lend itself to a brief overview here, but one aspect of the problem, namely, the phase noise, has led to interesting developments. Beginning from the 1990s, phase noise reduction has been pursued at different levels of abstraction: at the device level (by seeking inductors with higher quality factors), at the circuit level (by developing low-noise oscillators, e.g., as in [21, 22]), and, more recently, at the synthesizer and transceiver levels. We consider examples of the last two.

An interesting approach deals with one consequence of phase noise in receivers, namely, reciprocal mixing, and cancels the effect by feedforward. Recognizing that symmetric phase noise components around the carrier are correlated, this method reconstructs the phase noise around a downconverted blocker and subtracts it from the original composite baseband signal [23]. As shown in Fig. 17, an additional path re-

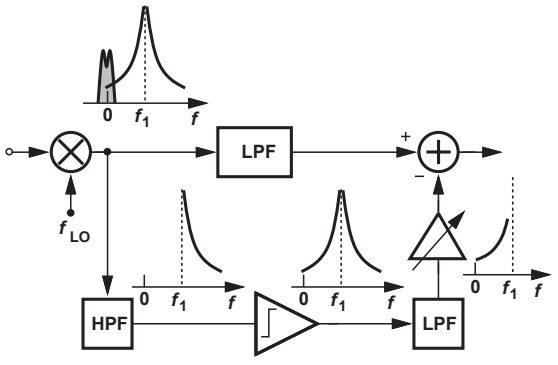

Fig. 17. Reciprocal mixing cancellation using feedforward.

moves the desired channel by a high-pass filter (HPF), the AM component by a limiter, and the blocker itself by a low-pass filter (LPF). The result is then scaled and subtracted from the downconverted components in the main path, leaving only the desired signal.

The above technique exemplifies correction at the transceiver level, but it does not remove the effect of phase noise on the

signal constellation; nor does it apply to transmitters.

At the synthesizer level, the bandwidth of type-II PLLs is limited by stability constraints to about $f_{REF}/10$, where f_{REF} is the input frequency. In practice, low spur levels dictate bandwidths on the order of $f_{REF}/20$, thus limiting the extent to which the VCO phase noise can be suppressed. This trade-off rules out ring oscillators and their benefits: the ability to cover decades of frequency range, especially by multiplexing of several rings, straightforward generation of multiple phases, and less coupling to and from other circuits. It is possible to depart from the type-II topology so as to avoid its limitations. Figure 18 depicts an example [24] where a type-I PLL incorporates a

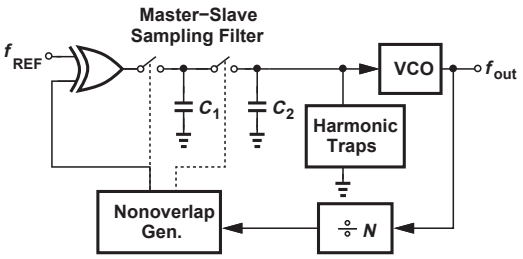

Fig. 18. Synthesizer with bandwidth approaching $f_{REF}/2$.

master-slave sampling loop filter to achieve a bandwidth close to $f_{REF}/2$, thereby suppressing the phase noise of the ring VCO and meeting the requirements of 2.4-GHz standards. In order to reduce the reference spurs, two "harmonic traps" in the form of simulated series LC resonances are tied to the oscillator control line and tuned to f_{REF} and $2f_{REF}$. The synthesizer draws 4 mW and exhibits a phase noise of -114 dBc/Hz at 1-MHz offset and sidebands below -65 dBc.

VI. Conclusion

Wireless communication continues to evolve and pervade, demanding universal radios with an exceedingly higher performance and a lower cost. Attractive choices for such radios include receivers employing translational circuits and transmitters using complex predistortion and RF DACs. The task of frequency synthesis for a wide frequency range also poses its own challenges and calls for inductorless oscillators whose phase noise is suppressed at the architecture level.

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