A 10-Bit 800-MHz 19-mW CMOS ADC

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Abstract—A pipelined ADC employs charge-steering op amps to relax the trade-offs among speed, noise, and power consumption. Applying full-rate nonlinearity and gain error calibration, a prototype realized in 65-nm CMOS technology achieves an SNDR of 52.2 dB at an input frequency of 399.2 MHz and an FoM of 53 fJ/conversion-step.

The concept of charge steering has been recently revived as a means of achieving low power dissipation at high speeds [5]. While not identified as such, this concept has also been utilized in amplifiers in [6] and [7] but only for linearities of around 6 bits. This paper describes a 10-bit pipelined ADC that employs circuit and architecture techniques to improve the linearity and noise performance of charge-steering op amps while maintaining their high power efficiency.

Charge-steering Op Amp A conventional two-stage op amp is transformed to a charge-steering topology as shown in Fig. 1 (a). When CK is low, C_1-C_4 are precharged to V_{DD} and the tail nodes float. When CK rises, the output nodes are released and the tail nodes are connected to ground, causing differential and common-mode (CM) currents to be drawn by M_1-M_2 and M_3-M_4 from their respective loads. As the CM level at X and Y falls, M_3 and M_4 eventually turn off, and the two stages provide a certain differential voltage gain. Note that C_1 and C_2 are primarily determined by the first pipelined stage kT/C noise while C_3 and C_4 represent the input capacitors of the next pipelined stage. The basic charge-steering op amp faces three issues. (1) The open-loop voltage gain resulting from the two stages is quite limited. In this work, capacitors C_F are added to introduce positive feedback around the first stage, thus raising the gain from 10 to 13. (2) If utilized in a multiplying digital-to-analog converter (MDAC), this topology limits the closed-loop linearity to about 7 bits. The ADC reported here incorporates nonlinearity calibration in the digital domain to achieve 10-bit linearity. (3) The open-loop voltage gain and the nonlinearity of the circuit in Fig. 1 are sensitive to the input CM level. This ADC employs an analog/digital common-mode feedback loop along with R_{CM} in Fig. 1 to resolve this issue.

The superior performance of charge-steering op amps can be appreciated as follows. If designed for the same power dissipation, voltage gain, and load capacitance, a charge-steering topology exhibits half as much input noise power and a quarter as much settling time as a conventional two-stage op amp.

The closed-loop behavior of charge-steering op amps presents interesting and useful properties. As evident from the simplified model shown in Fig. 1 (b), the overall circuit resembles a loop containing two integrators, which become lossy if the output resistances are included. The step response would thus exhibit an overshoot, except that the output stage *turns* off around t_1. In other words, the closed-loop voltage gain can *exceed* C_{in}/C_M.

Architecture and Calibration The ADC consists of 12 1.5-bit stages and one 1-bit stage, with the first five scaled down by a factor of 2 so as to save power. Using a high-precision on-chip ladder [8], the ADC performs foreground calibration and corrects, in the digital domain, the nonlinearity of the first four stages and the gain error of all of the stages by means of polynomial inverse functions [8]. The calibration begins with the last stage and proceeds backwards. Since the charge-steering op amp is somewhat sensitive to the input common-mode level, it is desirable to calibrate the second stage with an input CM voltage equal to the first stage output CM level. To avoid CM mismatches between the calibration and operation modes, the ADC calibrates the first and second stages as *one* block. Illustrated in Fig. 2, the idea is to apply 31 "golden" voltages produced by the ladder and adjust the α and β coefficients using an LMS algorithm so as to minimize the error D_{err}.

The use of a ladder with 31 taps limits the clock speed at which the ADC can be calibrated unless all 31 switches tied to the ladder are bootstrapped. This work introduces a clock gating method to avoid this issue. As shown in Fig. 3, a divided version of the clock is used to control the sampling and amplification phases: C_{in} remains connected to the ladder for $T_{samp} = 16T_{CK}$ seconds and subsequently switches to ground for $T_{CK}/2$ seconds. Thus, the circuit samples an accurate voltage and generates a result that contains the dynamics at the full rate.

CM Feedback As mentioned above, the gain and nonlinearity of charge-steering op amps are sensitive to the input CM level, an issue that perhaps does not manifest itself at lower resolutions [6, 7] but must be addressed in our work. The discrete-time nature of the circuit makes it difficult to measure and correct for CM level variations by mean of conventional techniques. Instead, we propose a mixed-signal method by recognizing that the ultimate purpose of CM control is to minimize the ADC's distortion. Specifically, in minimizing D_{err} in Fig. 3, we can adjust not only the α and β coefficients but also the analog CM level(s) within the op amp. To this end, the tail resistor R_{CM} in Fig. 1 (a) is programmable in 16 steps and is varied by the LMS machine, establishing the optimum output CM level after the LMS loop settles.

Experimental Results The ADC has been fabricated in 65-nm digital CMOS technology and tested with a 1-V supply. Figure 4 shows the die photo. The back-end digital calibra-

tion is performed off-chip. The prototype consumes 19 mW, of which 6.2 mW is drawn by the analog section, 11.1 mW by the digital section, and 1.4 mW by the references.

Figure 5 plots the DNL and INL before and after calibration, and Fig. 6 shows the SNDR as a function of the input frequency at f_s = 800 MHz. Table I summarizes the performance of this prototype and state-of-the-art 10- to 12-bit ADCs operating around the same speed.

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References

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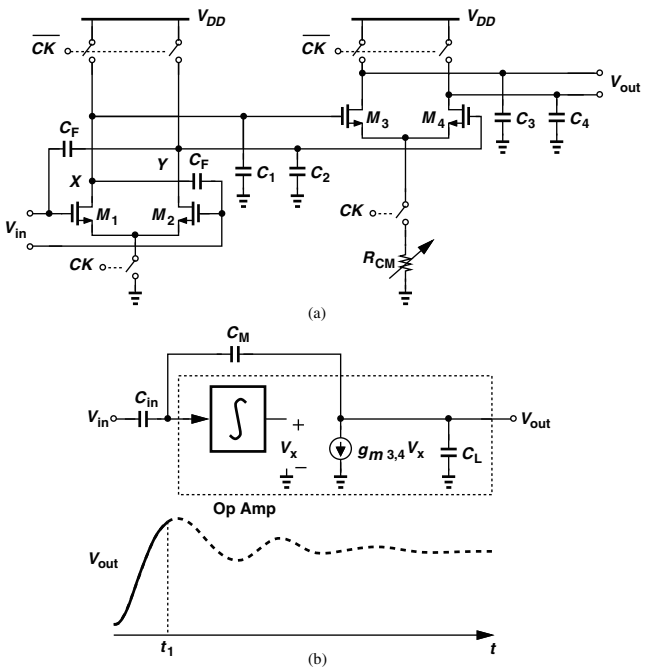

Fig. 1. (a) Charge-steering op amp and (b) its closed-loop model.

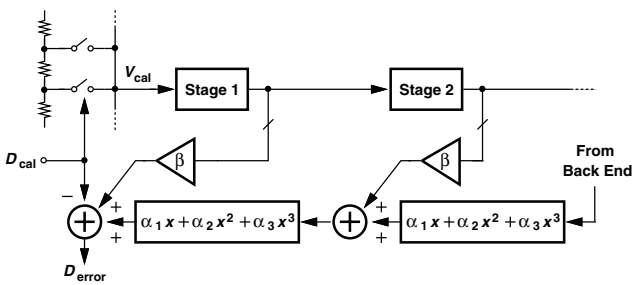

Fig. 2. Calibration of first two stages as one block.

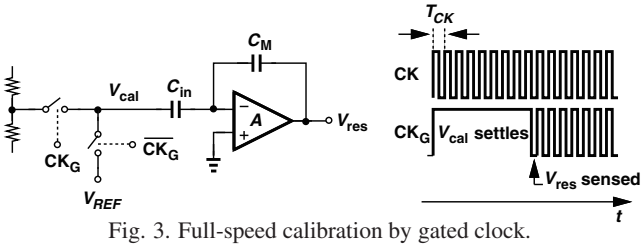

Fig. 3. Full-speed calibration by gated clock.

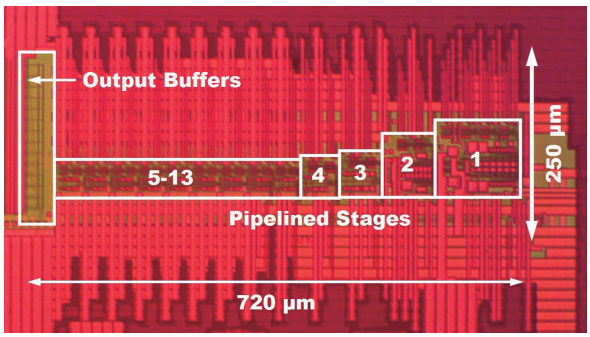

Fig. 4. ADC die photograph.

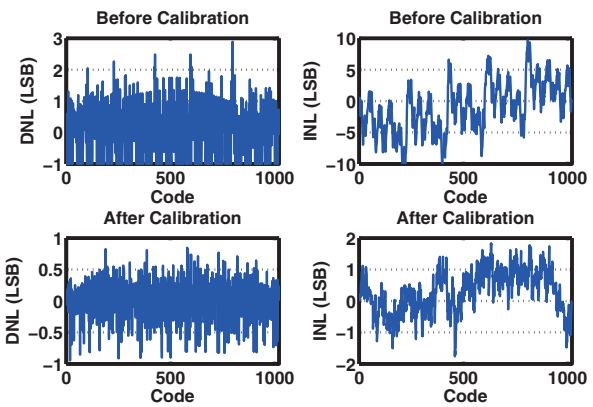

Fig. 5. DNL and INL before and after calibration.

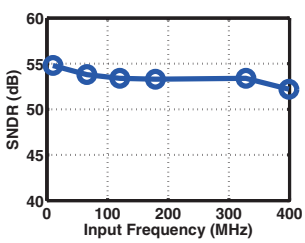

Fig. 6. Measured SNDR at a sampling rate of 800 MHz .

	[1]	[2]	[3]	[4]	This Work
Sampling Rate	1000 MHz	800 MHz	1000 MHz	1000 MHz	800 MHz
Power	575 mW	105 mW	36 mW	33 mW	19 mW
SNDR @ Nyq.	59.0 dB	59.0 dB	52.7 dB	52.4 dB	52.2 dB
FoM* (fJ/conv.)	553	180	70	93	53
FoM** (fJ/conv.)	790	180	102	97	71
Resolution	12 b	12 b	10 b	10 b	10 b
Area (mm^2)	2.350	0.880	0.175	0.225	0.180
Supply	1.8 / 3.3 V	1.0 / 2.5 V	1.2 V	NA	1.0 V
Technology	180 nm SiGe	40 nm	65 nm	65 nm	65 nm

* $P/(2^{ENOB@DC} \min\{f_s, 2ERBW\})$
** $P/(2^{ENOB@Nyq} f_s)$

TABLE I
Performance summary and comparison.