A 27-73 GHz Injection-Locked Frequency Divider

Hossein Razavi and Behzad Razavi
Department of Electrical and Computer Engineering, University of California, Los Angeles, CA, 90095, USA
shrazavi@ucla.edu

Abstract — A new model for injection-locked dividers leads to a 4.76-mW prototype that operates from 24 GHz to 73 GHz with no need for tuning or adjustments. Occupying an area of 0.037 mm^2, the circuit can robustly serve millimeter-wave radios as well as full-rate 28-Gb/s, 56-Gb/s and half-rate 112 Gb/s wireline transceivers.

Injection-locked frequency dividers (ILFDs) continue to find application as both wireless and wireline transceivers push for higher frequencies. Since ring oscillators suffer from limited speed, only LC-based ILFDs emerge as a viable choice for input frequencies of tens of gigahertz. Unfortunately, however, such topologies exhibit a limited lock range, requiring either multiple oscillators whose outputs are multiplexed or heavy frequency tuning [1,2]. Both translate to substantial complexity, especially if a phase-locked loop must automatically determine whether an ILFD fails for a given input frequency.

Injection-Locking Analysis The divider reported here owes its performance to a new formulation of injection locking, offering insights that, to our knowledge, have not been heretofore discovered. We begin with the topology shown in Fig. 1(a) [3]. Prior analyses of injection locking have modeled the injector by a current source [3,4], but we recognize that transistor S_1 simply introduces a switched resistance between nodes X and Y. As such, the injection does not behave as either a current or voltage. We must fundamentally represent the divider by a linear, time-variant system. The half-circuit model is depicted in Fig. 1(b), where the on-resistance of the input switch is denoted by R_{sw}. We express the switch conductance as a Fourier series:

$$G_{sw}(t)=0.5G_0+(2/\pi)[G_0\sin(\omega_{in}t)+(1/3)G_0\sin(3\omega_{in}t)]+\dots],$$

where $G_0=1/R_{sw}$ and ω_{in} is the input frequency. We assume the output is of the form $V_{out}(t)=V_0\cos[(\omega_{in}/2)t+\varphi]$. The transconductance of one transistor can be written as [5]:

$$G_m(t)=G_{m0}+2G_{m2}\cos[2(\omega_{in}/2)t+2\varphi]+2G_{m4}\cos[4(\omega_{in}/2)t+4\varphi]+\dots .$$

In general, the output frequency departs from $\omega_0=1/\sqrt{L_1C_1}$ by $\Delta\omega$. Writing a KCL at the output node in Fig. 1(b) at $\omega=\omega_{in}/2$ yields two key equations:

$$1/R_p=G_{m0}-G_{m2}-G_0[1-(2/\pi)\sin(2\varphi)] \quad (1)$$

$$2\Delta\omega C_1=(2/\pi)G_0\cos(2\varphi) . \quad (2)$$

Note that $G_{m0}-G_{m2}$ is the effective transconductance of the cross-coupled pair at the first output harmonic.

Equations (1) and (2) stand in sharp contrast to the behavior of injection-locked oscillators (i.e., with a unity divide ratio), which exhibit a zero phase difference in the middle of the lock range. We observe that, as $\Delta\omega$ approaches zero, 2φ drops to 90°, indicating that the output zero crossings are surrounded by the input edges [Fig. 1(c)]. Moreover, the conventional view of injection-locked oscillators tells us that the phase difference reaches 90° at the edge of the lock range [6], but that is not true here! The remarkable point emerging from (1) and (2) is that proper choice of G_0 (i.e., the switch resistance) can endow a greater lock range by allowing 2φ to be less than 180°. This is the first insight offered by our work.

Eliminating φ from (1) and (2) gives:

$$\Delta\omega=\pm 1/(\pi C_1)G_0\sqrt{1-\pi^2/4[(G_{m0}-G_{m2}-1/R_p)/G_0-1]^2} .$$

This lock range reaches a maximum of

$$\Delta\omega_{max}/\omega_0=1/(\sqrt{\pi^2-4})\,(g_mR_p-1)/Q,$$

where Q is the quality factor of the tank. Also, we have utilized the fact that $G_{m0}-G_{m2}$ is approximately equal to the equilibrium transconductance, g_m, [when $V_X=V_Y$ in Fig. 1(a)] at the edge of lock. For this optimum to occur, G_0 must be chosen as

$$G_{0,opt}=[\pi^2/(\pi^2-4)](g_m-1/R_p).$$

It can be shown that $\Delta\omega_{max}/\omega_0$ is about 30% greater than the value obtained by simply assuming $2\varphi=180°$ at the edge of lock.

Quadrature Coupling The second key insight that we wish to present is that the lock range can be shifted to lower or higher frequencies if we inject a current into the tank(s) that is in quadrature with respect to the oscillation current. As illustrated in Fig. 2(a), with a new current $I_0\sin[(\omega_{in}/2)t+\varphi]$, the KCL at the output node still leads to (1), while transforming (2) to

$$2\Delta\omega C_1=(2/\pi)G_0\cos(2\varphi)+I_0/V_0 .$$

Notably, (1) prescribes the bounds for φ whereas the above equation suggests that $\Delta\omega$ can be shifted up or down by the term I_0/V_0. In fact, we can shift $\Delta\omega$ completely above the resonance frequency, ω_0, by selecting

$$(I_0/V_0)_{opt}=(2/\sqrt{\pi^2-4})(g_m-1/R_p) \quad (3)$$

Similarly, $\Delta\omega$ can fully shift below ω_0 if we simply change the sign of I_0 [Fig. 2(b)].

The forgoing thoughts suggest the need for either $I_0\sin[(\omega_{in}/2)t+\varphi]$ or $-I_0\sin[(\omega_{in}/2)t+\varphi]$ depending on whether the circuit must operate at very high frequencies or very low frequencies. Fortunately, this sign inversion occurs naturally in a quadrature oscillator and leads to the divider shown in Fig. 3. Here the phase relation between V_{X1}–V_{Y1} and V_{X2}–V_{Y2} changes from – 90° to + 90° for an output frequency below ω_0 or above ω_0, respectively. We note the similarity between this topology and that in [7] but remark the novelty expressed by (3), which allows to substantially increase the lock range. The total practical range extends from $0.6\omega_0$ to $\omega_0+1.7\Delta\omega_{max}$.

The input injectors in Fig. 3 are realized by an NMOS device and a PMOS device to allow testing with a single-ended input, a necessity at these frequencies given the limitations of external signal sources and baluns. In practice, the circuit

would be driven by a differential oscillator and hence both switches would be NFETs.

Experimental Results The frequency divider die photograph in 28-nm CMOS technology is shown in Fig. 4(a). Transistors M_1-M_8 in Fig.3 are realized with a width of 3.2 µm and a length of 30 nm. The coupling stages have a relative strength of 0.6. The prototype has been tested on a high-speed probe station and exhibits an unprecedented lock range of 3x, and greater than 100% according to the definition $2(f_{max} - f_{min})/(f_{max} + f_{min})$ [4]. Plotted in Fig. 4(b) is the measured input sensitivity as a function of frequency, revealing that the circuit operates correctly for most of the range with an input power less than – 4 dBm. Fig. 5 shows the input and output phase noise profiles at the center and upper edge of the lock range. As can be seen, this characterization is limited by the signal source's phase noise. The divider intrinsic phase noise is around – 138 dBc/Hz at 10 MHz offset.

References

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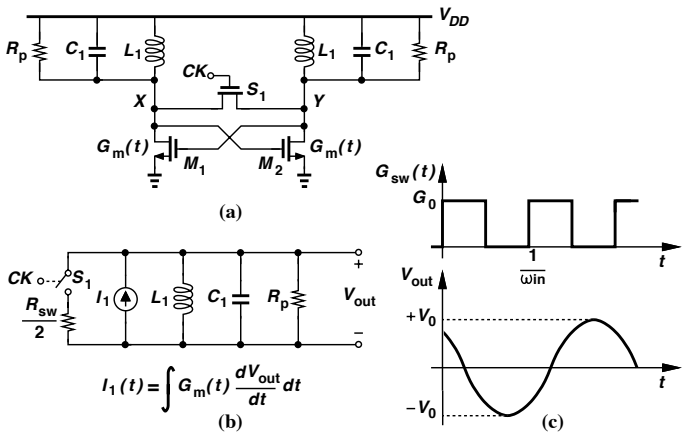

Fig. 1. (a) An ILFD, (b) its equivalent model and (c) input and output waveforms in the middle of the lock range.

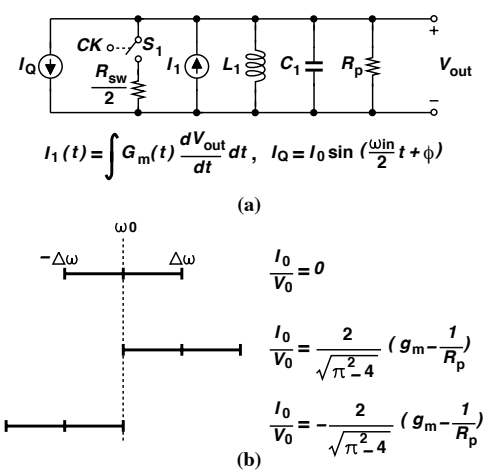

Fig. 2. (a) ILFD with added quadrature current and (b) lock range shift due to quadrature current.

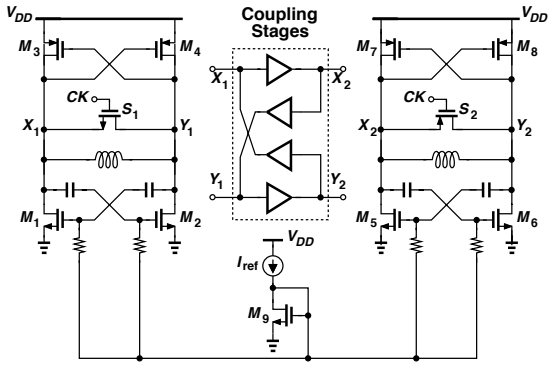

Fig. 3. Proposed divider architecture.

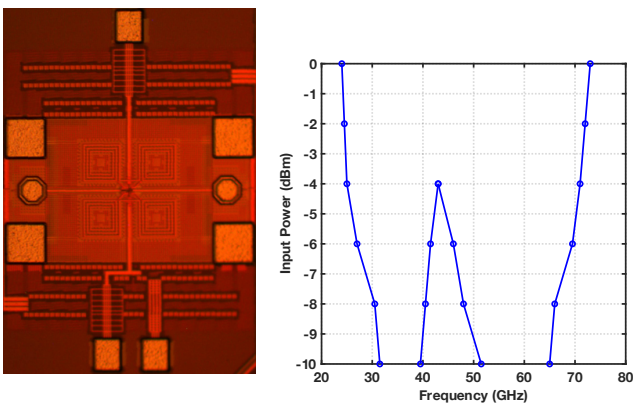

Fig. 4. (a) Divider die photograph and (b) measured divider sensitivity as a function of frequency.

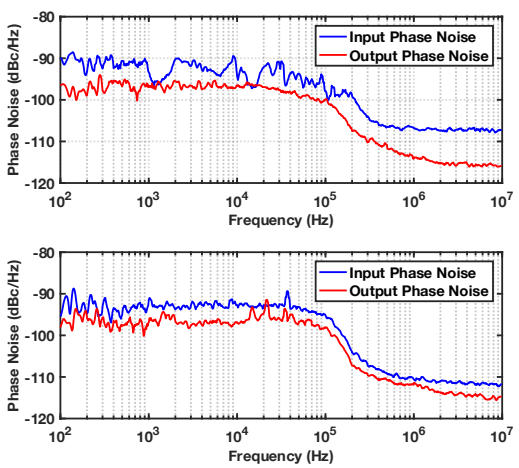

Fig. 5. Measured input and output phase noise for f_{in} = 45 GHz (top) and 73 GHz (bottom).

Table I. Performance summary

	[4][1]	Zhang[1], RFIC Symp., 2017	Chen[1], IMS, 2013	This Work[1]
Frequency [GHz]	12-32	27.9-53.5	25-53.6	24-73
Lock Range [%] [2]	90.9	62.9	72.7	101
P_{DC} [mW]	2.4	5.8	6.7	4.76
FOM [GHz/mW] [3]	8.33	4.41	4.26	10.29
Active Area [mm^2]	0.45	0.18	N/A	0.037
CMOS Technology	90 nm	65 nm	65 nm	28 nm

[1]All measurements with a maximum input power = 0 dBm
[2]Lock Range=$2(f_{max}-f_{min})/(f_{max}+f_{min})$ [3]FOM=$(f_{max}-f_{min})/P_{DC}$