2.4 A 25Gb/s 5.8mW CMOS Equalizer

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The power consumption of broadband receivers becomes particularly critical in multi-lane applications such as the 100 Gigabit Ethernet. However, the power-speed trade-off tends to intensify at higher rates, making it a greater challenge to reach the generally-accepted efficiency of 1mW/Gb/s. Prominent among the power-hungry receiver building blocks are the clock-and-data-recovery circuit, the deserializer, and the front-end equalizer. The use of charge-steering techniques has shown promise for the low-power implementation of the first two functions [1]. This paper introduces a half-rate 25Gb/s equalizer employing charge steering and achieving an efficiency of 0.232mW/Gb/s.

In addition to dealing with the generic delay bounds in direct or unrolled decision-feedback equalizers (DFEs), our architecture must also accommodate the return-to-zero (RZ) format inherent in certain charge-steering topologies [1]. Shown in Fig. 2.4.1, the overall system consists of a continuous-time linear equalizer (CTLE), a 1-to-2 demultiplexer ($DMUX_1$), and two half-rate/quarter-rate (HRQR) paths. Each path includes a summer, another level of demultiplexing (by means of charge-steering latches L_1-L_2 or L_3-L_4), and one more set of latches (L_5-L_6 or L_7-L_8). Operating with complementary clocks at 6.25GHz, L_1 and L_2 alternately apply their RZ outputs to the summer in the other path, thus realizing the first tap. This summer internally multiplexes the two data streams received from L_1 and L_2 and combines the result with the incoming data. This DMUX/MUX sequence ensures that the feedback information reaching the summing junction is correct and complete even though the RZ outputs of L_1-L_2 (or L_3-L_4) are reset for half a cycle. The second tap operates in a similar manner: charge-steering latches L_5-L_6 (or L_7-L_8) sample the demultiplexed data using the Q output of the divider and apply the results to the summer.

The architecture of Fig. 2.4.1 merits three remarks. First, while demultiplexing before the DFE is attractive [2], such a DMUX must maintain some linearity so as not to irreversibly corrupt the received dispersed data. For example, the designs in [2,3] employ simple passive samplers for this purpose. Second, this architecture merges the feedback MUX with the tap differential pairs within the summers, relaxing the loop timing. Third, to achieve low power consumption while generating quadrature phases, the divide-by-two circuit is based on the topology described in [1].

Figure 2.4.2 shows the implementation of the front-end. The one-stage CTLE incorporates degeneration to create a maximum high-frequency boost of 8dB as well as inductive peaking to drive the DMUX with sufficient bandwidth. This stage also realizes offset cancellation by imbalancing the tail currents and without adding devices in the signal path.

The DMUX employs passive switching but also boosts the sampled signal level by 6dB through the use of a regenerative charge-steering pair. With a 1dB-compression point of $180mV_{pp}$, this pair exhibits enough linearity for the odd and even DFEs to equalize the dispersed signal. Note that $DMUX_1$ delivers NRZ outputs because the cross-coupled charge-steering latches merge the reset and sampling phases [1].

Figure 2.4.3 presents the implementation of one half-rate/quarter-rate path (excluding tap 2 and RZ/NRZ conversion). The summing junction is driven by the input stage (running at 12.5Gb/s) and differential pairs comprising tap 1 and tap 2 (not shown), all of which steer charge and produce a single-ended output swing of about $150mV_{pp}$. The output is applied to the charge-steering DMUX consisting of L_1 and L_2.

We note several attributes of the circuit in Fig. 2.4.3. First, the charge-steering stages, and in particular the input pair, briefly draw a packet of charge and remain off for the rest of the time, dissipating low power and allowing operation across a wide frequency range. By contrast, integrating or dynamic summers [3,4] pull a continuous current from the output nodes for half a cycle, potentially consuming high power and making it difficult to run at different rates. Second, the degeneration network in the input pair also provides some linear equalization. Third, the cross-coupled PMOS pair tied to X and Y in Fig. 2.4.3 prevents collapse of these nodes when both tap 1 and tap 2 branches draw charge. Applied to all of the stages, this technique also increases the output swing by restoring the high level to V_{DD}. Fourth, the coefficients are adjusted by varying the tail capacitances in 25 discrete steps in tap 1 (and 10 in tap 2). Fifth, the multiplexing of the feedback components is accomplished through gating the tails in Fig. 2.4.3 by the 6.25GHz clock.

To ensure sufficient hold time throughout the cascade L_1-L_8, the quadrature phases of the 6.25GHz clock alternately sample the signals. The RZ/NRZ conversion circuit incorporates clocked comparators and RS latches similar to that in [1].

The equalizer is fabricated in TSMC's 45nm digital CMOS technology. Figure 2.4.7 shows the die core, which measures $100\times100\mu m^2$. The circuit is tested with a channel having a loss of 24dB at 12.5GHz. Figure 4 shows the received and output eye diagrams. The bit-error rate (BER) in this case is below 10^{-12}. Figure 2.4.5 plots the BER as a function of the external clock phase, revealing an eye opening of approximately 0.44UI. Since the input PRBS generator has a peak-to-peak jitter of about 7ps, an opening of about 0.18UI is lost.

Figure 2.4.6 summarizes the measured performance of the equalizer and compares it with that of prior art. The circuit consumes 5.8mW, of which 2.44mW is drawn by the CTLE, 1.25mW by the divide-by-2 circuit, and 2.11mW by the two HRQR paths. We note that [6] compensates for 10dB of loss and achieves an eye opening of 0.11UI for BER = 10^{-9}.

Acknowledgments:
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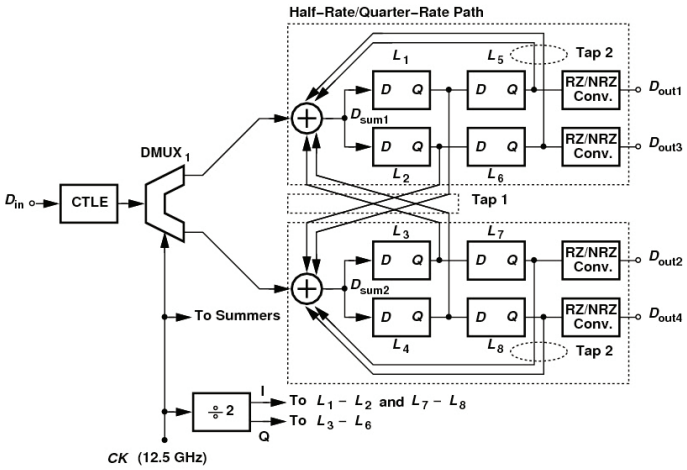

Figure 2.4.1: Equalizer architecture.

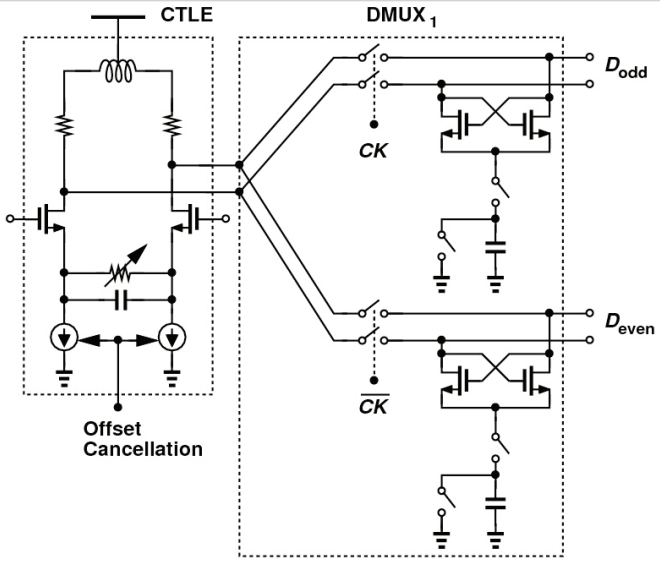

Figure 2.4.2: Implementation of front-end.

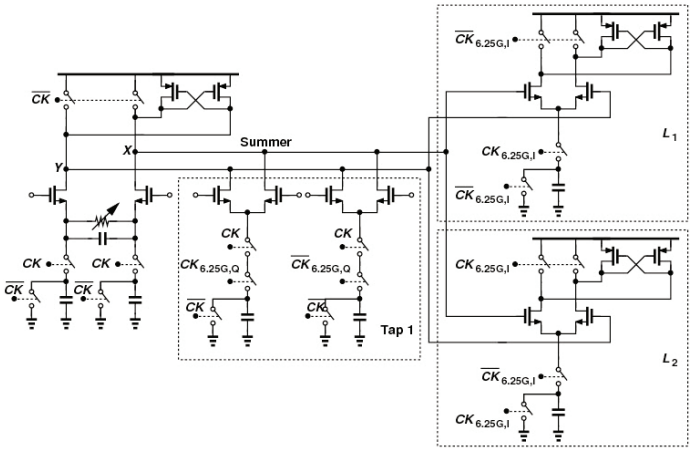

Figure 2.4.3: Implementation of one half-rate/quarter-rate path.

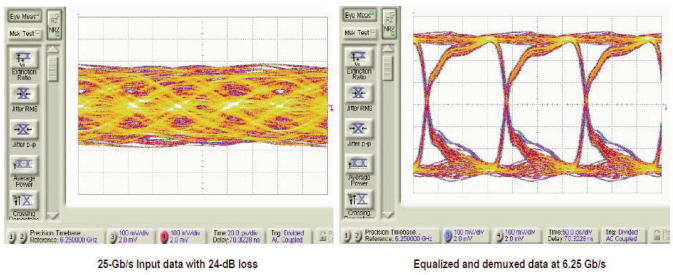

Figure 2.4.4: Measured eye diagrams of input and output data.

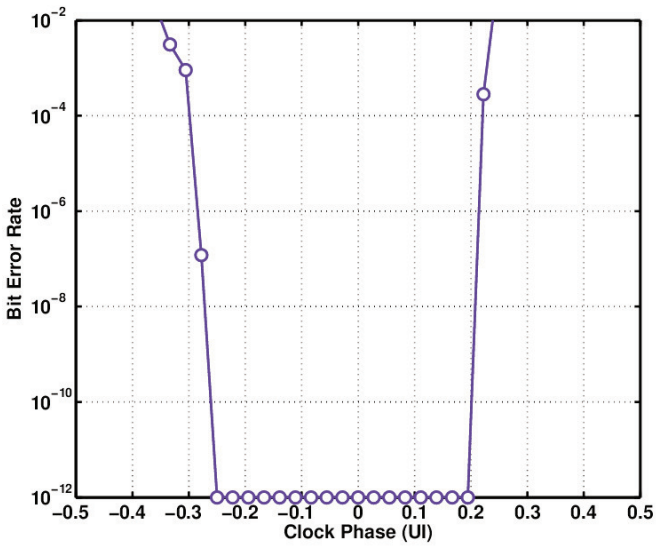

Figure 2.4.5: Measured bathtub curve at 25Gb/s with 24dB loss in channel.

Reference	[3]	[4]	[5]	[6]	[7]	This Work
Data Rate	19 Gb/s	28 Gb/s	22 Gb/s	27 Gb/s	20 Gb/s	25 Gb/s
Architecture	4-tap FFE + 5-tap DFE	CTLE + 15-tap DFE	CTLE + 2-tap DFE	1-tap DFE	CTLE + 1-tap DFE	CTLE + 2-tap DFE
DFE Clocking	Quarter Rate	Half Rate	Quarter Rate	Quarter Rate	Half Rate	Half Rate
Channel Loss @ Nyquist	25 dB	35 dB	16 dB	>10 dB	26.3 dB	24 dB
BER / horizontal eye opening	$< 10^{-9}$ / 36% UI	$< 10^{-9}$ / 35.6% UI	$< 10^{-12}$ / 26% UI	$< 10^{-9}$ / 11% UI	$< 10^{-8}$ / 26% UI	$< 10^{-12}$ / 44% UI
Supply (V)	1.1	1.05	1.15	1.1	1.2	1
Power (mW)	118	80*	20.6	11.1	13.2	5.8
Area (mm^2)	0.07	0.81**	0.016	0.015	0.012	0.01
Technology	45-nm SOI CMOS	32-nm SOI CMOS	40-nm CMOS	40-nm CMOS	45-nm SOI CMOS	45-nm CMOS

*Only for odd and even DFEs. Excludes CTLE, etc.

**Includes TX+RX+PLL/4

Figure 2.4.6: Performance summary and comparison with prior art.

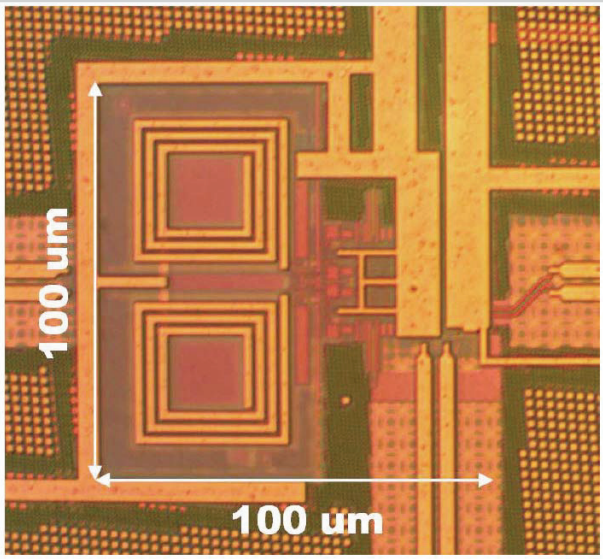

Figure 2.4.7: Equalizer die core in 45nm CMOS technology.

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