A 4-Tap 125-MHz Mixed-Signal Echo Canceller for Gigabit Ethernet on Copper Wire

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Abstract

A discrete-time analog echo canceller is described that reduces the echo in the front end of Gigabit Ethernet twisted-pair interfaces. Echo cancellation in the analog domain by means of four taps reduces the complexity of the digital echo canceller and crosstalk cancellers by 50 taps. Designed in a 0.4 μm-CMOS technology, the circuit employs an LMS algorithm to adapt to the cable length and impedance discontinuities, providing an echo suppression of 10 dB. The design operates at 125 MHz while consuming 43 mW from a 3-V supply.

I. INTROUDCTION

Gigabit Ethernet on copper cable is a fast evolving technology enabling 1 Gb/s full-duplex data communication over the existing UTP CAT-5 twisted pair cables. As depicted in Fig. 1, four pairs of twisted-pair cables and eight transceivers (four at each end) with 250 Mb/s data rate offer 1-Gb/s data communication. PAM-5 modulation reduces the baud rate to 125 MHz.

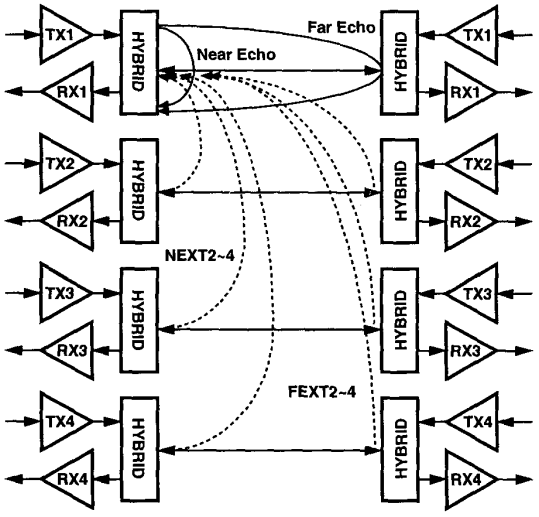

Fig. 1. Gigabit Ethernet over four twisted pairs.

In full-duplex communication, a hybrid is typically used to isolate the receiver from the transmitted signal. However, cable and connector impedance variation still results in substantial leakage of the large transmitted signal, thereby creating near-end echo. Also, impedance discontinuities along and at the end of the cable produce far-end echo. In addition, the near-end crosstalk between the four cables is significant.

The full digital solution, suggested by the IEEE 802.3ab task force[1], requires a 7-bit analog-to-digital converter (ADC) to quantize the attenuated signal as well as the echo and the crosstalk. Moreover, it employs four very long digital adaptive FIR filters, including one echo canceller and three near-end-crosstalk (NEXT) cancellers, in each transceiver.

This paper proposes a mixed-signal echo canceller to partially cancel the echo in the analog front end, relaxing the complexity in the digital domain. Using a least-mean-squared (LMS) algorithm, the circuit adapts the four taps of a discrete-time analog FIR filter at the startup, thus cancelling the four largest echo signals between two transceivers.

II. DESIGN CONSIDERATIONS

The IEEE 802.3ab allows a tolerance of ±15% in the component values and the impedance of the twisted pair. With such impedance mismatch, the hybrid can only suppress the near-end echo by 26 dB in the worst case. Furthermore, reflections from discontinuities along the cable corrupt the reception. Therefore, in order to achieve the required bit error rate (BER), additional echo cancellation is necessary.

Echo cancellers are typically implemented by digital transversal FIR filters to emulate the echo impulse response in the time domain. However, owing to the long impulse response of echo, the digital filters require a very large number of taps.

A mixed-signal adaptive filter can be realized to cancel the echo in the analog interface. Figure 2 shows a typical echo response. While the impulse response contains only a few large reflections, a long FIR filter is still required because the position of the reflections along the cable is not known.

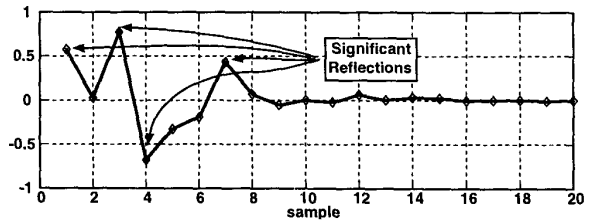

Fig. 2. Typical echo impulse response.

The echo canceller reported here incorporates a "significant echo locator" to identify the temporal location of the four

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largest reflections. The circuit then applies a signed LMS algorithm to generate an emulated echo and subtracts it from the signal+echo combination. System simulations indicate that a four-tap canceller reduces the echo by 10 to 15 dB. Since the near-end crosstalk from adjacent cables is only 16 dB below the uncorrected echo [1], additional echo cancellation in the analog domain does not improve the performance any more.

System simulations also suggest that the echo canceller reported here can reduce the complexity of the digital echo canceller and crosstalk cancellers by 50 taps. Employing a few more taps, the mixed-signal canceller can even relax the resolution of the ADC and hence the digital processing by one bit.

III. Architecture Design

Figure 4 shows the detailed architecture of the echo canceller. The transmitter consists of a 64 x 1 b FIFO register and a digital-to-analog converter (DAC), which drives the network R_1-R_3 and the transformer. The receiver employs a differential voltage-to-current converter (VIC_1), and the calibration circuit comprises a reflection locator circuit, an LMS machine, and an analog FIR filter. The voltages at nodes X and Y are scaled replicas of the transmitted signal and the transmitted+received signal, respectively. Thus, in the absence of impedance variations and discontinuities, the output of VIC_1 contains only the received signal.

The operation of the system is as follows. At the startup, the transmitter applies a unit step (rather than an impulse) to the hybrid and the cable, generating the uncorrected echo at the output of VIC_1. The reflection locator circuit then differentiates the result by means of a switched-capacitor circuit, obtaining the impulse response. If the response exhibits an amplitude greater than V_{REF}, the addr ess of the corresponding tap in the FIFO register is stored for actual operation. This test is repeated 64 times, identifying four significant taps.

Next, the analog FIR filter is adapted so as to emulate the echo. Driven by the four significant taps, the filter produces a current output that is subtracted from the output of VIC_1 and compared to zero. Based on the result, the LMS machine updates the multiplier coefficients m_1-m_4 in the FIR filter, forcing the echo residue to small values. Each multiplier is in fact realized as a DAC whose reference is modulated by the data bits provided by the selection logic. (The analog signal path is fully differential in both transmit and receive paths.) The LMS machine incorporates up/down counters to store the coefficients of the analog multiplier. The counters count up or down according to the product of the error sign *sgn(err)* and data sign *sgn(data)*.

The performance of the architecture was first analyzed by a behavioral model written in C language, including the characteristics of the cable and the sources of echo and crosstalk. Three critical parameters were determined by this analysis: (1) the minimum number of taps in the analog FIR filter, (2) the minimum required accuracy of the coefficients, (3) the maximum tolerable integral nonlinearity (INL) of the DACs. For approximately 10 dB echo suppression, four taps, a coefficient resolution of 10 bits, and a DAC nonlinearity of 0.8% are necessary. Figure 4 plots the amount of echo suppression versus the resolution of the multiplier coefficients, suggesting marginal improvement for resolutions greater than 10 bits.

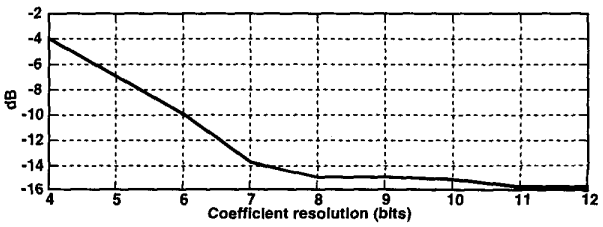

Fig. 4. Echo reduction vs. coefficient resolution.

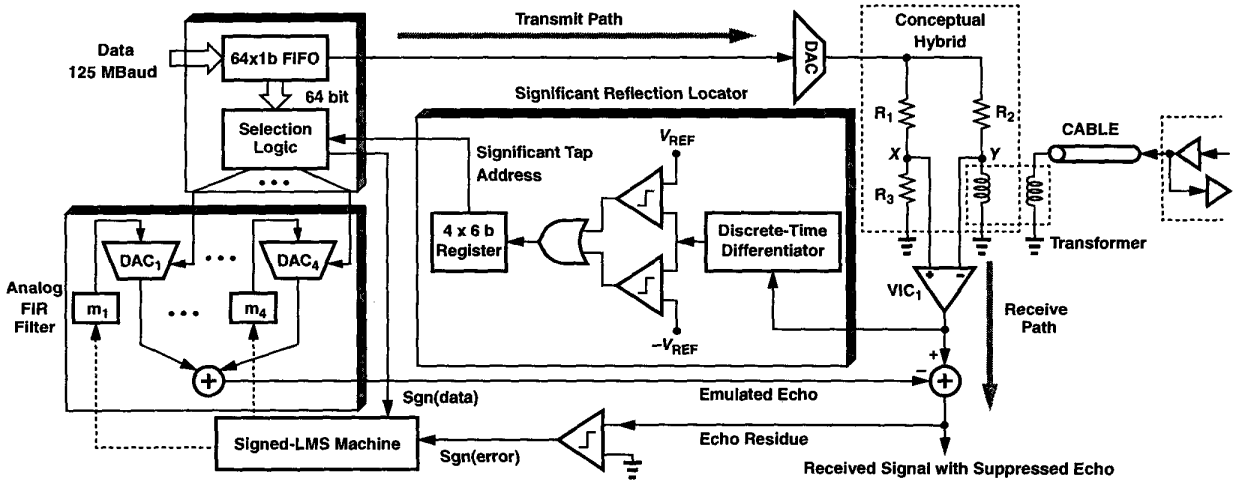

Fig. 3. Echo canceller architecture.

IV. Building Blocks

A. Differentiator

The discrete-time differentiator used in the reflection locator of Fig. 3 must sample the data at 125 Mb/s and subtract it from the previous data. Figure 5 depicts a compact high-speed realization of this function that requires only two phases. In the sampling phase [Fig. 5 (a)], A_1 and A_2 are reset while storing V_{in} on their input capacitors. At the same time, the discharged capacitor C_s samples the previous data stored on C_d (while dividing the amplitude by a factor of two). In the evaluation phase [Fig. 5 (b)], A_1 holds the sampled data, charging C_d while A_2 subtracts the sampled data from the value stored on C_s. Note that the virtual ground at the input of A_2 forces the voltage across C_s to zero, thereby preparing it for charge sharing with C_d in the next phase.

The charge sharing between C_s and C_d in the sampling mode is susceptible to the junction capacitance nonlinearity of MOS switches, but differential operation and proper sizing of transistors minimizes this effect. Each op amp is implemented by a folded-cascode topology. Note that the differentiator is turned off after the significant reflections are identified, saving power dissipation.

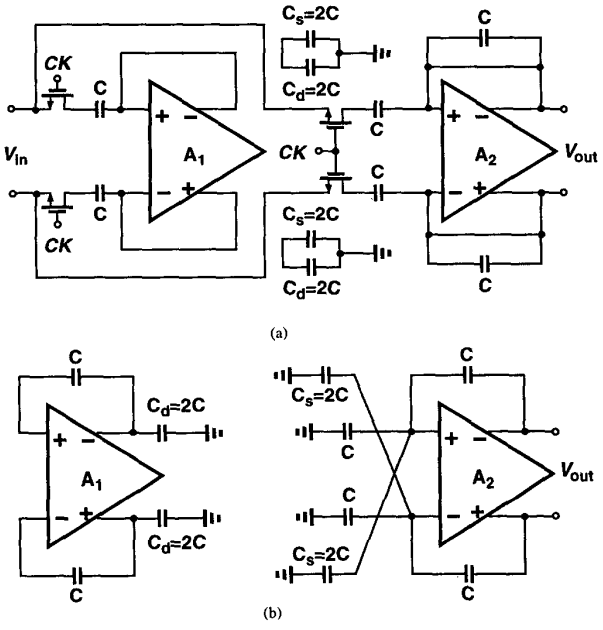

Fig. 5. Two-phase differentiator, (a) sampling mode (b) evaluation-mode.

B. Analog Multiplier

System simulations indicate that the multiplier coefficients in the mixed-signal FIR filter must have a resolution of 10 bits so as to maintain the LMS loop stability and achieve acceptable echo suppression. It is also ascertained that the *nonlinearity* in the coefficients need not be less than 0.8% (approximately 7 bits). Thus, the DACs performing the multiplication must provide 1024 monotonic steps with moderate INL. Since the FIR filter incorporates four such DACs, their complexity and power dissipation must be minimized while allowing operation at 125 MHz.

Figure 6 illustrates the DAC architecture, consisting of a coarse section driven by the five MSBs and a fine section driven by the five LSBs. Each section selects a tap voltage produced by a resistor ladder and converts the voltage to a current. The actual implementation is fully differential. Note that the output must be in the current domain to allow addition to the output of other DACs and eventually the output of VIC_1 in Fig. 3.

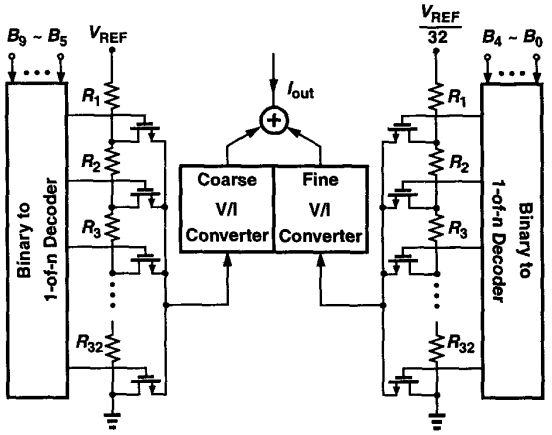

Fig. 6. 10-bit DAC with 7-bit linearity.

The role of each DAC in Fig. 7 is to multiply the one-bit signal generated by the selection logic by the 10-bit coefficients m_j. This operation is performed in the DAC by swapping the outputs of each differential ladder according to the one-bit signal. Figure 8 illustrates the actual implementation with differential ladders.

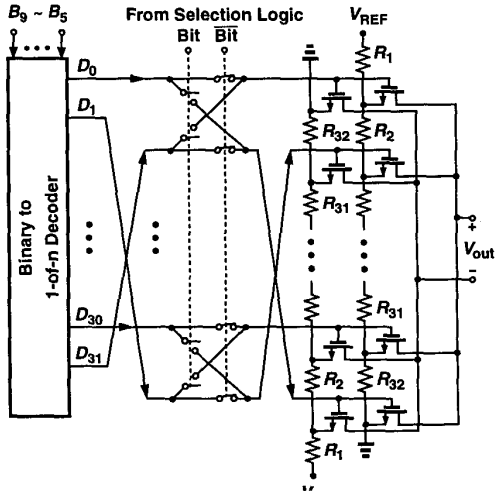

Fig. 7. The actual switching of the differential tap voltages.

C. V/I and I/V Converters

The V/I converters in Fig. 6 must exhibit sufficient linearity with input differential swings of about 2 V. Due to the lack

of high-quality resistors in the CMOS technology used here, simple resistive degeneration is not feasible. Thus, as depicted in Fig. 8, the topology proposed in [2] is utilized. The choice $W_I/W_S=7$ guarantees sufficient linearity for the LMS algorithm.

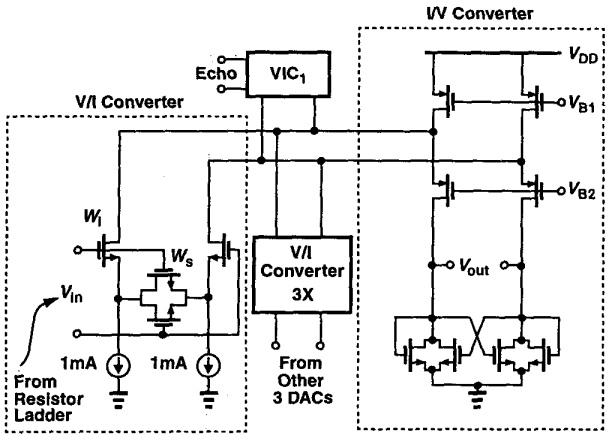

Fig. 8. The V/I and I/V converter.

The currents produced by the four DACs and VIC_1 in Fig. 3 must be added and converted to voltage. As shown in Fig. 8, the addition is performed at the sources of a differential common-gate stage to minimize the resulting time constant. The I/V conversion is then carried out by means of diode-connected devices with a small amount of positive feedback. Interestingly, this type of load partially cancels the nonlinearity of the V/I converter, thus yielding a higher linearity.

V. Experimental Results

The echo canceller has been fabricated in a 0.4-μm digital CMOS technology and tested with a 3-V supply. Figure 9 is a photograph of the die, which occupies an area of 1mm x 1mm.

The prototype contains both the transmit and the receive paths. Random data is fed to the transmitter, which drives a transformer and a CAT-5 cable. Impedance mismatches are introduced by setting different terminated resistors in both the near and the far end, thereby creating various echo levels.

Figure 10 shows the measured echo in the time domain before and after cancellation. The total echo power is reduced by approximately 10 dB. The LMS algorithm converges roughly in 10 μs.

Clock/Data Rate	125 MHz
Echo Suppression	10 dB
Power Dissipation	43 mW
Power Supply	3 V
Convergence Time	10 μs
Input Swing	2 V_{pp}
Active Area	1mm x 1mm
Technology	0.4-μm CMOS

Table 1: Measured performance of echo canceller at 125 MHz

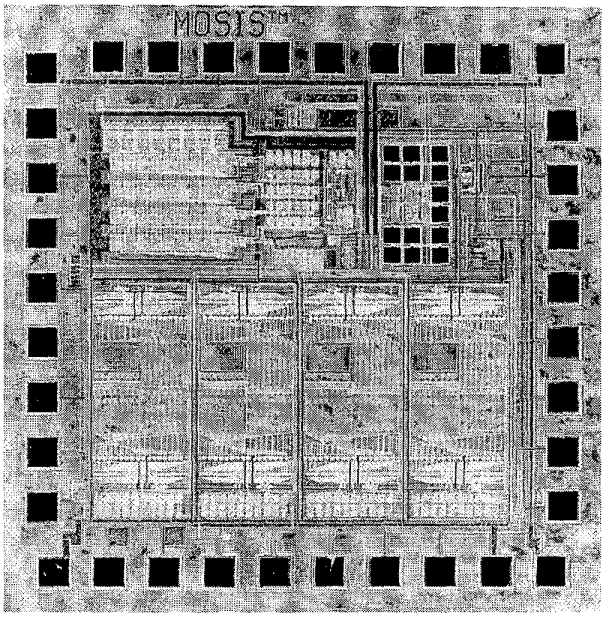

Fig. 9. Die photo of mixed-signal echo canceller.

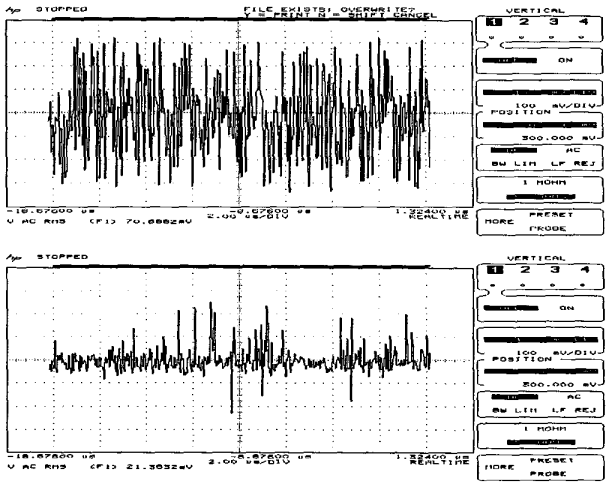

Fig. 10. Measured echo in time domain before (top) and after (bottom) cancellation.

References

[1] IEEE 802.3ab, A Tutorial presentation for 1000 BASE-T. URL: http://grouper.ieee.org/groups/802/3/ab/public/march98/index.html

[2] F. Krummenacher, N Joehl, "A 4-MHZ CMOS Continuous-Time Filter with On-chip Automatic Tuning," *IEEE Journal of Solid-State Circuits*, vol. 23, pp. 750-758, June 1988