A Stabilization Technique for Phase-Locked Frequency Synthesizers

Tai-Cheng Lee and Behzad Razavi
Electrical Engineering Department
University of California, Los Angeles

Abstract

A stabilization technique is presented that relaxes the trade-off between the settling speed and the magnitude of output sidebands in phase-locked frequency synthesizers. The method introduces a zero in the open-loop transfer function through the use of a discrete-time delay cell, obviating the need for resistors in the loop filter. A 2.4-GHz CMOS frequency synthesizer employing the technique settles in approximately 60 μs with 1-MHz channel spacing while exhibiting a sideband magnitude of −58.7 dBc. Designed for Bluetooth applications and fabricated in a 0.25-μm digital CMOS technology, the synthesizer achieves a phase noise of −112 dBc/Hz at 1-MHz offset and consumes 20 mW from a 2.5-V supply.

I. Introduction

Phase-locked loops (PLLs) typically suffer from a trade-off between the settling time and the ripple on the control voltage, limiting the performance that can be achieved in terms of channel switching speed and output sideband magnitude in RF synthesizers. This paper describes a loop stabilization technique that yields a small ripple while achieving fast settling. Using a discrete-time delay cell, the PLL architecture creates a zero in the open-loop transfer function. Another important advantage of the technique is that it uses no resistors in the loop filter, lending itself to digital CMOS technologies.

The next section of the paper develops the foundation for the proposed technique. Section III describes the synthesizer architecture and the design of its building blocks and Section IV proposes fast simulation techniques for the synthesizer. Section V summarizes the experimental results.

II. Stabilization Technique

Consider the PLL shown in Fig. 1, where a voltage-controlled oscillator (VCO) is driven by a charge pump (CP) and a phase-frequency detector (PFD). Resistor R_1 provides the stabilizing zero and capacitor C_2 suppresses the glitch generated by the charge pump on every phase comparison instant. The glitch arises from mismatches between the width of Up and Down pulses produced by the PFD as well as charge injection and clock feedthrough mismatches between PMOS and NMOS devices in the charge pump.

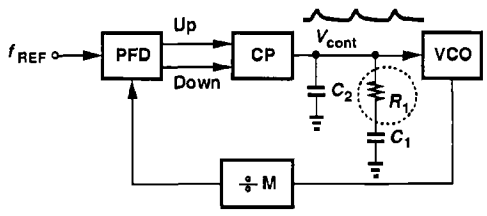

Fig. 1. Conventional PLL architecture.

The principal drawback of this architecture is that C_1 determines the settling whereas C_2 controls the ripple on the control voltage. Since C_2 must remain below C_1 by roughly a factor of 10 so as to avoid underdamped settling, the loop must be slowed down by a large C_1 if C_2 is to yield a sufficiently small ripple. It is therefore desirable to seek methods of creating the stabilizing zero without the resistor so that the capacitor that defines the switching speed also directly suppresses the ripple.

It is important to note that the problem of ripple becomes increasingly more serious as the supply voltage is scaled down and/or the operating frequency goes up. The relative magnitude of the primary sidebands at the output of the VCO is given by $A_m K_{VCO}/(2\omega_{REF})$ where A_m is the peak amplitude of the first harmonic of the ripple, K_{VCO} is the gain of the VCO, and ω_{REF} is the synthesizer reference frequency. [For a given relative tuning range (e.g. $\pm 10\%$), the gain of LC VCOs must increase if the supply voltage goes down.] If $K_{VCO} = 100$ MHz/V and $f_{REF} = 1$ MHz, then the fundamental ripple amplitude must be less than 63 μV to guarantee sidebands 60 dB below the carrier.

In order to arrive at the stabilization technique, consider the PLL architecture shown in Fig. 2. Here, the primary charge pump, CP_1, drives a single capacitor C_1 while a secondary charge pump, CP_2, injects charge after some delay ΔT. The total current flowing through C_1 is thus equal to

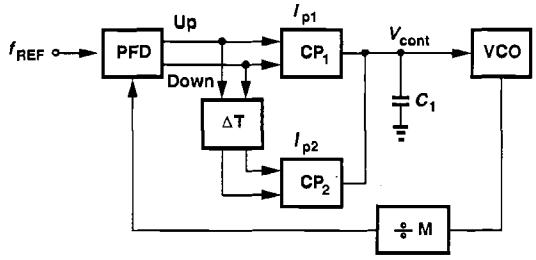

Fig. 2. Proposed PLL architecture with delayed charge pump circuit.

$$I_p = I_{p1} + I_{p2} e^{-s\Delta T} \quad (1)$$

$$\approx I_{p1} + I_{p2}(1 - s\Delta T), \quad (2)$$

where ΔT is assumed to be much smaller than the loop time constant. Consequently, the transfer function of the PFD/CP/LPF combination can be expressed as

$$\frac{V_{cont}}{\Delta\phi}(s) = \frac{I_{p1} + I_{p2}}{2\pi C_1 s} - \frac{I_{p2}}{2\pi C_1}\Delta T. \quad (3)$$

Assuming $I_{p2} = -\alpha I_{p1}$, we have

$$\frac{V_{cont}}{\Delta\phi}(s) = \frac{I_{p1}}{2\pi}\left(\frac{1-\alpha}{C_1 s} + \frac{\alpha\Delta T}{C_1}\right), \quad (4)$$

obtaining a zero at

$$\omega_z = \frac{1-\alpha}{\alpha}\frac{1}{\Delta T}. \quad (5)$$

In order to achieve a sufficiently low zero frequency, ΔT must be large or α close to unity. Since the accuracy in the definition of α is limited by mismatches between the two charge pumps, ΔT must still be a large value. For example, if $f_{REF} =$ 1 MHz, and $\alpha = 0.9$, then a ΔT of approximately 200 ns is required to ensure a well-behaved loop response.

The architecture of Fig. 2 suffers from a critical drawback: it requires a very long delay before CP_2 while the Up and Down pulses generated by the PFD can assume a very narrow width during lock. If the bandwidth of each stage in the delay line is reduced so as to produce a large delay, then the narrow Up and Down pulses are heavily attenuated, thus giving rise to a dead zone. Conversely, if the bandwidth of each stage is wide enough to support such pulses, then a very large number of stages is required to obtain the necessary ΔT.

To resolve the above difficulty, the architecture is modified as shown in Fig. 3(a), where a discrete-time analog delay line is placed after CP_2 and C_2. The delay network is realized as depicted in Fig. 3(b), consisting of two interleaved master-slave sample-and-hold branches operating at half of the reference frequency. The circuit emulates ΔT as follows. When CK_{even} is high, C_{s1} shares a charge packet corresponding to the previous phase comparison with C_1 while C_{s2} samples a level proportional to the present phase difference. In the next period, C_{s1} and C_{s2} exchange roles. The interleaved sampling network therefore provides a delay equal to the reference period, $1/f_{REF}$.

The discrete-time delay technique of Fig. 3 allows a precise definition of the zero frequency without the use of resistors. To quantify the behavior of a PLL incorporating this method, we assume the loop settling time is much greater than $1/f_{REF}$ so that the delay network can be represented by the continuous-time model shown in Fig. 4. Here, $R_{eq} = (f_{REF}C_s)^{-1}$ approximates the interleaved branches. Equation (4) can then be rewritten as

$$\frac{V_{cont}}{\Delta\phi}(s) = \frac{I_{p1}}{2\pi}\left(\frac{1}{f_{REF}C_s} + \frac{I_{p1}+I_{p2}}{I_{p1}}\frac{1}{sC_2}\right), \quad (6)$$

where it is assumed $C_2 \gg C_1$ and the current through C_1 is neglected. This equation exhibits two interesting properties. First, if $I_{p2} = -\alpha I_{p1}$, then $(I_{p1} + I_{p2})/I_{p1} = 1 - \alpha$ and

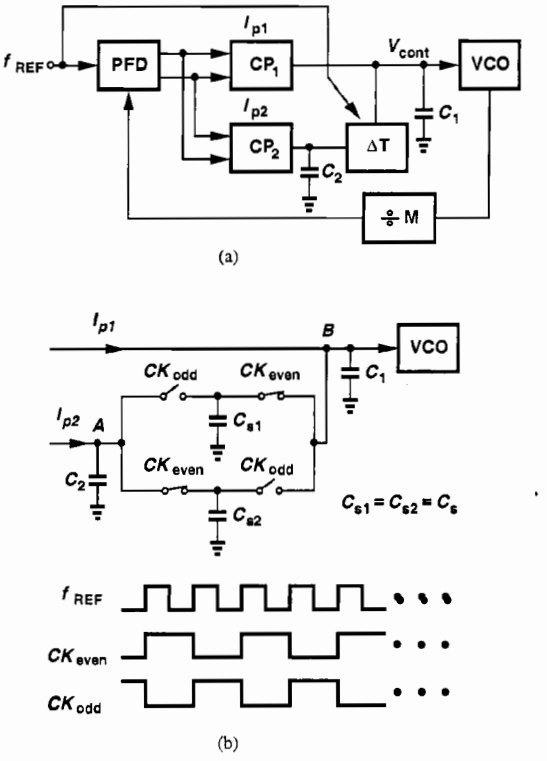

Fig. 3. Actual implementation of PLL with delay sampling circuit.

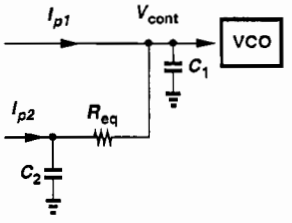

Fig. 4. Continuous-time approximation of delay network.

the value of C_2 is "amplified" by $(1-\alpha)^{-1}$. For example, if $\alpha = 0.9$, then C_2 is multiplied by a factor of 10, saving substantial area. Second, the zero frequency is equal to

$$\omega_Z = \left(1 + \frac{I_{p2}}{I_{p1}}\right)\frac{C_s}{C_2}f_{REF}, \quad (7)$$

a value independent of process and temperature. Assuming $C_2 = C_s$ and $I_{p1} = -\alpha I_{p2} = I_p$, we obtain the damping factor and the settling time constant of the loop as:

$$\zeta = \frac{1}{2(1-\alpha)f_{REF}}\sqrt{\frac{I_p}{2\pi C_2}\frac{K_{VCO}}{M}} \quad (8)$$

$$(\zeta\omega_n)^{-1} = \frac{4\pi f_{REF}C_2}{I_p}\frac{M}{K_{VCO}}. \quad (9)$$

The key observation here is that the factor $(1-\alpha)^{-1}$ appears in ζ but not in $(\zeta\omega_n)^{-1}$. Thus, the two parameters can be

optimized relatively independently. Furthermore, the damping factor exhibits much less process and temperature dependence than in the conventional loop of Fig. 1. Note that for $I_{p2} = 0$, the proposed circuit resembles the topology of Fig. 1 but with the resistor replaced with a switched-capacitor network.

For RF synthesis, the delay network of Fig. 2 must be designed carefully so as to minimize ripple on the control voltage. Since in the locked condition, the voltages at nodes A and B are nearly equal, the charge sharing between C_{s1} or C_{s2} and C_1 creates only a small ripple. Furthermore, the switches in the delay stage are realized as small, complementary devices to introduce negligible charge injection and clock feedthrough.

III. Synthesizer Design

A 2.4-GHz CMOS synthesizer targeting Bluetooth applications has been designed using the stabilization technique described above. This section presents the architecture and building blocks of the synthesizer.

Shown in Fig. 5, the synthesizer uses an integer-N architecture with a feedback divider whose modulus is given by $M = NP + S + 1$, where $N = 4$, $P = 600$, and $S =$

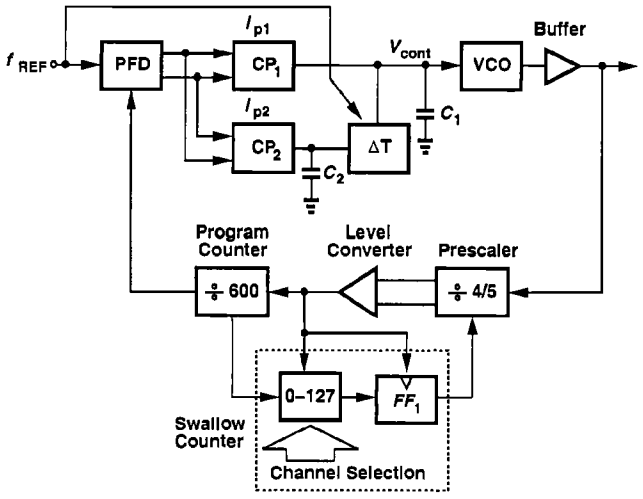

Fig. 5. Synthesizer architecture.

0-127. With $f_{REF} = 1$ MHz, the output frequency covers the 2.4-GHz ISM band. The output of the swallow counter is pipelined by the flipflop FF_1 to allow a relaxed design for the level converter and the swallow counter [1]. The buffer following the VCO suppresses the kickback noise of the prescaler when the modulus changes. It also avoids limiting the tuning range of the VCO by the input capacitance of the prescaler.

The VCO topology is shown in Fig. 6(a). To provide both negative and positive voltages across the MOS varactors, the sources of M_1 and M_2 are grounded and the circuit is biased on top by I_{DD}. The inductors are realized as shown in Fig. 6(b), with the bottom spiral moved down to metal 2 so as to reduce the parasitic capacitance [2].

The prescaler must divide the 2.4-GHz signal while consuming a small power dissipation. Depicted in Fig. 7, the

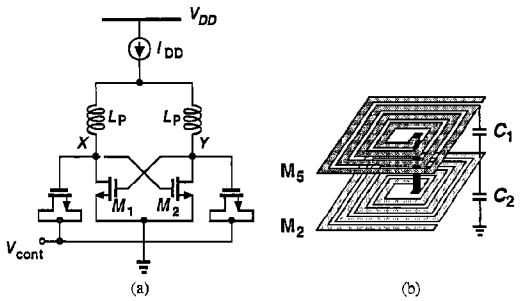

Fig. 6. (a) LC oscillator, (b) two-layer stacked inductor.

circuit employs three current-steering flipflops with diode-

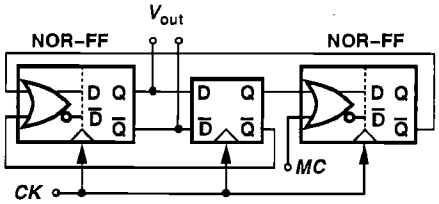

Fig. 7. Prescaler.

connected loads. The use of NOR gates obviates the need for power- and headroom-hungry level shift circuits required in NAND implementations.

IV. Simulation Techniques

A 2.4-GHz synthesizer with a reference frequency of 1 MHz requires a transient simulation step of approximately 20 ps for a total settling time on the order of 100 μs. The simulation therefore requires an extremely long time owing to both the vastly different time scales and the large number of devices (especially in the divider).

In order to study the loop dynamics with realistic transistor-level PFD, CP and VCO design, two speed-up techniques have been employed. First, the reference frequency is scaled up by a factor of 100 and the loop filter capacitor and the divide ratio are scaled down by the same factor. Since the PFD operates reliably at 100 MHz with no dead zone, this method directly reduces the simulation time by a factor of 100. From Eqs. (8) and (9), we note that scaling C_2 and M by 100 maintains a constant damping factor while scaling the settling time by 100.

Second, the divider is realized as a simple behavioral model in HSPICE that uses a handful of ideal devices and its complexity is independent of the divide ratio. Illustrated in Fig. 8, the principle of the behavioral divider is to pump a well-defined charge packet into an integrator in every period and reset the integrator when its output exceeds a certain level, V_{REF}. Using an ideal op amp, comparator, and switches with proper choice of V_b and V_{REF}, the circuit can achieve arbitrarily long high divide ratios. This techniques yields another factor of 20 improvement in the simulation speed, allowing the synthesizer to be simulated in less than 3 minutes on an Ultra 10 Sun workstation.

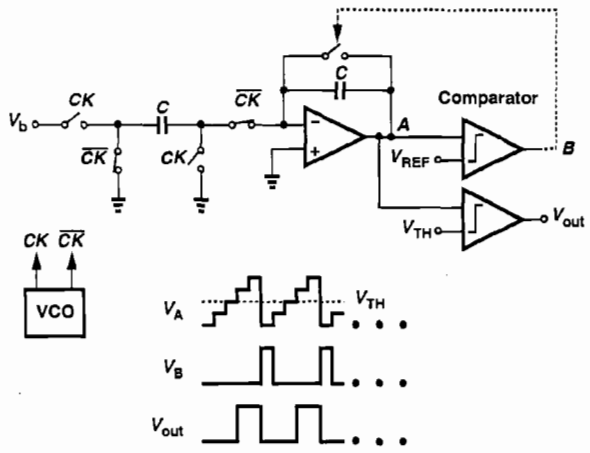

Fig. 8. Divider behavioral model.

V. Experimental Results

The frequency synthesizer has been fabricated in a digital 0.25-μm CMOS technology. Shown in Fig. 9 is a photograph of the die, whose active area measures 0.65 mm × 0.45 mm.

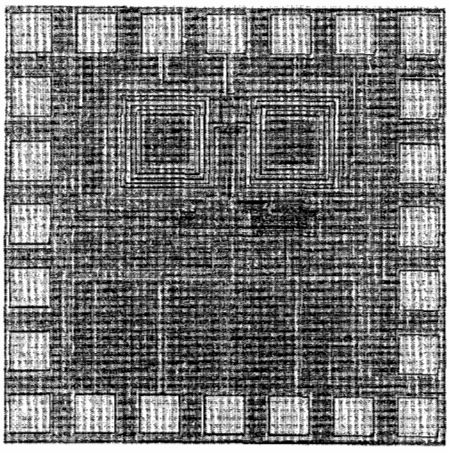

Fig. 9. Die photo.

The circuit has been tested in a chip-on-board assembly while running from a 2.5-V power supply.

Figure 10 shows the output spectrum in the locked condition. The phase noise is equal to −112 dBc/Hz at 1 MHz offset, well exceeding the Bluetooth requirement. The primary reference sidebands are at approximately −58.7 dBc. This level is lower than that achieved in [3] with differential VCO control and an 86.4-MHz reference frequency.

Figure 11 plots the measured settling behavior of the synthesizer when its channel number is switched by 64. The settling time is about 60 μs, i.e., 60 input cycles.

References

[1] C. Lam and B. Razavi, "A 2.6-GHz/5.2-GHz Frequency Synthesizer in 0.4-μm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 35, pp. 788-794, May 2000.

[2] A. Zolfaghari, A. Chan, and B. Razavi, "Stacked Inductors and 1-to-2 Transformers in CMOS Technology," *Proc. of CICC*, pp. 345-348, May 2000.

[3] L. Lin, L. Tee, and P. R. Gray, "A 1.4-GHz Differential Low-Noise CMOS Frequency Synthesizer using a Wideband PLL Architecture," *ISSCC Dig. Tech. Paper*, pp. 204-205, Feb. 2000.

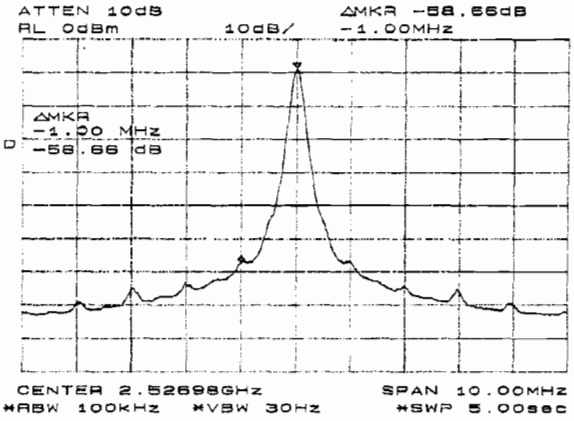

Fig. 10. Measured spectrum at the output of VCO.

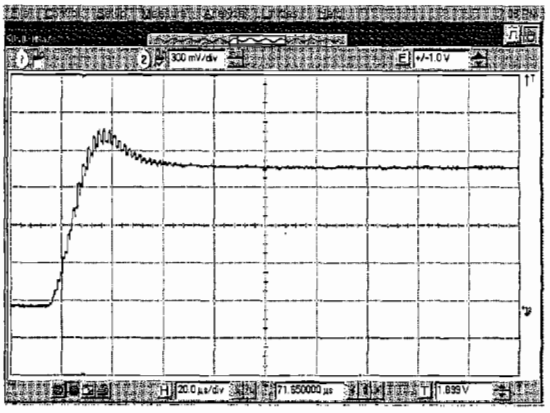

Fig. 11. Control voltage during loop settling.

Center Frequency	**2.4 GHz**
Channel Spacing	**1 MHz**
No. of Channels	**128**
Phase Noise at 1 MHz Offset	**-112 dBc/Hz**
Reference Sidebands	**-58.7 dBc**
Settling Time	**60 μs**
Power Dissipation	
VCO	**10 mW**
VCO Buffer	**3 mW**
Divider	**6 mW**
Charge Pump	**0.5 mW**
Others	**0.5 mW**
Total	**20 mW**
Supply Voltage	**2.5 V**
Die Area	**0.65 mm x 0.45 mm**
Technology	**0.25-μm CMOS**

Table 1. Performance summary.