A 40-GHz Frequency Divider in 0.18-μm CMOS Technology

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Abstract

A frequency divider employs resonance techniques by means of on-chip spiral inductors to operate at high speeds. Configured as two cascaded $\div 2$ stages, the circuit achieves a frequency range of 2.3 GHz at 40 GHz while consuming 31 mW from a 2.5-V supply.

I. Introduction

Broadband data transmitters typically incorporate a flipflop running at full rate to retime the multiplexed data, thereby removing the jitter due to mismatches in the multiplexer. The clock driving this flipflop is generated by a phase-locked loop, which in turn requires a full-rate frequency divider.

This paper describes a divider circuit based on the Miller topology [1] but using double resonant networks to achieve a high speed. Configured as two cascaded $\div 2$ stages, the circuit operates at an input frequency of 40 GHz while consuming 31 mW from a 2.5-V supply.

The next section of the paper develops the foundation for the proposed divider. Section III describes the circuit details, and Section IV summarizes the experimental results.

II. Divider with Bandpass Load

In order to both minimize the required voltage headroom and maximize the speed, it is desirable to employ an LC tank as the load in the Miller divider (Fig. 1). The Q of the tank leads to a trade-off between the loop gain (i.e., the maximum speed) and the frequency range across which the circuit divides correctly.

The necessary condition for proper division is that the loop gain at $\omega_{in}/2$ be at least unity. Modeling the multiplier by a proportionality factor β (i.e., $w = \beta xy$) and assuming the following transfer function for the RLC tank:

$$H(s) = \frac{2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \tag{1}$$

we have

$$\frac{\beta A}{2}\left|H(j\frac{\omega_{in}}{2})\right| = 1. \tag{2}$$

(The factor 1/2 arises from the product-to-sum conversion of sinusoids after multiplication.) That is,

$$\frac{\beta A}{2}\left|\frac{2\zeta\omega_n\omega}{\sqrt{(\omega_n^2-\omega^2)^2+4\zeta^2\omega_n^2\omega^2}}\right| = 1. \tag{3}$$

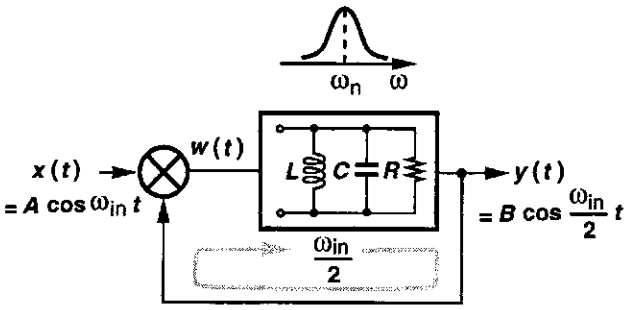

Fig. 1. Miller divider with bandpass filter.

Thus, the minimum input amplitude necessary for correct division is given by

$$A \geq \frac{2}{\beta}\sqrt{1+\frac{(1-\frac{\omega_{in}^2}{4\omega_n^2})^2}{\zeta^2\frac{\omega_{in}^2}{\omega_n^2}}}. \tag{4}$$

As expected, the right-hand side falls to a minimum of $2/\beta$ for $\omega_{in} = 2\omega_n = 2/\sqrt{LC}$. For $\Delta\omega = |\omega_{in} - 2\omega_n| \ll 2\omega_n$, we have

$$1 - \frac{\omega_{in}^2}{4\omega_n^2} = \frac{(2\omega_n+\omega_{in})(2\omega_n-\omega_{in})}{4\omega_n^2} \tag{5}$$

$$\approx \frac{4\omega_n(2\omega_n-\omega_{in})}{4\omega_n^2} \tag{6}$$

$$\approx \frac{\Delta\omega}{\omega_n}. \tag{7}$$

Consequently, since $\zeta = (2Q)^{-1}$, the fraction under the square root in Eq. (4) can be reduced to $(Q\Delta\omega/\omega_n)^2$, yielding

$$A \geq \frac{2}{\beta}\sqrt{1+(\frac{Q\Delta\omega}{\omega_n})^2}. \tag{8}$$

Figure 2 plots the required input amplitude as a function of ω_{in}. For example, if we restrict the maximum input amplitude to $4/\beta$, then

$$\Delta\omega = \frac{\sqrt{3}}{Q}\omega_n. \tag{9}$$

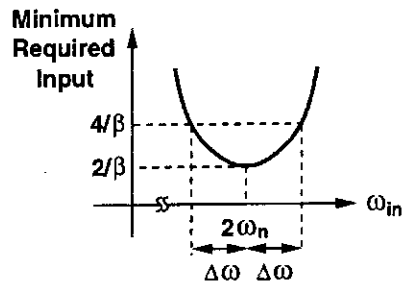

Fig. 2. Minimum input amplitude for correct division versus input frequency.

III. Circuit Implementation

Differential implementations of the Miller divider can assume either of the two topologies depicted in Fig. 3, where the two ports of the mixer are distinguished from each other. This distinction leads to interesting points regarding the operation of each topology.

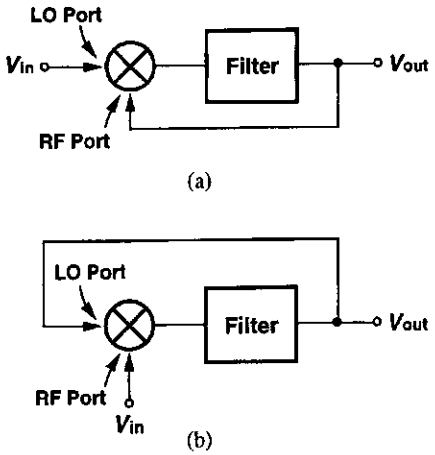

Fig. 3. Miller divider realized as (a) RF-port feedback, (b) LO-port feedback.

A. First Divider Stage

Figure 4(a) shows the first $\div 2$ stage, configured according to the topology of Fig. 3(a). Here, the load inductors $L_1 = L_2 = 0.85$ nH resonate with the parasitic capacitances as nodes X and Y and the input capacitance of M_1 and M_2, thus providing a significant impedance at 20 GHz with negligible voltage headroom consumption.

The device dimensions and component values in this circuit must be chosen so as to provide both sufficient loop gain - to guarantee correct division - and large enough output swings necessary for the subsequent stage. Assuming abrupt, complete switching of M_3-M_6, neglecting the effect of L_3 and parasitic capacitances, and simplifying the circuit to that shown in Fig. 4(b), we express the voltage conversion gain of the mixer (= loop gain) as

$$A_v = \frac{2}{\pi} g_{m1,2} R_p, \tag{10}$$

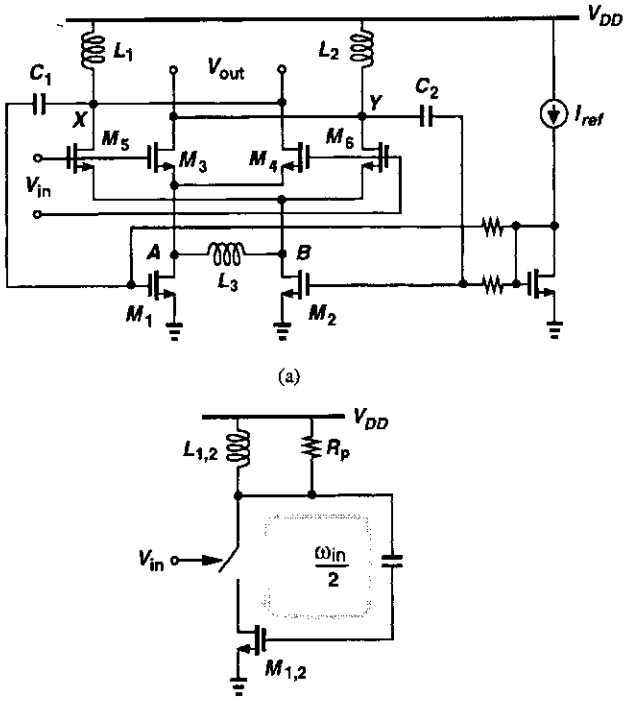

Fig. 4. (a) First $\div 2$ stage, (b) simplification of (a).

where $R_p = QL_{1,2}\omega$ denotes the equivalent parallel resistance of each tank. Since $g_m \approx 2\pi f_T C_{GS}$,

$$\frac{2}{\pi} 2\pi f_T C_{GS} Q L_{1,2} \omega = 1. \tag{11}$$

With all of the parasitics neglected, $\omega \approx 1/\sqrt{C_{GS}L_{1,2}}$ and hence

$$Q = \frac{\pi}{2}\frac{f}{f_T}, \tag{12}$$

where f is the output frequency. This result implies that, if $f \approx f_T/2$, a tank Q near unity suffices. However, the following effects necessitate a much higher Q: (1) The total capacitance at nodes A and B; even if the source/drain junction capacitances are neglected, M_3-M_6 create a pole around f_T at these nodes, "wasting" about half of the small-signal drain currents of M_1 and M_2. (2) The gradual switching of M_3-M_6 with a nearly sinusoidal drive converts a fraction of the differential currents produced by M_1 and M_2 to a common-mode component. (3) The parasitic capacitances of the load inductors and the coupling capacitors lead to $\omega_n < 1/\sqrt{C_{GS}L_{1,2}}$. Simulations reveal that the Q must exceed 4.5 for correct division.

Since all of the six transistors in this circuit are relatively wide $[(W/L)_{1,2} = 16/0.18, (W/L)_{3\sim6} = 10/0.18]$, the total capacitance at the drains of M_1 and M_2 shunts a considerable portion of their small-signal drain current to ground. Inductor L_3 is therefore added to resonate with this capacitance. Realized as a symmetric structure, $L_3 = 1.6$nH exhibits a higher Q with differential signals [2] (estimated to be around 10 at

20 GHz), introducing a resistance of 2 kΩ between A and B. This impedance is much greater than that seen looking into the sources of M_3-M_6, thereby wasting little current.

Figure 5 plots the operation behavior of three CMOS Miller dividers using (a) resistive loads, (b) inductively-peaked resistive loads[1], and (c) inductive loads. Obtained through transistor-level simulations, the plots demonstrate the speed advantage of inductive loads, albeit at the cost of a narrower fractional frequency range. It is worth noting that high-speed CMOS Miller dividers using purely resistive loads are prone to failure due to insufficient phase shift around the loop. This issue is rarely encountered in bipolar implementations because most employ emitter followers in the feedback path, thereby providing the requisite delay.

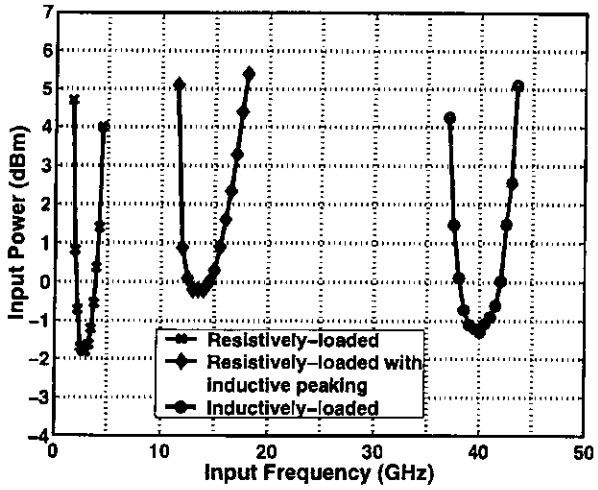

Fig. 5. Simulated operation behavior of three Miller dividers.

The conceptual representation in Fig. 3(a) bears some resemblance to an injection-locked oscillator, except that the input modulates the loop "violently," prohibiting oscillation for $V_{in} = 0$ (because the double-balanced mixer produces a zero output). Thus, the loop is insensitive to injection pulling by other sources.

B. *Second Divider Stage*

Depicted in Fig. 6(a), the second ÷2 stage is based on the topology of Fig. 3(b). In this case, the output is returned to the switching quad rather than to the bottom pair so as to present less capacitance to the first divider. This circuit in fact operates as an injection-locked oscillator [Fig. 6(b)]: M_3 and M_4 form a cross-coupled pair, and M_5 and M_6 appear as diode-connected transistors lowering the Q of the tank and hence increasing the lock range. Inductor L_3 resonates with the capacitances at nodes A and B, widening the lock range to some extent [4]. In contrast to injection-locked dividers with a single-ended input [4, 5], this topology injects the differential phases of the 20-GHz signal into the tail nodes and the output nodes. Simulations indicate that differential injection in this manner increases the lock range by 20%.

[1] Similar to that in [3].

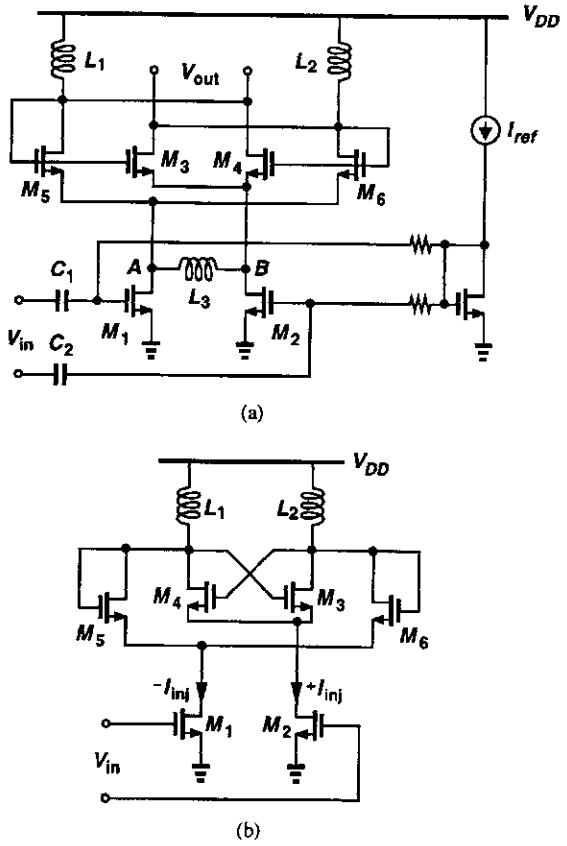

Fig. 6. (a) Second ÷2 stage, (b) redrawn to show injection locking.

The bottom-plate parasitic capacitance of C_1 and C_2 in Figs. 4(a) and 6(a) lowers the loop gain of the first stage. These capacitors are therefore realized as "fringe" structures [6] to obtain both small parasitics and high density.

Since the operation frequency range of the overall ÷4 circuit is given by the intersection of those of the two stages, accurate device modeling proves critical here. In particular, the inductors and their parasitics must be modeled carefully to achieve proper resonance frequencies.

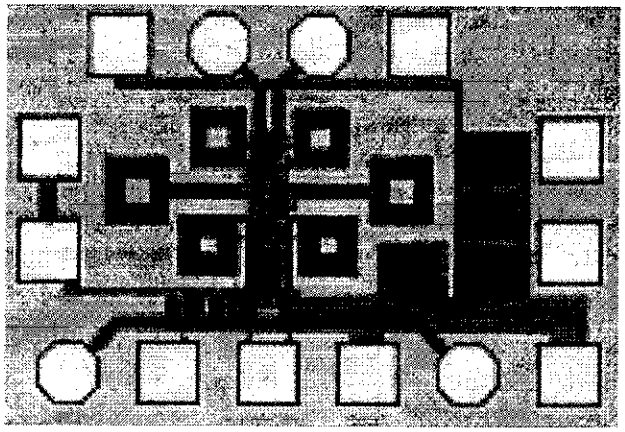

Fig. 7. Die photo.

IV. Experimental Results

The frequency divider has been designed and fabricated in a 0.18-μm CMOS technology. Shown in Fig. 7 is a photograph of the die, which measures 0.5 mm $\times$ 0.7 mm. The circuit has been tested on a high-speed probe station while running from a 2.5-V power supply.

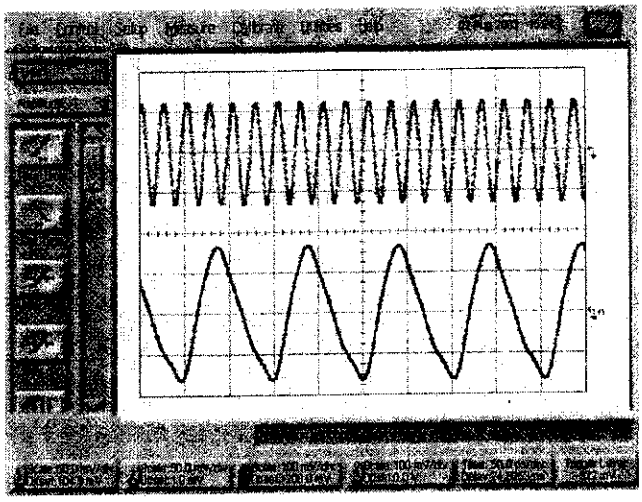

Fig. 8. Single-ended input and output waveforms of the divider. (Horizontal scale: 50 ps/div, vertical scale: 100 mV/div.)

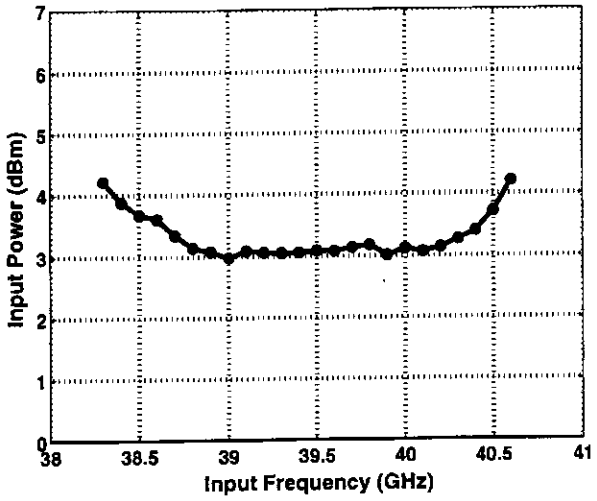

Fig. 9. Measured input sensitivity of the divider.

Figure 8 shows the measured input and output waveforms of the divider, and Fig. 9 plots the minimum required input level for correct operation. This measurement is constrained by the limited output power of the 40-GHz RF generator used here. Nonetheless, the frequency range of ± 1.25 GHz around 39.5 GHz for 1.3-dB increase in input level agrees reasonably well with that predicted by Eq. (8) if a Q of 8 is assumed at 20 GHz.

The spectrum of the 10-GHz output is shown in Fig. 10, exhibiting a phase noise of approximately -115 dBc/Hz at 1-MHz offset. The circuit draws 16.8 mW in the first stage and 14 mW in the second.

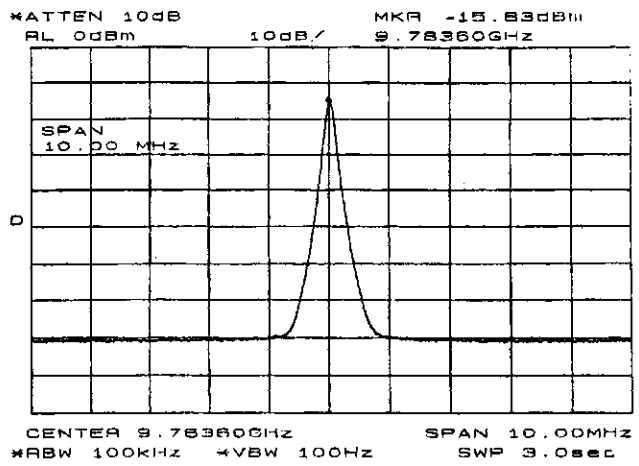

Fig. 10. Spectrum of the 10-GHz output. (Horizontal scale: 1 MHz/div., vertical scale: 10 dB/div.)

References

[1] R. L. Miller, "Fractional-Frequency Generators Utilizing Regenerative Modulation," *Proc. IRE*, vol. 27, pp. 446-456, July 1939.

[2] M. Danesh et al., "A Q-Factor Enhancement Technique for MMIC Inductors," *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, pp. 217–220, April 1998.

[3] M. Kuriso et al, "A Si Bipolar 28GHz Dynamic Frequency Divider," *ISSCC Dig. Tech. papers*, pp. 92-93, Feb. 1992.

[4] Hui Wu and Ali Hajimiri, "A 19GHz 0.5mW 0.35 μmm CMOS Frequency Divider with Shunt-Peaking Locking Range Enhancement," *ISSCC Dig. of Tech. Papers*, pp. 412-413, Feb. 2001.

[5] H. R. Rategh and T. H. Lee, "Superharmonic Injection-Locked Frequency Dividers," *IEEE J. Solid-State Circuits*, vol. 34, pp. 813-821, June 1999.

[6] O. E. Akcasu, "High-capacity Structures in a Semiconductor Device," US patent 5,208,725, May 1993.