19.5 A 2.4GHz RF Fractional-N Synthesizer with 0.25f_{REF} BW

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The loop bandwidth of conventional RF fractional-N synthesizers has been limited to about $f_{REF}/10$ despite the use of methods that suppress the $\Delta\Sigma$-modulator quantization noise [1-4]. The trade-off between the loop bandwidth and the $\Delta\Sigma$ noise peaking becomes more serious if the synthesizer employs a ring oscillator to achieve multiband operation, less unwanted coupling, and greater design flexibility than LC oscillators [5].

This paper proposes a simple, robust fractional-N architecture that reduces the $\Delta\Sigma$ noise peak at $f_{REF}/2$ by 62dB without significant bandwidth penalty. The synthesizer can thus incorporate a ring oscillator while achieving a performance commensurate with WiFi receivers and transmitters.

We wish to suppress the $\Delta\Sigma$ noise before it reaches the first potentially nonlinear stage in the loop, preferably using a single dual-modulus feedback divider. If this divider one-bit output is applied to an FIR filter with a transfer function of the form $\alpha_0 + \alpha_1 z^{-1} + \ldots + \alpha_n z^{-n}$ (Fig. 19.5.1), then a sharp roll-off can be realized by proper choice of the α coefficients, and with negligible peaks in the transfer function. Such an endeavor entails a number of issues. (1) The filter order, n, must be high enough; e.g., a 35-tap Kaiser-Bessel filter has a 3dB bandwidth of $0.02f_{REF}$ and an attenuation of 62dB at $f_{REF}/2$. (2) The filter bandwidth, e.g., $0.02f_{REF}$, must not limit the synthesizer bandwidth, an interesting dilemma given that the filter follows the divider and, evidently, affects the loop characteristics. (3) If immediately following the delay stages, the α coefficients must be implemented in the digital domain, necessitating digital multipliers, creating multi-bit outputs, and leading to a complex phase detector.

With these considerations, we introduce the approach illustrated on the bottom of Fig. 19.5.1. Here, 34 delay lines serve as the required z^{-1} stages and the coefficients are realized after the XOR phase detectors by means of R_0, $R_1, \ldots, R_n$. In other words, the FIR filter and the phase detector are merged. Moreover, the delay lines are directly clocked by the VCO output and hence do not limit the loop bandwidth [6]. Specifically, a phase step at the VCO output simultaneously reaches all of the delay stages and is therefore not impeded by the filter transfer function. In other words, the $\Delta\Sigma$ noise experiences the filter action, but the VCO output does not.

The proposed approach merits a few remarks. First, the XOR phase detectors exhibit negligible nonlinearity, and can process high $\Delta\Sigma$-modulator noise without folding it to low frequencies. Second, the necessary matching among the combining resistors, R_0 to R_{34}, is much simpler to achieve than in charge pumps, especially in view of channel-length modulation in the latter. According to Monte Carlo simulations, a one-σ resistor mismatch of 1% degrades the attenuation at $f_{REF}/2$ from 62dB to 55dB, still sufficient even for a third-order $\Delta\Sigma$. Third, the delay stages in Fig. 19.5.1 must provide a delay equal to T_{REF}, while their flipflops are clocked at the VCO frequency. That is, each delay stage must incorporate about 100 flipflops, potentially consuming a high power, but, since the data flowing through the flipflops is still at f_{REF}, we need consider only the power dissipation in the clock path.

The proposed approach avoids conventional fractional-N-loop remedies and, except for resistor matching, operates as a simple, fully digital, robust solution. The overall synthesizer architecture is shown in Fig. 19.5.2. In a manner similar to the work in [5], the single-loop design incorporates a master-slave sampling filter (MSSF) to reduce the large reference ripple otherwise created by the XOR gates, and a harmonic trap to further suppress the ripple. As shown in [5], the XOR/MSSF combination allows a loop bandwidth approaching $f_{REF}/2$. The VCO is a three-stage varactor-tuned ring topology and draws 3mW.

The high suppression provided by the FIR filter allows an aggressive choice of the $\Delta\Sigma$-modulator order, 3 in this work. Note that in conventional loops, such an order dictates a loop bandwidth of $f_{REF}/50$ [4], imposes more stringent linearity requirements on the charge pump to minimize noise folding, and also makes it difficult to utilize feedforward DAC cancellation due to large phase fluctuations reaching the charge pump. In our work, an on-chip cascaded MASH topology realizes the function in a compact, low-power form.

The synchronous delay lines (ΔT's) in the FIR filter of Fig. 19.5.2 must deal with phase offset accumulation. Clocked at the VCO frequency, $(N + \alpha)f_{REF}$, each stage generates a delay equal to $\Delta T = NT_{VCO} = T_{REF}N/(N + \alpha) \approx (1 - \alpha/N)T_{REF}$ (Fig. 19.5.3). As α goes from 0 to 1, the delay departs from T_{REF}, and the error, $(\alpha/N)T_{REF}$, accumulates over 34 stages, thereby creating a large phase offset. One or more of the XORs may thus perform phase comparison on the negative-slope section of their characteristics while the rest do on the positive-slope section (or vice versa). The change in the slope translates to nonlinearity, folding down high-frequency $\Delta\Sigma$-modulator noise as the phase fluctuates randomly. We propose a method of eliminating this effect by making ΔT programmable in conjunction with the frequency control word (FCW). Based on inserting or removing flipflops, the programmability affords a resolution of T_{VCO} for ΔT. To further increase the resolution, all three phases of the VCO are available for clocking the last flipflop in the delay stages; the resolution is therefore equal to $T_{VCO}/3 \approx 140$ps, and the maximum error equal to $T_{VCO}/6$. This ensures that all XORs operate with the same slope polarity.

The delay lines in the FIR filter contain a total of 34×108 = 3672 flipflops. The power consumption is given by the total width of the clocked transistors and the interconnect capacitance in the clock path. To minimize the former, the flipflops are realized as TSPC stages with W/L = 160nm/40nm for the clocked devices. A compact layout with dimensions of 170µm×200µm ensures short interconnects. The FIR filter draws 5.6mW, a value that directly scales down with technology.

The fractional-N synthesizer has been fabricated in TSMC 45nm digital CMOS technology. Figure 19.5.7 shows the die and an active area of 320µm×300µm. The synthesizer operates from 2.31 to 3.05GHz and draws 10mW from a 1V supply. The prototype has been characterized with f_{REF}=22.6MHz (generated by a low-noise crystal oscillator) and in two cases: (1) only the first two taps of the FIR filter are enabled, and (2) all taps are enabled. Figure 19.5.4 shows the corresponding measured output spectra, revealing considerable noise folding in the former (top) and 45dB reduction at 10MHz offset in the latter (bottom). This corresponds to 62dB of attenuation compared to the case of no FIR action. Here, the divide ratio is equal to $107 + 2^{-15} + 2^{-16}$, giving f_{VCO} = 2.416GHz. The reference sidebands fall to -60dBc.

Figure 19.5.5 plots the phase noise profiles. With only two FIR taps enabled, the phase noise remains around -76dBc/Hz for offsets as high as 10MHz. With all taps enabled, the roll-off begins around 5kHz, reaching -121.4dBc/Hz at 10MHz offset. Integrated from 10kHz to 50MHz, the rms jitter is reduced from 100ps in the former to 1.5ps in the latter. The closed-loop bandwidth is 5.5MHz. Figure 19.5.6 summarizes the performance of our prototype and other synthesizers. Our circuit performance even approaches that of the LC-based synthesizer in this figure if we take into account the factor of 2 difference in f_{REF}.

Acknowledgements:
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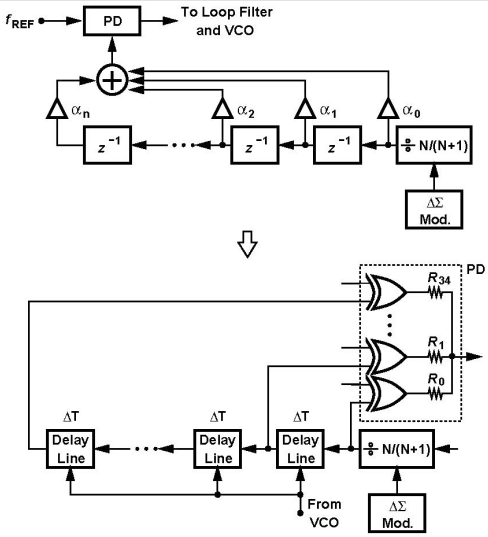

Figure 19.5.1: Conceptual diagram of FIR filter (top) and its realization with XOR PDs (bottom).

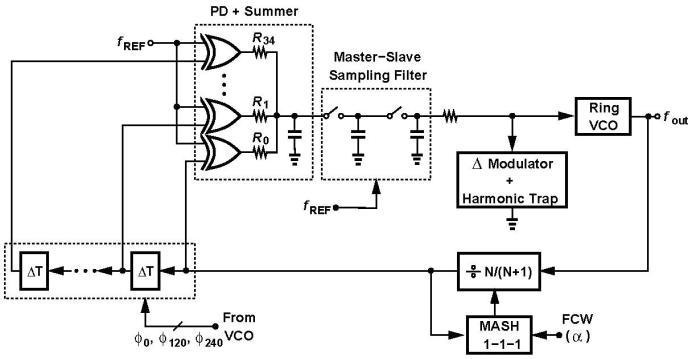

Figure 19.5.2: Proposed fractional-N synthesizer architecture.

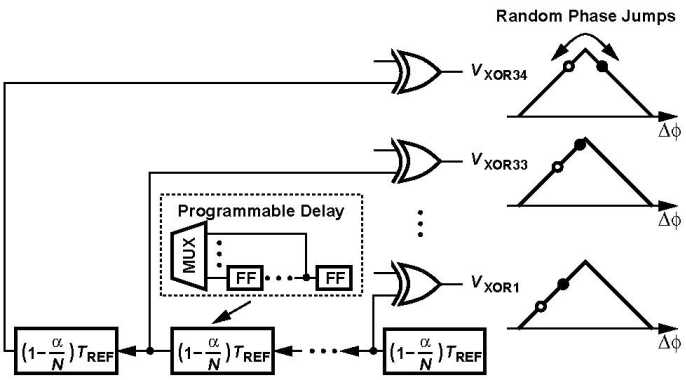

Figure 19.5.3: Effect of phase offset accumulation on the operation of XOR PDs.

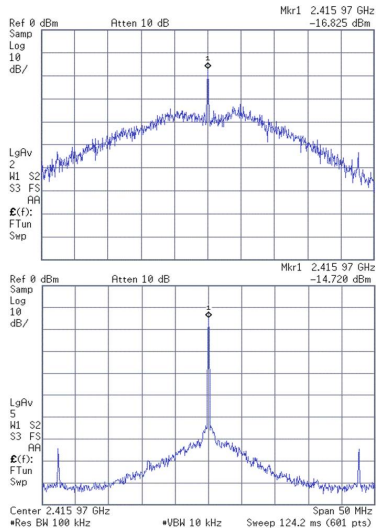

Figure 19.5.4: Measured output spectra with 2-tap (top) and 35-tap (bottom) FIR filter.

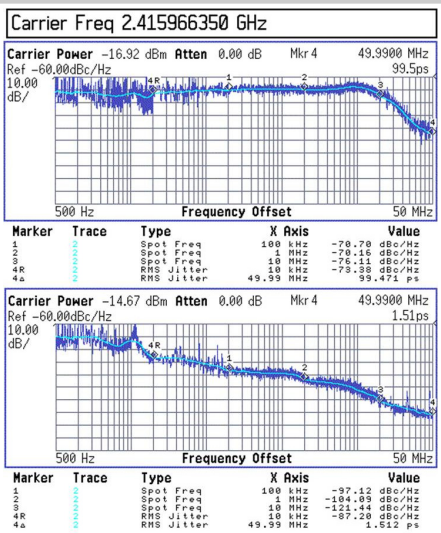

Figure 19.5.5: Measured phase noise with 2-tap (top) and 35-tap (bottom) FIR filter.

	Jee ISSCC'11	Kao ISSCC'13	Chang JSSC, Dec. 14	Liang ISSCC'15	Kong VLSI'16	This Work
Oscillator Topology	Ring	Ring	LC	Ring	Ring	Ring
Reference Freq. (MHz)	32	26	48	26	22.6	22.6
Output Frequency (GHz)	1	1.87	2.27	2	2.37	2.42
f_{BW}/f_{REF}	0.1	0.077	0.01	0.058	0.5	0.25
Phase Noise @ 1–MHz offset (dBc/Hz)	−103	−98	−114	−98	−109	−104
Phase Noise @ 10–MHz offset (dBc/Hz)	−114	−115	−135	−115	−113.6	−121.4
RMS Jitter (ps) Integ. range (MHz)	N/A	3.4 (0.004~40)	0.36 (0.01~30)	2.4 (0.001~40)	1.7 (0.01~50)	1.5 (0.01~50)
Ref. Spur (dBc)	−66	−67	−55	−87	−70	−60
Freq. Resolution (kHz)	N/A	0.1	N/A	0.1	0.95	0.34
Power (mW)	16.8	10	17.3	9.1	6.4	10
Area (mm^2)	0.31	0.047	0.75	0.046	0.03	0.096
Tech. (nm)	130	40	180	40	45	45
FoM @ 1–MHz offset (dB)	150.7	153.4	168.7	154.4	168.4	161.7

$$\text{PLL FoM} = 10\log_{10}[(\frac{f_{osc}}{\Delta f})^2(\frac{1\text{ mW}}{\text{Power}})] - \text{Phase Noise (dBc/Hz)}$$

Figure 19.5.6: Performance summary and comparison with state of the art.

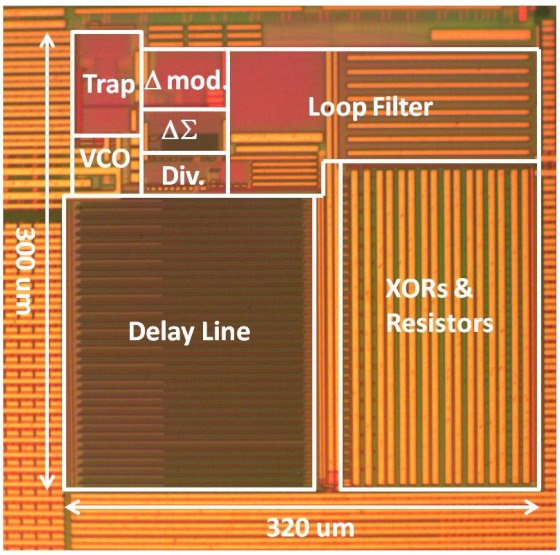

Figure 19.5.7: Synthesizer die micrograph.

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