A Self-Calibrating 900-MHz CMOS Image-Reject Receiver

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Abstract

This paper introduces an analog phase and gain calibration technique for image-reject receivers. The technique uniquely detects the phase and gain mismatches and drives their magnitudes toward zero through the use of a negative-feedback loop. An experimental CMOS prototype operating at 900 MHz achieves an image rejection ratio of 57 dB by applying phase calibration to a Weaver architecture. Fabricated in a 0.35-µm CMOS technology and running from a 3-V supply, the receiver dissipates 105 mW during the receive mode and 170 mW during the calibration mode.

1. Introduction

Heterodyne receivers provide a robust solution for the processing of small RF signals in the presence of large interferers. Such architectures, however, suffer from a trade-off between image rejection and channel selection: a higher intermediate frequency (IF) allows a more relaxed image-reject filtering but requires a more difficult channel-select filtering. Furthermore, the external imagereject filter interposed between the low-noise amplifier (LNA) and the first mixer leads to a higher cost and greater power dissipation. Image-reject architectures offer a method of improving the above trade-off, but their performance is very sensitive to phase and gain mismatches. While polyphase filters have been used to lower this sensitivity [1,2], they typically introduce substantial loss in the signal path, demanding a high power dissipation.

This paper introduces an analog self-calibration technique that uniquely determines the phase and gain mismatches of a Weaver architecture and applies feedback through phase and gain adjustment to improve the image rejection. Experimental results indicate that phase calibration by itself boosts the image rejection from 17 dB to 57 dB at 900 MHz with no external filters.

2. Self-Calibration Technique

The self-calibration technique is described in the context of the Weaver architecture [3] shown in Figure 1. In this design, $f_{LO1} = 1$ GHz and $f_{LO2} = 100$ MHz.

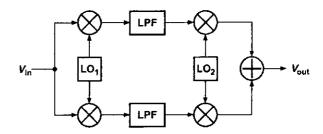


Figure 1. Weaver image-reject receiver.

Each quadrature signal path has a nominal voltage conversion gain of A, and the total gain and phase mismatches between the two paths are denoted by ΔA and θ , respectively. For an image signal of amplitude V_m and frequency ω_{IMG} , finite mismatches yield an output that, after low-pass filtering, is given by

$$V_{\text{out}} = \left(A + \frac{\Delta A}{2}\right) V_{\text{m}} \sin\left(\omega_{\text{IF}}t + \frac{\theta}{2}\right) \qquad (1)$$
$$-\left(A - \frac{\Delta A}{2}\right) V_{\text{m}} \sin\left(\omega_{\text{IF}}t - \frac{\theta}{2}\right)$$

where

$$\omega_{IF} = |\omega_{IMG} - \omega_{LOI} - \omega_{LO2}|$$

For $\theta \ll 1$ rad and $\Delta A \ll 1$, the image-rejection ratio (IRR) is given by [4]:

$$IRR^{-1} = \frac{\theta^2 + (\Delta A/A)^2}{4}$$

The proposed calibration technique detects θ and ΔA and adjusts the phase and gain so as to suppress these errors. Since the results are stored on capacitors, the calibration must be performed periodically. This is feasible in time-division multiple access (TDMA) systems, where the receiver remains idle between time slots. Most of the calibration circuitry can be turned off during normal reception to save power. For longer retention, the calibration results may be stored digitally.

The principal challenge in calibration is that IRR is a function of two variables, making it difficult to ensure convergence in the feedback loop. For this reason it is desirable to detect and adjust the variables independently.

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2.1. Phase Calibration

Equation (1) provides the starting point for the calibration technique. If as shown in Figure 2(a), V_{out} is multiplied by a tone $\cos(\omega_{IF}t)$, we have

$$V_{\text{out}} \cdot \cos(\omega_{\text{IF}} t) = \left(A + \frac{\Delta A}{2} \right) \frac{V_{\text{m}}}{2} \left[\sin\left(2\omega_{\text{IF}} t + \frac{\theta}{2}\right) + \sin\frac{\theta}{2} \right]$$
$$- \left(A - \frac{\Delta A}{2} \right) \frac{V_{\text{m}}}{2} \left[\sin\left(2\omega_{\text{IF}} t + \frac{\theta}{2}\right) - \sin\frac{\theta}{2} \right]$$

After low-pass filtering this result, we obtain the phase mismatch information:

$$V_{\theta} = A \cdot V_{\text{m}} \sin\left(\frac{\theta}{2}\right) \approx A \cdot V_{\text{m}}\left(\frac{\theta}{2}\right)$$

Note that V_{θ} contains both the sign and magnitude of the phase mismatch and is independent of the gain mismatch. Thus, the phase calibration results are not corrupted by gain calibration.

Before using V_{θ} for phase correction, we must generate the multiplicative tone $\cos(\omega_{IF}t)$. As depicted in Figure 2(b), two downconversion mixers driven by LO₁ and LO₂ readily produce this component. As explained below, since the noise and linearity of the three additional mixers are unimportant, the power penalty is negligible.

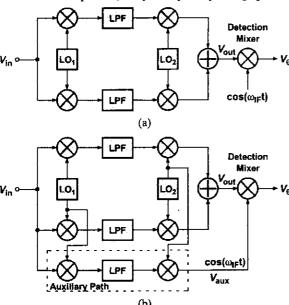


Figure 2. (a) Error signal generation, (b) practical realization.

The phase mismatch information provided by V_{θ} can now be utilized in a feedback loop incorporating variable delay cells that adjust the signal or LO phases. Figure 3 shows the overall architecture. To avoid corrupting the signal or the first LO output, which typically has a much higher frequency than LO₂, the delay lines are placed in the quadrature paths of the second LO. The low-pass filters are simply first-order sections to suppress high-frequency components.

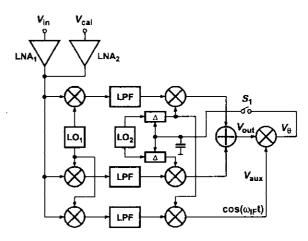


Figure 3. Image-reject receiver with phase calibration loop.

The system operates as follows. During calibration, LNA₁ is off, LNA₂ is on, a single calibration tone is applied at $V_{\rm cal}$, the three additional mixers generate $V_{\rm \theta}$, and the two delay cells (Δ) are varied differentially so as to drive $V_{\rm \theta}$ toward zero. When the loop settles, the final value of $V_{\rm \theta}$ is stored across the capacitor, S₁ and LNA₂ are turned off, and LNA₁ is turned on.

In the architecture of Figure 3, three issues must be addressed. First, during calibration, the leakage of $V_{\rm cal}$ to the antenna may be of concern. Thus, LNA₁ must achieve a reasonable reverse isolation when it is off (e.g., on the order of 45 dB if $V_{\rm cal}$ is about -15 dBm). Second, the noise and linearity of the three additional mixers used for calibration are unimportant because $V_{\rm cal}$ is a single tone with an amplitude of tens of millivolts. Third, dc offsets corrupting the detection mixer output (e.g., due to self-mixing of the LO) limit the overall correction of the phase. For this reason, a simple offset-cancellation circuit is added to this mixer.

Most of the building blocks in the receiver employ differential signaling. In particular, V_{θ} and the delay cells are differential, suppressing systematic errors because their nominal phase shift is equal to zero when $V_{\theta}=0$. Moreover, storing V_{θ} differentially greatly reduces the effect of leakage currents.

In order to maximize the calibration loop gain and overwhelm the dc offsets of the delay cells, the mixer producing V_{θ} is designed with a high conversion gain. The mixer's high output impedance and the sampling capacitors form a low-pass filter, suppressing the ripple in V_{θ} . The filter also stabilizes the loop.

The architecture of Figure 3 entails two other issues as well. First, the calibration tone must be generated. Since the amplitude and purity of this tone are not critical, a single-sideband mixer using the first LO frequency and half of the second LO frequency can readily produce a tone at $f_{\text{LOI}} + f_{\text{LOI}}/2 \approx 1050 \text{ MHz}$, which is in the vicinity of the image. Second, the phase mismatch

between the auxiliary path and the two main signal paths has only a minor effect on the calibration. It can be shown that a phase mismatch of ϕ leads to the multiplication of the loop gain by $\cos \phi$. Thus, even mismatches of several tens of degrees can be tolerated. Note that the proposed technique does not degrade the noise, linearity, or gain of the main signal path.

In the actual implementation, quadrature auxiliary paths are used for two reasons. First, they minimize systematic mismatches due to asymetric loading of the LO paths. Second, combining the quadrature auxiliary paths cancels the sum frequency generated in the second downconversion, providing a cleaner signal, $V_{\rm aux}$, with which to mix $V_{\rm out}$.

2.2. Gain Calibration

If V_{out} in Equation (1) is multiplied by $\sin(\omega_{\text{IF}}t)$, then an error signal containing the amplitude mismatch is obtained:

$$V_{\Delta A} = V_{\text{out}} \cdot \sin(\omega_{\text{IF}} t) = \frac{\Delta A}{2} \cdot \cos(\frac{\theta}{2}) \approx \frac{1}{2} \Delta A$$
 (2)

As with V_{θ} , $V_{\Delta A}$ carries both sign and magnitude information. Utilizing this error to adjust the gain of the second downconversion mixers in the Weaver architecture can drive the gain error toward zero. To minimize the interaction between phase and gain calibration, only a *fraction* of the gain can be controlled.

3. Building Blocks

In order to demonstrate the feasibility of the proposed technique, a CMOS receiver incorporating the phase calibration scheme has been designed and tested. Since the emphasis is on improving image rejection, other aspects of design are optimized to a lesser extent.

3.1. RF Front End

For testing simplicity, a common-gate LNA topology is chosen for both LNA₁ and LNA₂. Depicted in Figure 4, the two LNAs drive an on-chip balun and subsequently a double-balanced mixer.

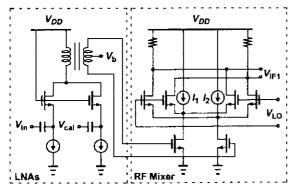


Figure 4. RF front end.

The currents I_1 and I_2 are added to (1) increase the conversion gain (because the load resistors can be larger), (2) decrease the required LO drive, and (3) lower the channel thermal noise injected by the switching quad to the output. The mixers in the auxiliary path are based on the same topology. The first LO frequency is 1 GHz, placing the image at 1.1 GHz. The RF mixers are capacitively coupled to the IF mixers.

3.2. IF Mixers

The IF mixers in the signal path utilize the same topology as the RF mixers. The outputs of the quadrature IF mixers are combined in the current domain by sharing a common resistive load. This output is then used to drive the input differential pair of the detection mixer.

The IF mixers in the auxiliary path are designed to have higher gain, less linearity, and less current than those of the signal path. Unlike the signal path, the auxiliary path need not be linear. In fact, since the output of the auxiliary path is used to drive the LO port of the detection mixer, a large, rectangular waveform is desired. As with the signal path, the outputs of the IF mixers in the auxiliary paths are added in the current domain and share a common load. An active PMOS load with simple common-mode feedback is used to obtain a high output impedance. The second LO frequency is about 100 MHz, centering the output spectrum around the zero frequency.

3.3. Mismatch Detection Mixer

Much of the calibration loop gain is provided by the detection mixer (Figure 5). The circuit is implemented as a Gilbert cell with a folded-cascode load, yielding a high conversion gain. This topology easily lends itself to offset cancellation. When switches S_1 and S_2 are on, transistors M_1 and M_2 sense the output offset of the mixer, returning a corrective differential current to the folding points. After the loop has settled, S_1 and S_2 turn off, sampling the offset error voltage onto C_1 and C_2 . This differential voltage need not be stored for a long period because it is used only during phase calibration.

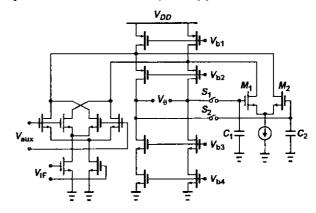


Figure 5. Detection mixer with offset cancellation (commonmode feedback not shown).

3.4. Variable-Delay Cell

The variable-delay cell is realized by interpolating between the phases of a fast signal path and a slow signal path (Figure 6). The fast path consists of a single differential pair M_5 - M_6 and the slow path a cascade of two differential pairs, M_1 - M_2 and M_3 - M_4 . Phase control is achieved by adjusting the gain in each path through the differential pair M_7 - M_8 . The resulting output phase is a weighted sum of the phase delays in the two paths.

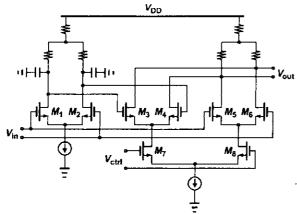


Figure 6. Variable-delay cell.

4. Experimental Results

The receiver is implemented in a 0.35-µm CMOS technology. Shown in Figure 7, the die is packaged in a 48-pin thin quad flat package (TQFP) with exposed down-set paddle. A two-stage polyphase filter for each LO is implemented on the test board to generate quadrature LO signals. Interestingly, the board parasitics and asymmetries introduce so much mismatch that the intrinsic image rejection of the receiver is only 17 dB.

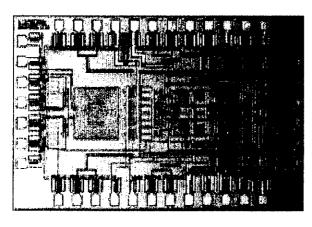


Figure 7. Die photo.

Calibration is performed in two steps: (1) the dc offset is cancelled, and the differential error voltage is stored on capacitors; (2) a calibration tone at 1.1 GHz is injected, the phase is calibrated, and the differential error voltage is stored on capacitors.

After phase calibration, image rejection is measured by injecting a desired tone (900 MHz) and an image tone (1100.2 MHz) of equal power and measuring the difference in the downconverted tones at 15 MHz (desired) and 14.8 MHz (undesired). (Here, $f_{\rm LO2}=115$ MHz.) As shown in Figure 8, phase calibration improves IRR from 17 dB to 57 dB.

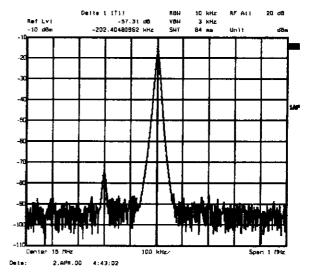


Figure 8. Output spectrum after calibration with a desired tone at 15 MHz and an image at 14.8 MHz.

5. Conclusion

A self-calibration method has been introduced that substantially improves the image rejection of RF receivers with no penalty in noise, linearity, or gain and only a small increase in power dissipation. Independent detection and correction of phase and gain mismatches allow a high IRR regardless of the frequency difference between the signal and the image, eliminating the trade-off between image rejection and channel selection.

An experimental prototype designed in a 0.35-µm CMOS technology exhibits an image rejection of 57 dB by phase calibration. It is expected that addition of gain calibration achieves rejections above 70 dB.

Acknowledgement

The authors wish to thank Silicon Wave, Inc. for generous design, fabrication, and test support.

References

- [1] J. Crols and M. S. J. Steyaert, "A Single-Chip 900 MHz CMOS Receiver Front-End with a High-Performance Low-IF Topology," *IEEE Journal of Solid-State Circuits*, Vol. 30, No. 12, pp. 1483-1492, Dec. 1995.
- [2] F. Behbahani et al, "An Adaptive 2.4-GHz Low-IF Receiver in 0.6-µm CMOS for Wideband Wireless LAN," ISSCC Dig. of Tech. Papers, pp. 146-147, Feb. 2000.
- [3] D. K. Weaver, Jr., "A Third Method of Generation and Detection of Single-Sideband Signals," *Proc. IRE*, pp. 1703-1705, June 1956.
- [4] B. Razavi, *RF Microelectronics*, Englewood Cliffs, NJ: Prentice-Hall, 1998, p. 143.