4.7 A 300GHz 52mW CMOS Receiver with On-Chip LO Generation

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Data communication in the 300GHz band has found renewed interest in the past few years. Two reasons can account for this trend. First, the IEEE 802.15.3d standard was established in 2017 for radios in the unallocated frequency band from 252GHz to 322GHz [1]. Second, a number of researchers have demonstrated the viability of such radios in CMOS technology [2-5]. For 300GHz transceivers to serve as an attractive complement to WiFi and WiGig, they should perform extensive beam forming so as to overcome the path loss. This point underscores the importance of low power consumption per element. Moreover, high-order modulation schemes require a local oscillator (LO) signal with very low phase noise. Unfortunately, the generation and distribution of LO phases proves extremely power hungry, making the realization of a single-chip 300GHz CMOS data-communication radio a difficult challenge.

In addition to the limited speed of the technology, the principal challenge here is the need for quadrature downconversion. The prior art therefore begins with an external LO of around 50GHz, multiplies it up, and generates quadrature phases by passive devices. Thus, even without an on-chip LO generator, the power consumption of 300GHz CMOS data-communication receivers has been in the range of 140mW [2] to 897mW [1]. This paper introduces a single-chip receiver (RX) and LO generator that is realized in 28nm CMOS technology and dissipates 20mW in the signal path and 32mW in the LO path.

The proposed receiver architecture is shown in Fig. 4.7.1. A heterodyne approach offers several advantages. First, it allows quadrature signal decomposition at an IF of 27GHz, thereby decoupling the difficulties associated with generating a terahertz LO and separating it into I and Q phases. Second, it introduces only one mixer at the input, reducing the input capacitance and improving the input match. Third, we also expect lower I/Q mismatches because the separation occurs at a relatively low frequency. PLL_1 runs at 54GHz, delivering this frequency to PLL_2 and PLL_3 and its divided quadrature components to the IF mixers. The LOs are generated directly by VCOs rather than by frequency multiplication, thereby reducing the power consumption considerably.

Figure 4.7.2 shows the realization of the input mixer, MX_1, and the IF amplifier. A passive single-balanced fundamental-mode mixer driven directly by the 270GHz LO incorporates series peaking at the input to deal with the pad and ESD capacitances. The mixer switches are designed in conjunction with M_3 and M_4 for optimum performance. Specifically, the kT/C noise at the gates of M_3 and M_4 trades with the mixer conversion gain due to the limited sampling bandwidth. Moreover, the input capacitance of MX_1 trades with its noise contribution. The IF amplifier employs inductive peaking along with a PMOS cross-coupled pair to boost the gain and provide a relatively flat frequency response from zero to about 37GHz, thereby accommodating a bandwidth of 20GHz around 27GHz IF. This amplifier draws 2mW and, along with MX_1, provides a total gain of 12dB. Each IF mixer consists of a common-source stage and a double-balanced passive mixer; the baseband amplifiers also incorporate inductive peaking.

A critical issue in LO generation for data-communication radios is the reference phase noise. A 450MHz crystal oscillator with a phase noise of -168dBc/Hz yields significant jitter at 270GHz. Similarly, PFDs and charge pumps prove excessively noisy, unless the PLL bandwidth is reduced but then the VCO phase noise dominates. For these reasons, cascaded PLLs are preferable. In this work, PLL_1 has a loop bandwidth of 50MHz to limit the reference phase noise whereas PLL_2 and PLL_3 respectively benefit from loop bandwidths of 400MHz and 700MHz to suppress their VCOs' contributions. Figure 4.7.3 depicts the proposed architectures of PLL_2 and PLL_3. PLL_2 employs subsampling to double the 54GHz output of PLL_1 without a frequency divider in the feedback loop. The principal advantage of this topology over conventional doublers is that it can generate large, differential output swings with only 2.5mW of power and a phase noise of -111dBc/Hz at 10MHz offset. PLL_2 locks from 107GHz to 110GHz.

PLL_3 in Fig. 4.7.3 exploits both offset mixing and subsampling to avoid high-frequency dividers. It can be shown that without the offset mixer, the subsampling circuit bandwidth does not suffice for capturing the 270GHz output of VCO_3, causing lock failure. This PLL merits three remarks. First, it delivers differential voltage swings of at least $2\times800mV_{pp}$ to the RF mixer in Fig. 4.7.2, minimizing the conversion loss. Second, it draws 9.7mW and exhibits a phase noise of -103dBc/Hz at 10MHz offset. Third, offset mixing does not generate spurs in this environment because its output components can be expressed as 108k+270n GHz, where k and n are integers; these values are harmonics of 54GHz and map to dc after the PD.

Figure 4.7.3 also shows the 270GHz VCO design. Based on the oscillator structure in [6], the circuit utilizes magnetic feedback from the output stage, M_3-M_4, to M_1-M_2 to achieve a high speed. With the lack of varactor models at these frequencies, we employed a tuning method that adjusts the CM level at X and Y by M_5. At lower CM levels, M_1-M_4 spend more time in the off region, exhibiting a smaller average gate capacitance and hence providing a higher oscillation frequency. Resistor R_1 ensures startup even if V_{cont} begins near V_{DD}. One issue here is that the flicker noise of M_5 directly modulates the frequency, but it is still suppressed due to the 400MHz loop bandwidth. Note that M_5 is a large transistor as its parasitics do not affect the oscillation frequency. The VCO achieves an average tuning range of 7GHz, according to 5 measured samples with a power consumption of 2.5mW. The 108GHz VCO is based on the same topology, but it also uses discrete tuning.

The single-chip receiver and LO generator has been fabricated in TSMC's 28nm CMOS technology. Shown in Fig. 4.7.7 is the die whose active area measures 300µm×200µm. This prototype has been characterized by more than a dozen tests. For the receiver gain, noise figure, and I/Q matching measurements, the Virginia Diodes' WR10M-SGX-M combined with the WR3.4×3 frequency multiplier provides a 300GHz input, which travels through a waveguide probe to reach the DUT. The output power of the multiplier is monitored by Virginia Diodes' Erickson PM5B power meter. Also, the reference for PLL_1 in Fig. 4.7.3 is generated by Crystek's CRBSVS-01-450.000 450MHz crystal oscillator.

Figure 4.7.4 plots the measured RX gain. The close agreement between these results and the simulated gain of 20dB confirms that the 270GHz fundamental-mode VCO indeed delivers large voltage swings to the RF mixer. The gain variation over the bandwidth is caused by the capacitive loading seen by the passive mixers. The baseband outputs exhibit a gain mismatch of 1.2dB and a phase mismatch of 5.4°. Figure 4.7.4 also depicts the measured noise figure, computed by dividing the RX output noise by its gain. The average noise figure across the band is about 20dB. The RX linearity is evaluated by sweeping the input power level, as shown in Fig. 4.7.4, revealing an input P_{1dB} of -17.3dBm and suitability for 64QAM.

The phase noise of the PLLs is measured as follows. The output power of PLL_3 is sensed by a separate mixer (not shown in Fig. 4.7.1) that downconverts it to 1.5GHz by means of an external 90GHz LO. Figure 4.7.5 shows the resulting profile. The phase noise is about -105dBc/Hz at 10MHz offset, and the integrated jitter is $105.4fs_{rms}$. Note that this measurement includes the phase noise of PLL_2 and PLL_1 as well. For the phase noise of the 54GHz PLL, the 450MHz output of its feedback divider is monitored. The integrated jitter of this PLL is $34fs_{rms}$.

Figure 4.7.6 summarizes the performance of our prototype and compares it with that of the state of the art. In comparison to [2], which requires an external 40GHz LO, the conversion gain is improved by 36dB and the power is reduced by a factor of 2.6. In comparison to the RX in [1], which uses an external 44GHz LO, the conversion gain is improved by about 15dB and the power is reduced by a factor of 17.

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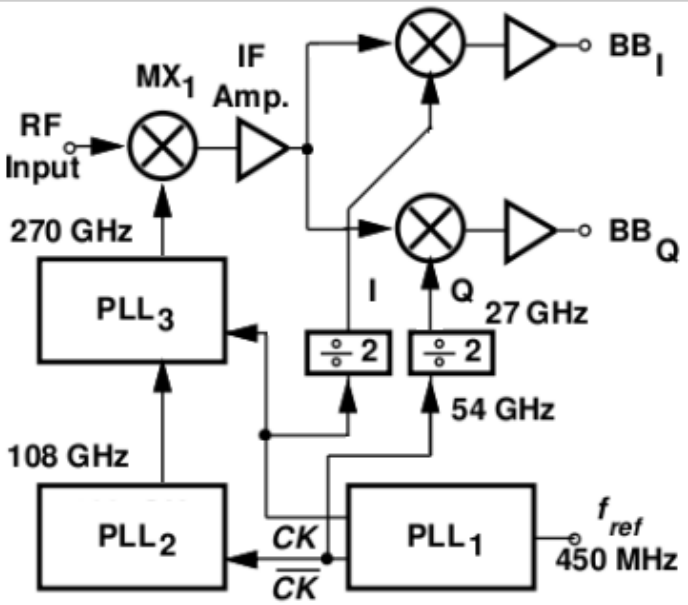

Figure 4.7.1: Overall receiver architecture.

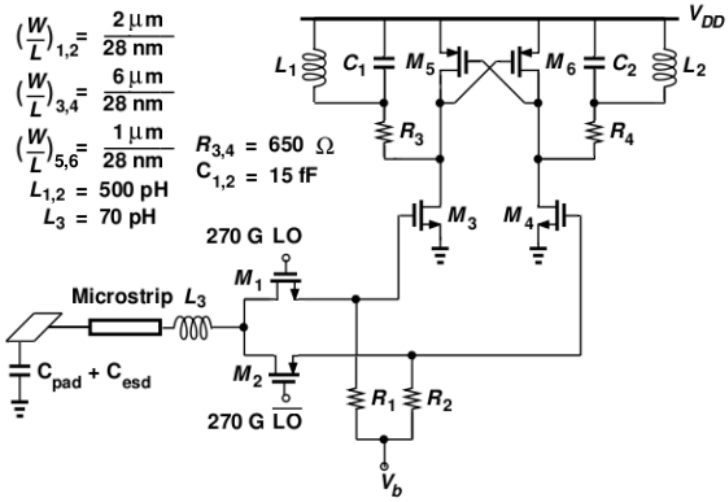

Figure 4.7.2: Schematic of input mixer and IF amplifier.

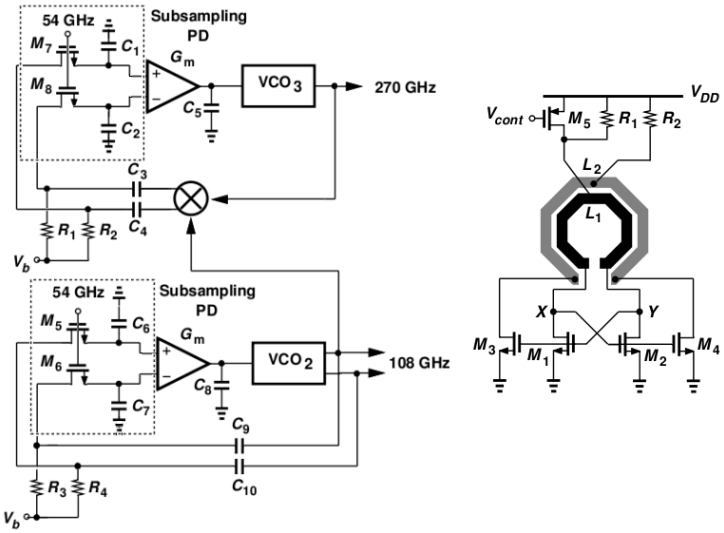

Figure 4.7.3: PLL_2 and PLL_3 combined schematic (left) with the 270GHz VCO schematic (right).

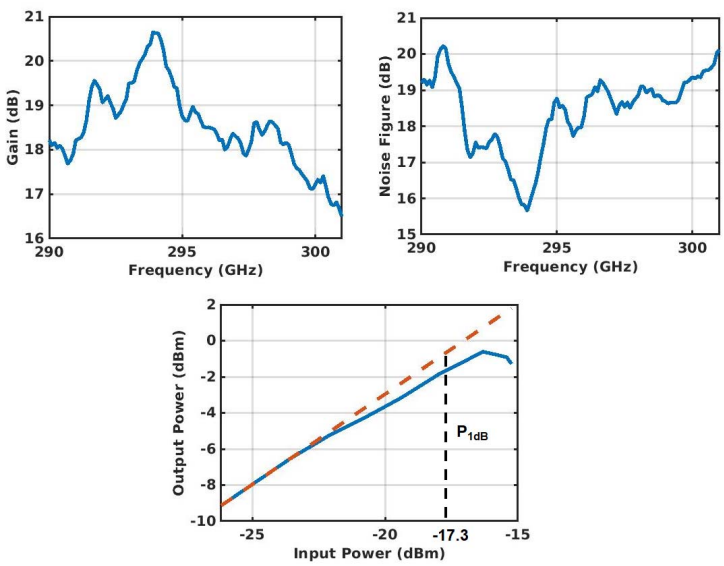

Figure 4.7.4: Gain (top left) and noise figure (top right) of the receiver. Bottom graph shows the input P_{1dB} compression point.

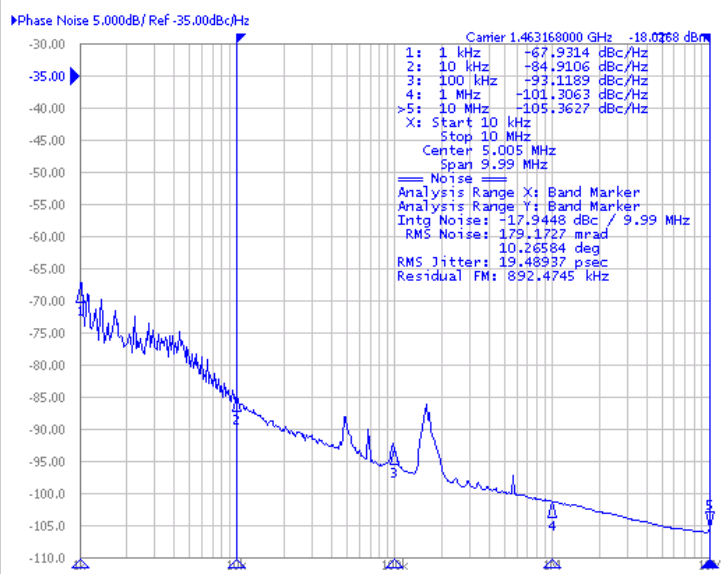

Figure 4.7.5: Phase noise of locked downconverted 270GHz signal. (The peaks near 100kHz are an artifact of the phase-noise analyzer).

	This Work	JSSC'19 [1]	MTT-S'20 [2]	APMC'18 [3]	RFIT'17 [4]
f_{min} (GHz)	289	255	278	286.5	287
f_{max} (GHz)	305	275	304	313.5	320
Gain (dB)	18	3	–16.5	–19.5	–18
Noise Fig. (dB)	20	22.9	NA	27	25.5
Power (mW)	52	897*	140*	650*	416*
Chip area (mm^2)	0.72	NA	1.9	NA	2.29
Tech. (nm)	28–nm CMOS	40–nm CMOS	65–nm CMOS	40–nm CMOS	40–nm CMOS

*with external LO

Figure 4.7.6: Performance comparison with other state-of-the-art 300GHz receivers.

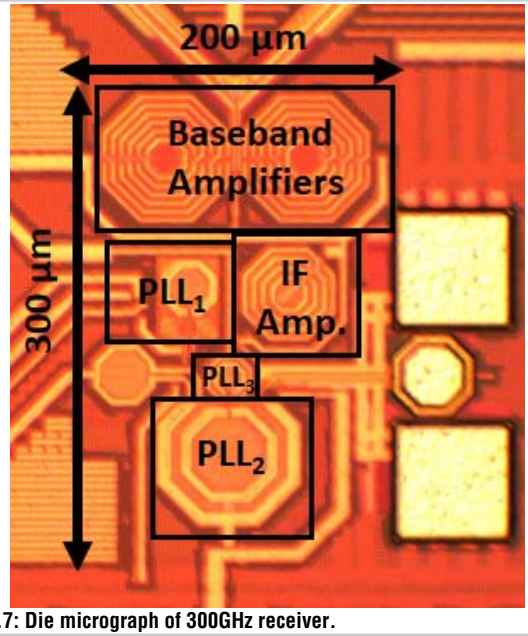

Figure 4.7.7: Die micrograph of 300GHz receiver.

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