A 3-GHz 25-mW CMOS Phase-Locked Loop

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The demand for high-speed, low-power communication circuits has dramatically grown over the past few years. Potential markets from powerful personal communicators to wireless ATM systems have stimulated great effort in reducing the supply voltage and power dissipation of gigahertz circuits. In this respect, deep submicron CMOS technologies have become contenders to III-V and silicon bipolar devices because they offer the speed, density, and power required for such applications.

This paper describes the design of a 3-GHz phase-locked loop (PLL) fabricated in a partially-scaled 0.1-μm bulk CMOS technology [1]. The circuit employs a number of techniques to allow operation from a low supply voltage and overcome the limitations due to device layout rules described below.

In order to improve the yield and reduce the turnaround time and cost, the CMOS process used here scales only the channel length to 0.1 μm and the gate oxide thickness to 40 Å [1]. The remaining dimensions follow the design rules of a typical 1-μm technology, yielding a minimum source/drain area of 2.2 μm $\times$ 2.2 μm (Figure 1(a)). Since the contribution of the source/drain junction capacitance is substantial, the regular structure of Figure 1(a) does not take full advantage of the drive capability provided by partial scaling.

To resolve this issue, ring-shaped transistors such as that in Figure 1(b) can be used, but only if the source terminal does not appear in the signal path. Under this condition, the ring-shaped geometry proves beneficial because the ratio of its effective width and its drain junction capacitance is approximately 4 times that of Figure 1(a). It also provides a lower gate resistance, an important issue in wide, short-channel MOSFETs [2].

The principal challenge in the design of this PLL has been to develop circuit topologies in which only one of the source or drain terminals is utilized in the high-speed path. In addition, the use of PMOS devices has been limited to noncritical places so that their transconductance-input capacitance trade-off has little impact on the speed.

Figure 2 shows the PLL block diagram. It consists of an input buffer and a loop including a mixer, a low-pass filter (LPF), a current amplifier, and a current-controlled oscillator (CCO). The oscillator output drives an open-drain NMOS device, delivering a few milliamperes of current to an external 50-Ω load.

The input buffer is designed so as to present the same waveform and impedance to the mixer as does the CCO. This reduces the static phase error because at high speeds mixers are sensitive to the waveform and the driving impedance seen at their inputs.

The design of the loop oscillator has influenced all aspects of the PLL's performance. While it is desirable to implement the circuit and its control in differential form to suppress the effect of common-mode noise, low supply voltages ($\leq$ 3 V) limit the headroom, making it difficult to utilize differential amplifiers. Thus, the oscillator uses a single-ended toplogy, but it employs current-mode control signals to lower the sensitivity to supply and substrate noise.

Shown in Figure 3 is the CCO circuit diagram. Using a three-stage ring oscillator with controlled current sources as loads, the CCO achieves both a wide tuning range and a maximum speed relatively independent of PMOS characteristics. This configuration also yields a low phase noise because the noise contributed by the PMOS transistors to the output can be minimized without incurring a speed penalty. Note that all the devices are ring-shaped here.

Figure 4 depicts the mixer-LPF-amplifier cascade. Transistors M_1-M_6 constitute an exclusive NOR (XNOR) gate, M_7 and C_L form the LPF, and M_8-M_{10} operate as a current amplifier. The bias voltage V_{b1} is approximately equal to $V_{DD}/2$ and I_1 functions as coarse frequency control. To understand the operation of the XNOR gate, note that when A is low, only M_4 and M_5 are active and $V_X = \overline{B}$. Similarly, when B is low, $V_X = \overline{A}$. Thus, $V_X = \overline{A \oplus B}$.

In contrast to the conventional CMOS XOR [3], the proposed mixer has two advantages: 1) it is inherently symmetric with respect to inputs A and B, and hence free from systematic phase error; 2) it easily lends itself to implementation with ring-shaped devices (with their low-capacitance terminals connected to nodes P and Q). This circuit, however, dissipates static power when A or B is high, a nonetheless minor issue at an operating speed of 3 GHz.

The PLL has been fabricated in our 0.1-μm CMOS process. Shown in Figure 5 are photographs of the die and the core. The circuit has been tested on wafer using high-speed Picoprobes to apply the input and sense the output and a Cascade multi-contact probe to provide power and ground connections. All tests are performed at room temperature with a supply voltage of 2.8 V.

Figures 6(a) and (b) show the 3-GHz output waveform and its jitter histogram, respectively. The jitter is 3.6 psec rms and 36 psec peak-to-peak. The PLL (including the I/O buffers) dissipates 25 mW at this frequency. The tracking range is 350 MHz around 3 GHz.

The spectral purity of the output is illustrated in Figure 7; all side bands drop to 55 dB below the carrier at frequency offsets greater than 50 kHz. Attributed to the setup, the pattern of sidebands around the carrier is currently under investigation.

The small jitter and high spectral purity indicate that the circuit may be useful in both timing recovery applications and RF synthesizers.

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References

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[2] B. Razavi, R. H. Yan, and K. F. Lee, "Impact of Gate Resistance on the Performance of MOS Devices," to be published in *IEEE Trans. Circuits and Syst. - Part I.*
[3] K. M. Ware, H. S. Lee, and C. G. Sodini, "A 200-MHz CMOS Phase-Locked Loop with Dual Phase Detectors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1560-1568, Dec. 1989.

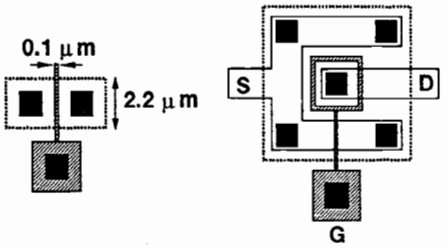

Fig. 1. (a) Regular and (b) ring-shaped MOS structures.

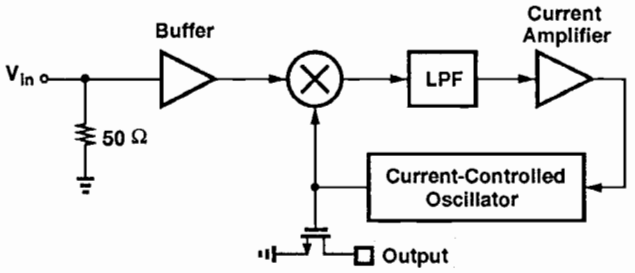

Fig. 2. PLL block diagram.

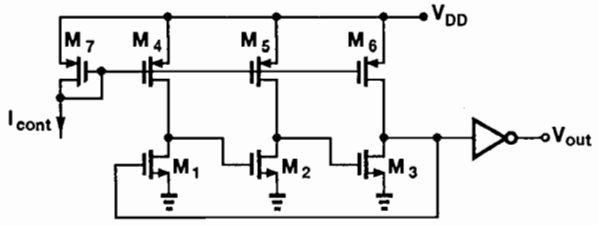

Fig. 3. Current-controlled oscillator.

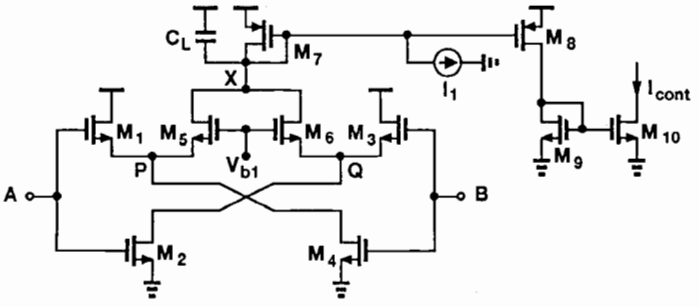

Fig. 4. Mixer, LPF, and current amplifier.

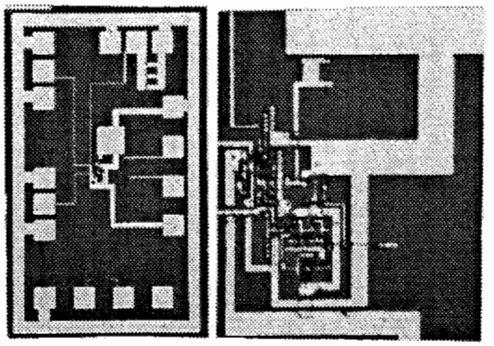

Fig. 5. PLL die and core photos.

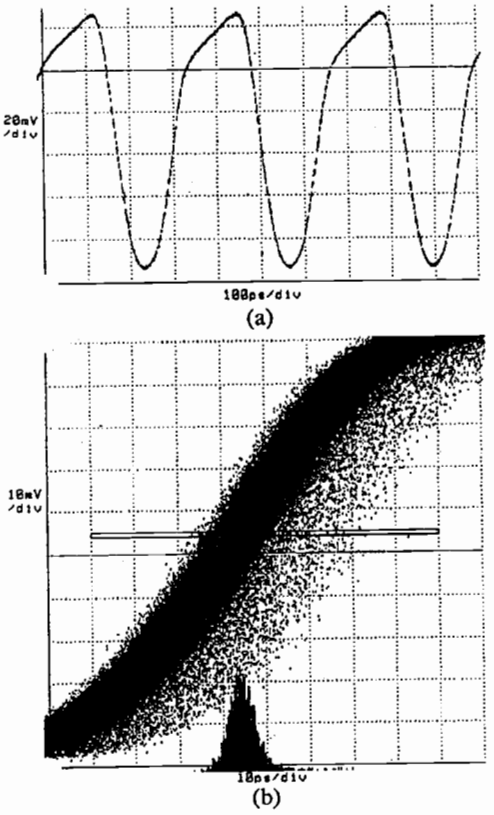

Fig. 6. PLL's (a) output and (b) jitter at 3 GHz.

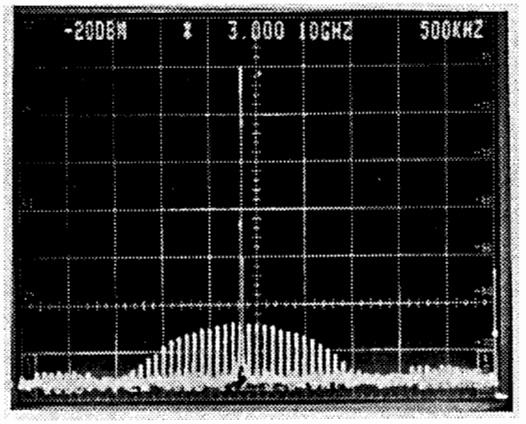

Fig. 7. PLL output spectrum (Vert. 10 dB/div, Horiz. 500 kHz/div).