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LOW VOLTAGE TECHNIQUES FOR HIGH SPEED DIGITAL BIPOLAR CIRCUITS

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This paper describes design techniques for multi-GHz digital bipolar circuits that operate with supply voltages as low as 1.5 V. Examples include a multiplexer (MUX), a latch, two exclusive OR (XOR) gates, and a buffer/level shifter, circuits that typically employ stacked differential pairs in conventional ECL and hence do not easily lend themselves to low voltage operation. When implemented in a 1.5-μm, 12-GHz bipolar technology, these circuits exhibit a speed comparable with that of their 1.5-V CMOS counterparts designed in a 0.5-μm process with a threshold voltage of 0.5 V. These results suggest that, although V_{BE} of bipolar transistors does not scale as easily as the threshold voltage of MOS devices, the large bipolar transconductance can be advantageous even in 1.5-V systems.

In order to ensure reliable operation, the circuits described herein employ 400-mV single-ended swings and can also provide differential outputs. These circuits utilize two types of signals, called type I and type II and shown in Fig. 1. The designs presented here produce type II outputs; if type I is required, the resistor R_{SH} in each circuit can be set to zero.

The bias currents of differential pairs and emitter followers used in this work are generated using resistors tied from their respective emitters to $V_{EE}(= -1.5$ V), with approximately 500 mV of drop across each . If NMOS devices are available, they can replace these resistors to provide much higher immunity to supply variations. This is possible because, if properly sized, MOS transistors can remain in saturation even with a drain-source voltage of 500 mV.

MUX. Shown in Fig. 2 is a circuit diagram of the 2/1 multiplexer. It consists of two differential pairs Q1-Q2 and Q3-Q4 that are controlled by CK and $\overline{CK}$ through Q5 and Q6, respectively. The output currents of the two pairs are summed at nodes X and Y and flow through resistors R1 and R2. Note that CK and $\overline{CK}$ are type I while other signals are type II. The circuit operates as follows. When CK goes high, Q5 pulls the node M high, turning off Q1 and Q2, while $\overline{CK}$ goes low, allowing R4 to draw current from Q3 and Q4. Thus, the pair Q1-Q2 is disabled, the pair Q3-Q4 is enabled, and the logical output is equal to the B input. Similarly, when CK goes low, the output becomes equal to the A input. Note that Q1-Q4 experience a base-collector forward bias of 400 mV and hence enter soft saturation.

Latch. Fig. 3 shows the latch circuit diagram. It comprises an input differential pair Q1-Q2 and a latch pair Q3-Q4, which are controlled by CK and $\overline{CK}$ in a manner similar to that described for the MUX of Fig. 2. When CK is low, the input pair is enabled, nodes X and Y track the input, and Q3 and Q4 are off. When CK goes high, the input pair turns off, the latch pair turns on, and the instantaneous state at X and Y is stored in the loop around Q3 and Q4.

XOR Gates. The MUX of Fig. 2 can perform an XOR function if configured as in Fig. 4. Here, the logical value of the output is equal to input A if B is low and equal to the complement of input A if B is high. In contrast with conventional ECL XOR, where one of the inputs propagates through level shift and stacked differential pairs, this circuit exhibits roughly equal delays for both inputs and is faster.

In the XOR of Fig. 4, the signal paths of A and B are not exactly identical, thereby introducing a slight phase error at high frequencies. In applications where this error is crucial — such as in phase-locked loops— the symmetrical XOR of Fig. 5 can be utilized. This circuit consists of two similar sections (Q1-Q3 and R2, Q4-Q6 and R3) with their outputs summed at node X. The reference voltage V_{b1} is equal to the common-mode level of the input signals (A, $\overline{A}$, B, and $\overline{B}$). The operation of the circuit can be explained by noting that Q3 is on only if both A and B are low and, similarly, Q4 is on only if both $\overline{A}$ and $\overline{B}$ are low. Thus, $I_{C1} = \overline{A} \cdot \overline{B}$ and $I_{C4} = A \cdot B$, where I_{C1} and I_{C4} represent the logical value of collector currents of Q3 and Q4, respectively. The summation of these two currents at X is equivalent to a logical OR function and the conversion of the resulting current to a voltage below ground (by R1) is equivalent to a logical inversion. Thus, the output is equal to $\overline{A \cdot B + \overline{A} \cdot \overline{B}}(= A \oplus B)$. To produce differential outputs, this circuit can be replicated and the inputs A and $\overline{A}$ interchanged.

Buffer/Level Shifter. Distribution of signals across a large chip often entails the use of long interconnects with substantial capacitance to the substrate. Fig. 6 illustrates an arrangement where emitter followers Q1 and Q2 drive the interconnects and the circuit consisting of Q3-Q5 and R3-R8 performs level shift and amplification. The input is assumed to be differential.

In order to reduce sensitivity to unwanted voltage drops across large chips, the circuit of Fig. 6 recovers the common-mode level of the signals received from the interconnects and biases the common-base transistors Q3 and Q4 according to that level. Reproduced by (equal) resistors R3 and R4, the common-mode level is established at node P and shifted up by Q5. The base voltage of Q5 is therefore a close approximation of the common-mode level of A and $\overline{A}$, hence providing the proper bias for Q3 and Q4. The collector currents of Q1-Q4 are set by sizing them with respect to Q5 and by the values of R1-R5. For a 0.5-pF parasitic capacitance, the buffer has a delay of 150 psec while dissipating 1.4 mW.

Experimental Results. A number of the above circuits have been fabricated in a 1.5-μm, 12-GHz bipolar process [1] and tested with $V_{EE} = -1.5$ V. Fig. 7 depicts the MUX output at 0.5 and 1 Gb/sec with a power dissipation of 1.2 mW. The latch has been incorporated in a $\div 2$ prescaler, which operates up to 2.2 GHz with 1.4 mW per latch (Fig. 8). A ring oscillator comprising seven stages of the XOR of Fig. 5 yields a gate delay of 190 psec with 1.3 mW per stage. All the circuits tolerate a 10% variation in V_{EE} with no significant degradation in performance.

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Reference

[1] K. G. Moerschel, *et al.*, "BEST: A BiCMOS-Compatible Super-Self-Aligned ECL Technology, " *Proceedings of CICC*, pp. 18.3.1-18.3.4, May 1990.

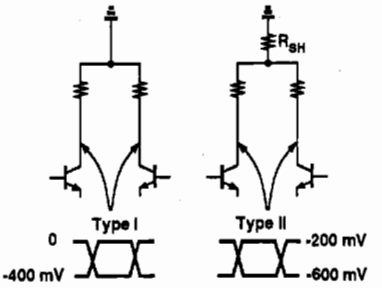

Figure 1: Signal levels and swings used in the proposed circuits.

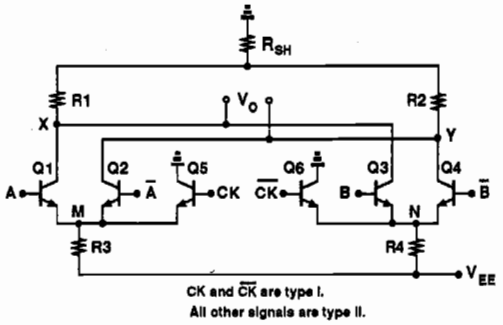

Figure 2: 2/1 multiplexer.

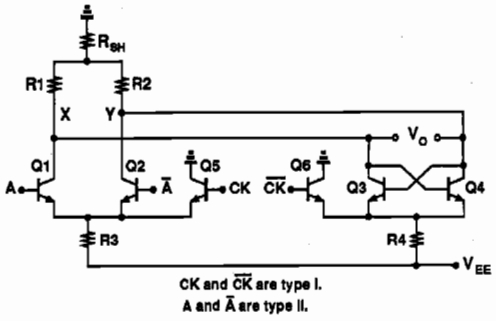

Figure 3: Latch circuit diagram.

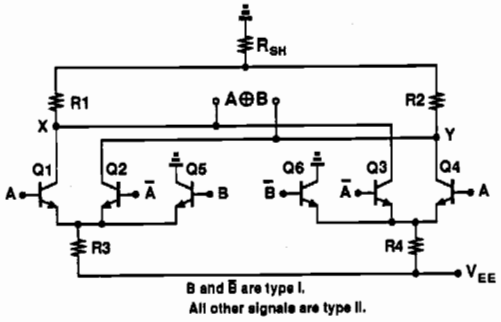

Figure 4: Exclusive OR gate derived form MUX of Figure 2.

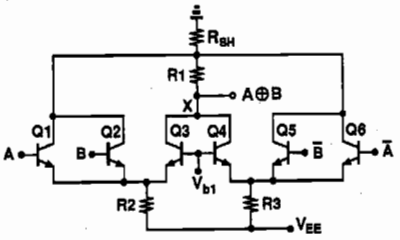

Figure 5: Symmetrical XOR gate.

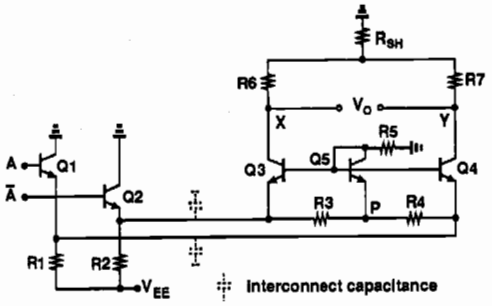

Figure 6: Buffer/level shifter.

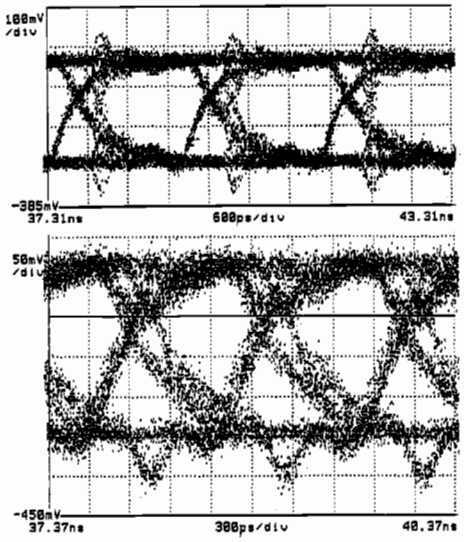

Figure 7: Measured MUX output at 0.5 and 1 Gb/sec.

Figure 8: Measured ÷2 prescaler input and output at 2.2 GHz.