A New Receiver Architecture for Multiple-Antenna Systems

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Abstract

A low-IF receiver architecture translates two antenna signals to positive and negative frequencies in complex domain, thus reducing the number of baseband A/D converters by a factor of two. A dual-receiver prototype designed and fabricated in 0.18-μm CMOS technology provides a sensitivity of -72 dBm with EVM of -25 dB for 64QAM signals while drawing 60.2 mW from a 1.8-V supply.

I. Introduction

The use of multiple antennas and receivers can substantially boost the performance in wireless communication. For example, antenna diversity and beamforming techniques improve the link budget considerably. Moreover, multiple-input-multiple-output (MIMO) systems can raise the channel capacity in the presence of multipath fading and are now under consideration for the IEEE 802.11n standard. Since the brute force method of duplicating the entire receive path for each additional antenna entails a significant area and power penalty, it is desirable to share as much of the receiver among the antennas as possible.

This paper introduces a two-antenna receiver architecture that lowers the number of baseband analog-to-digital converters (ADCs) by a factor of two while requiring a single frequency synthesizer. Since the two baseband ADCs in high-data-rate systems consume nearly as much power as the entire receiver [1], the proposed architecture offers significant power savings. Targeting 802.11a specifications in the 5-GHz band (similar to those of IEEE 802.11n), the dual receiver is realized in 0.18-μm CMOS technology.

Section II of the paper examines a conventional method of receiver sharing and identifies its inadequacies for high-performance applications. Section III describes the proposed architecture and Section IV deals with the design of the building blocks. Section V presents the experimental results.

II. Conventional Receiver Sharing Technique

In order to process two antenna signals having the same carrier frequency, one may naturally conceive the arrangement shown in Fig. 1(a), where a single receive path (RX) (including RF and baseband sections) is shared[1] and the switching is performed at a rate of at least the RF channel bandwidth, f_{ch}, to avoid aliasing.

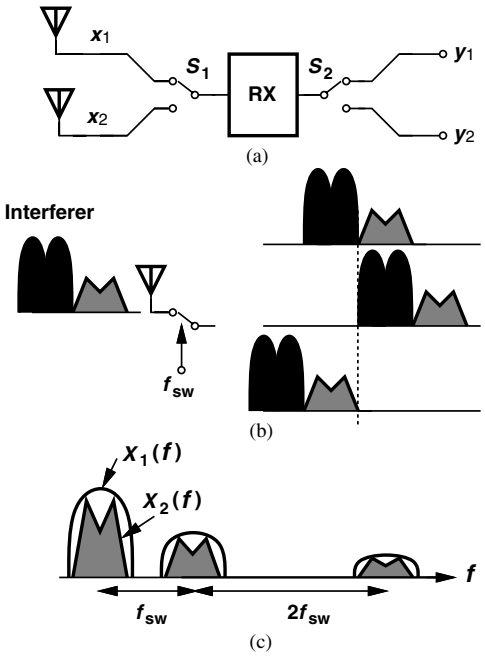

Fig. 1. (a) Sharing a receiver between two antennas, (b) aliasing of adjacent channel, (c) switching between two antennas.

The architecture of Fig. 1(a) suffers from several *fundamental* drawbacks. First, suppose the received signal is accompanied with a large interferer in the adjacent channel [Fig. 1(b)]. For a switching rate, f_{sw}, equal to f_{ch}, the desired channel is corrupted by the shifted versions of the interferer before entering the common receive path. Unfortunately, subsequent switching by S_2 fails to undo this corruption because the entire path from $x_1(t)$ to $y_1(t)$ is still "broken" for half of the time (i.e., modulated by a square wave toggling between 0 and 1).

Second, even in the absence of interferers, $y_1(t)$ faithfully represents $x_1(t)$ only if the receive path contains *no* channel-select filtering. This is because the switching at S_1 distributes and superimposes replicas of $X_1(f)$ and $X_2(f)$ over the harmonics of the switching function (a square wave) [Fig. 1(c)], thus requiring *broadband* processing of these replicas before S_2 separates the signals into $y_1(t)$ and $y_2(t)$. From another

[1]In practice, the antennas may be immediately followed with low-noise amplifiers to suppress the noise due to switching.

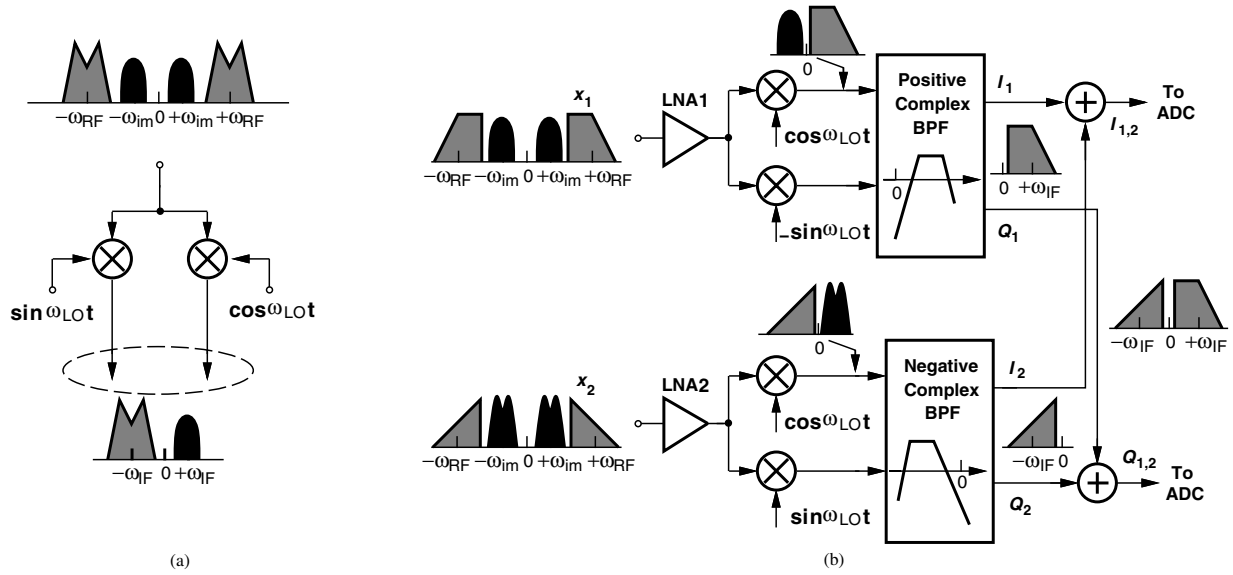

Fig. 2. (a) Complex spectra in quadrature mixing, (b) proposed receiver architecture.

perspective, since the switching occurs at a rate of at least f_{ch}, a shared channel-select filter cannot settle properly as it alternately receives chopped signals corresponding to $x_1(t)$ and $x_2(t)$.

Third, even if channel-select filters appear after S_2, they still fail to settle properly because their input port is disturbed at a rate of at least f_{ch}.

The foregoing observations suggest that discrete-time sharing of a receive path between two antennas finds limited application in high-performance systems.

III. Proposed Receiver Architecture

The proposed architecture employs quadrature down conversion and complex filtering in a low-IF topology. For the sake of brevity, we draw the spectra as illustrated in Fig. 2(a) to denote quadrature mixing.

The principle introduced in this paper is based on processing the two antenna signals such that one appears in the positive frequency range and the other in the negative frequency range, thus allowing their direct summation and hence digitization by only one pair of ADCs. Figure 2(b) depicts the dual-receiver architecture. Each path consists of a low-noise amplifier (LNA), quadrature mixers, complex channel-select filters, and a voltage summer. The mixers are driven by the same local oscillator (LO) frequency, except that one of the quadrature phases is negated for the top path. Also, note that the complex band-pass filters (BPFs) operate on different frequency polarities.

The architecture processes the signals as follows. In the top path, quadrature mixing yields a complex signal containing X_1 at $+\omega_{IF}$ and its image ($\approx$ adjacent channel) at $-\omega_{IF}$. The BPF thus suppresses the adjacent channel while maintaining X_1 at $+\omega_{IF}$. The bottom path, on the other hand, translates X_2 to $-\omega_{IF}$ and performs the filtration such that the image, located at $+\omega_{IF}$, is removed. Now, I_1 and Q_1 contain only X_1 at $+\omega_{IF}$, and I_2 and Q_2 contain only X_2 at $-\omega_{IF}$. Summation of these voltages halves the number of signals to be digitized while introducing no corruption[2].

After digitization, the two sets of quadrature signals corresponding to X_1 and X_2 can be reconstructed in the digital domain as shown is Fig. 3. In this work, IF $= 13$ MHz (rather

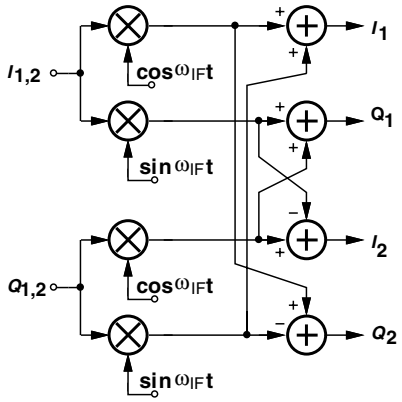

Fig. 3. Baseband processing to recover $X_1 = [I_1 \;\; Q_1]$ and $X_2 = [I_2 \;\; Q_2]$.

than 10 MHz) to minimize the effect of flicker noise in the baseband.

While reducing the number of ADCs by a factor of two, the proposed architecture still duplicates much of the receive path, potentially consuming a high power. In the next section, we present RF and baseband circuit techniques that lead to a power dissipation of 30.2 mW per receiver—several times less than that of prior IEEE802.11a receivers in 0.18-μm CMOS technology [1].

[2]In reality, mismatches within each summer lead to some corruption, but in this work, the summers utilize resistors having mismatches below 0.5%.

IV. Building Blocks

A. Receiver Front End

Figure 4 depicts the front end of each receive path. A cascode LNA with a voltage gain of 29 dB is followed by two

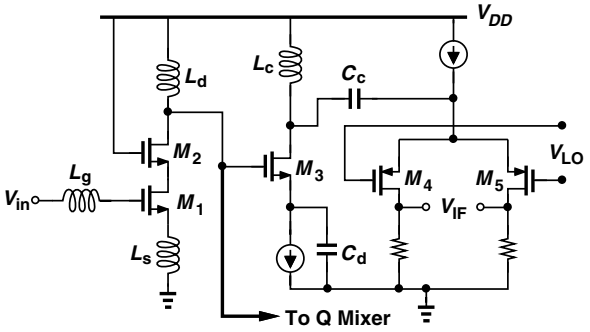

Fig. 4. Receiver front-end.

quadrature mixers. Each mixer incorporates a voltage-to- current converter, M_3, with capacitive degeneration so as to improve the linearity without degrading the noise figure. The high-pass network L_c and C_c also rejects low-frequency beat components that arise from even-order distortion in the LNA and in M_3, thus raising the IP_2. To provide an output common-mode level compatible with the subsequent filter, the switching pair employs PMOS devices.

Simulations indicate that the front end exhibits a noise figure of 4.5 dB, a voltage gain of 32 dB and an IIP_3 of -23 dBm while consuming 19.1 mW from a 1.8-V supply.

B. Complex Bandpass Filter

In order to perform adequate channel selection with IEEE802.11a adjacent channel select specifications, a Chebyshev filter of fifth order is necessary. With an IF of 13 MHz and 1.7-MHz unused guard bands on each side of the channel, the filter passband must span 4.7 MHz to 21.3 MHz. This work incorporates an op amp-RC realization.

The principal challenge in the design of the filter stems from the large number of op amps that must provide a broad bandwidth while driving a heavy capacitive and resistive load. Specifically, for a passband ripple of 0.5 dB, each integrator must achieve a quality factor of 130 at frequencies as high as 21.3 MHz, thus requiring an op amp unity-gain bandwidth of 2.8 GHz. Moreover, with a front-end gain of 32 dB, the resistors in the filter must fall below roughly 1.7 kΩ, and hence the capacitors loading the op amps cannot exceed approximately 1 pF. To achieve this performance, each op amp would draw about 10 mA, leading to 200 mA of supply current for the 20 op amps used in the dual receiver.

This paper introduces a feedforward technique that relaxes the op amp requirements, allowing a 20-fold reduction in the power consumed by the filters. Consider the integrator shown in Fig.5(a), where the branch consisting of $-jV_{out}$ (the output of the Q channel) and R_0 shifts the complex filter frequency response to the right by $\omega_0 = 1/(R_0C_1)$. Inadequate op amp bandwidth here creates substantial peaking in the filter response near the upper edge (23 MHz). Figure 5(b) depicts

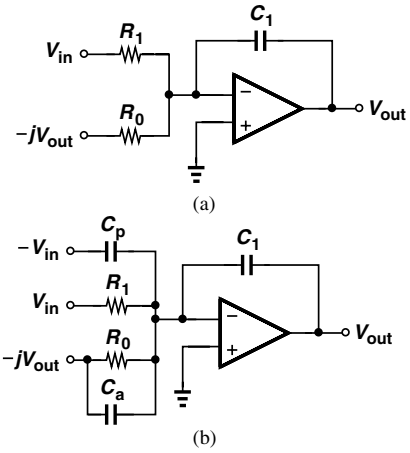

Fig. 5. (a) Conventional and (b) proposed integrator topologies for I block.

a modification that can suppress the high-frequency peaking. With the addition of C_p and C_a to the signal paths, the filter transfer function (for an ideal op amp) is given by

$$\left|\frac{V_{out}}{V_{in}}(j\omega)\right| = \sqrt{\frac{1+\omega^2 R_1^2 C_p^2}{R_1^2 C_1^2(\omega-\omega_0)^2 + R_1^2 C_a^2 \omega^2}}, \qquad (1)$$

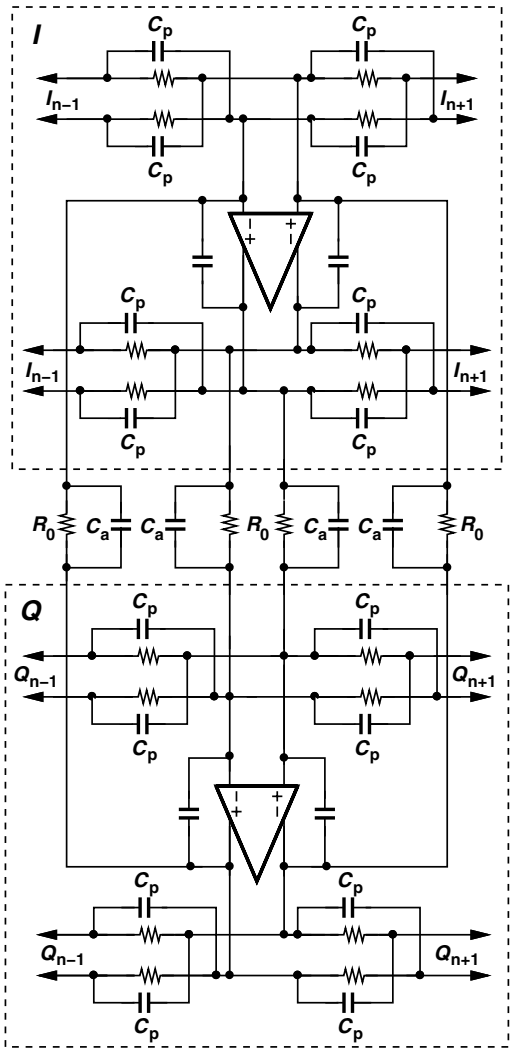

Fig. 6. One slice of complex filter.

suggesting that C_a reduces the peaking due to the limited bandwidth of the op amp, and C_p compensates the high-frequency droop introduced by C_a. For an actual op amp with a unity-gain bandwidth of 900 MHz, a C_a/C_p of 9 lowers the passband ripple to 0.4 dB. This performance is achieved with an op amp supply current of 0.5 mA.

Figure 6 shows a slice of the positive complex filter and its connections to the preceding and following slices. For the negative complex filter, the R_0-C_a branch in Fig.5(b) is connected to $+jV_{out}$.

The BPFs are tuned for process variations with digitally-controllable 4-bit array of capacitors. Each array consists of a fixed capacitance, half of the nominal capacitance, and a binary-weighted array of four capacitors.

To suppress the noise of the latter stages and subsequent summers, the filter employs a nominal gain of 14 dB in the passband, thereby requiring cancellation or removal of the dc offsets produced by the mixers. Since ac coupling necessitates linear (low-density) capacitors, the offset is cancelled by feedback (Fig. 7) through the use of grounded (MOS) capacitors. The resulting high-pass characteristic exhibits a -3 dB corner of 600 kHz, well below the lower edge of the channel (4.7 MHz).

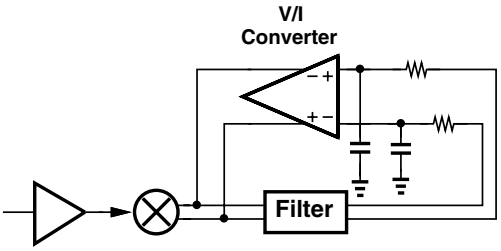

Fig. 7. Receiver offset cancellation.

Each complex bandpass filter displays an input-referred noise voltage of 18.3 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and, together with its offset cancellation loops, consumes 10.1 mW.

V. Experimental Results

The dual receiver has been fabricated in a digital 0.18-μm CMOS technology. Shown in Fig. 8 is a die photograph, whose active area measures 1.9 mm $\times$ 1.3 mm. The measured noise figure and voltage gain are 5.5 dB and 43 dB, respectively. Figure 9 shows the measured 64QAM constellation produced by one receiver in response to an RF input level of -72 dBm. The error vector magnitude (EVM) is -25 dB.

To test both receivers, two synchronized vector signal generators are used to apply a 64QAM OFDM signal to one path and a 16QAM OFDM signal to the other. Both signals are at -70dBm. Since substrate coupling between the two LNAs limits the isolation between the two channels to 14 dB, the vector signal analyzer measuring the two sets of outputs cannot distinguish the other channel from noise.[3] Figure 10 shows the output constellations if the two input signals are isolated from each other in the time domain. The EVM is -25 dB for the 64QAM signal. Figure 11 depicts the output 64QAM and 16QAM spectra, revealing the characteristics of the complex filters in each receiver.

[3] Inherent to any multi-transceiver system, the coupling between the LNAs alters the communication channel matrix, which can possibly be still estimated properly.

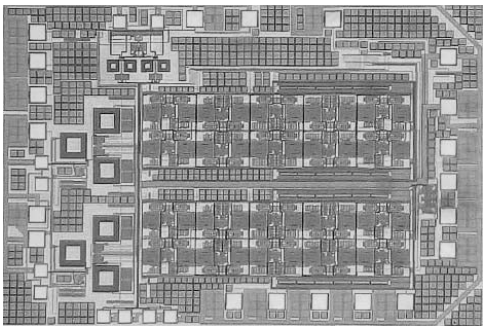

Fig. 8. Die photograph.

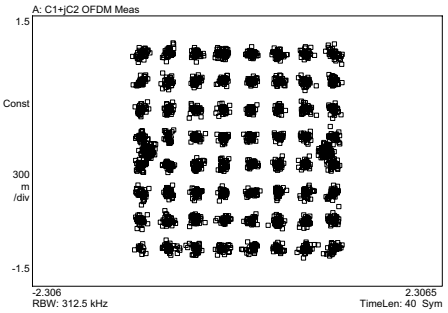

Fig. 9. Sensitivity measurement for one receiver.

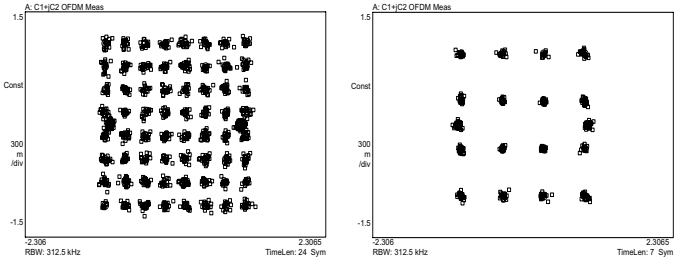

Fig. 10. Output constellations of both receivers.

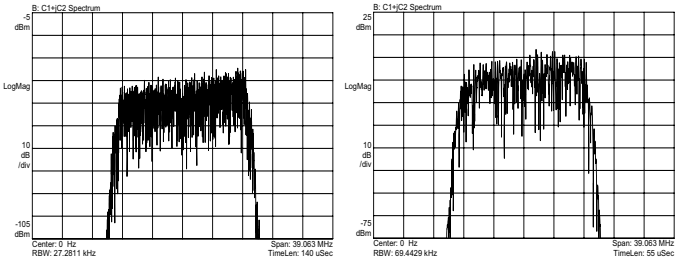

Fig. 11. Baseband spectra of two receivers.

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Reference

[1] Masoud Zargari et al, "A Single-Chip Dual-Band Tri-Mode CMOS Transceiver for IEEE 802.11a/b/g WLAN," *ISSCC Dig. Tech. Papers,* pp. 96-97, Feb. 2004.