TA 6.4: A 6GHz 60mW BiCMOS Phase-Locked Loop with 2V Supply

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This 6GHz phase-locked loop (PLL) in a 20GHz BiCMOS, requires no external components, and dissipates 60mW, a factor of 13 less than the circuit in a 22GHz HBT technology reported in Reference 1. Low-voltage techniques allow the PLL to operate with supply voltages as low as 2V.

Figure 1 shows the PLL consisting of a pulse-shaping circuit followed by a loop witha differential phase detector (PD)/ low-pass filter (LPF), an error amplifier, A_L, and a voltage-controlled oscillator (VCO). Amplifier A_M monitors the differential voltage that controls VCO frequency, providing a demodulated output if V_{in} is frequency-modulated. The loop is fully differential to enhance immunity to supply noise and cross-talk. The main output of the circuit is the current I_{out}, delivered to 50Ω load resistors off the chip. The pulse-shaping circuit serves two purposes. First, it converts the single-ended input to a differential signal having an amplitude equal to that of the VCO output. Second, it presents a driving impedance to the PD that is identical to the output impedance of the VCO. These precautions are necessary to suppress static phase error in the loop because, at these speeds, the output of the PD is sensitive to any difference between shapes of its two input waveforms.

Critical parameters of the PLL, such as speed, jitter, and power dissipation, strongly depend on the performance of the VCO. While relaxation multivibrators have been successfully used to obtain gigahertz speeds, simulations indicate that the trade-off between the loop gain and the minimum value of frequency-setting capacitor in such oscillators precludes a frequency of 6 GHz in this technology [2]. Also, frequency multiplication techniques typically require several high-speed, fully-symmetric mixers and hence large power dissipation [1].

The VCO topology employed here senses and combines the transitions in consecutive stages of a ring oscillator to achieve a period equal to two ECL gate delays. The block diagram and idealized waveforms of the VCO are shown in Figure 2. The circuit consists of three differential amplifiers A_1-A_3, that constitute a ring oscillator, and three transconductance stages G_{m1}-G_{m3}, that sense the output voltages of A_1-A_3, respectively. The output currents of the G_m stages are summed at the emitters of common-base transistors Q_1 and Q_2, thereby providing a voltage output V_{out} as well as a current output I_{out}.

To illustrate operation of the VCO, assume that in Figure 2, for j=1, 2, 3, when V_j goes high, G_{mj} switches its output current from node Y to node X. At t=0, V_1 goes high, switching G_{m1} and driving V_{XY} low. After a gate delay, at $t=t_d$, V_2 goes low and switches G_{m2}, forcing V_{XY} high. At $t=2t_d$, V_3 goes high, driving V_{XY} low again. Thus, V_{XY} experiences a full cycle every $2t_d$ seconds, a period equal to that of a "one-stage ring oscillator".

While conventional ring oscillators having fewer than three stages face severe reliability issues due to insufficient phase shift and incomplete switching, the speed of the proposed VCO does not depend on the number of stages in the ring and hence bears no trade-off with the reliability of oscillations. Nonetheless, special care must be taken to match the delay of all A_j stages and, in particular, equalize the wiring capacitance seen at their output. Also, the number of stages in the ring must remain odd to avoid multiple levels in V_{XY}.

The amplitude of V_{XY} is given by the output current of each G_m stage and the total impedance seen at nodes X and Y, including the impedance seen looking into the emitters of Q_1 and Q_2 and the input capacitance of the phase detector. Resistors R_{B1} and R_{B2} increase the inductive component of emitter impedance of Q_1 and Q_2, boosting V_{XY} at 6 GHz [3]. R_{B1} and R_{B2} can vary by a factor of two with no significant effect on output amplitude.

Figure 3 depicts the circuit details of one stage of the VCO. Each of the amplifiers A_1-A_3 is implemented as a differential pair Q_1-Q_2 and two emitter followers Q_3-Q_4. Each G_m block consists of a current-steering pair Q_5-Q_6. Differential pairs Q_7-Q_8 and Q_9-Q_{10} adjust the bias current of the emitter followers to fine-tune the frequency of oscillation. Current sources I_1 and I_2 are used to avoid starving Q_3 and Q_4 during loop transients and to provide means for coarse frequency adjustment.

Figure 4 shows a half-circuit equivalent of the phase detector/ low-pass filter. The PD incorporates an exclusive-OR gate comprising Q_1-Q_8 [4]. In contrast with the conventional ECL XOR, this topology has two advantages. 1) It avoids stacked transistors and hence operates from a lower supply voltage. 2) It is inherently symmetric with respect to the inputs A and B, providing equal phase shift for these signals and thus zero static phase error. The output current of the PD is directly low-pass filtered using the lead-lag network R_1, R_2, and C_1. Current source I_P is approximately equal to $0.75(I_{C3}+I_{C4})$, allowing a larger R_2 and hence higher gain for a given $I_{C3}+I_{C4}$. M and N are the only high-speed nodes in this circuit. The PD/LPF circuit utilizes two half-circuits shown in Figure 4, with A and A $\overline{\text{interchanged}}$ in half to generate differential outputs [4].

All the current sources in the PLL are implemented with MOSFETs. Since these devices can remain in saturation for drain-source voltages as low as 0.5V, they consume less voltage headroom than bipolar current sources with emitter degeneration, allowing a lower supply voltage than a pure bipolar design. When the PLL operates with a 2V supply, some of the MOS current sources are slightly in the triode region, with no adverse effect on performance.

The PLL is fabricated in a 1μm, 20GHz BiCMOS technology. Figure 5 is a chip micrograph. Active area is approximately 500x500μm². The circuit is tested on wafer while running from a 2V supply. High-speed Picoprobes apply input and measure output while multi-contact Cascade probes provide power, bias, and ground connections. A ground ring on chip establishes low-inductance connection among grounds of all probes. Figure 6 shows the measured differential output of the circuit at 6GHz. The PLL has tracking range of 300MHz, while its center frequency can be varied by 700MHz. Plotted in Figure 7 is an output time histogram showing 3.1ps rms phase jitter.

References

[1] Buchwald, A., et al., "A 6-GHz Integrated Phase-Locked Loop Using AlGaAs/GaAs Heterojunction Bipolar Transistors," IEEE J. Solid-State Circuits, vol. 27, pp. 1752-1762, Dec., 1992.

[2] Soyuer, M., H. A. Ainspan, "A Monolithic 2.3 Gb/s 100mW Clock and Data Recovery Circuit," ISSCC Digest of Technical Papers, pp. 158-159, Feb., 1993.

[3] Choma, J. Jr., "Actively-Peaked Broadbanded Monolithic Amplifier," Proc. IEE, vol. 127, pp. 61-66, Feb., 1980.

[4] Razavi, B., et al., "Low-Voltage Techniques for High-Speed Digital Bipolar Circuits," VLSI Circuits Symp. Tech. Digest, pp. 31-32, May, 1993.

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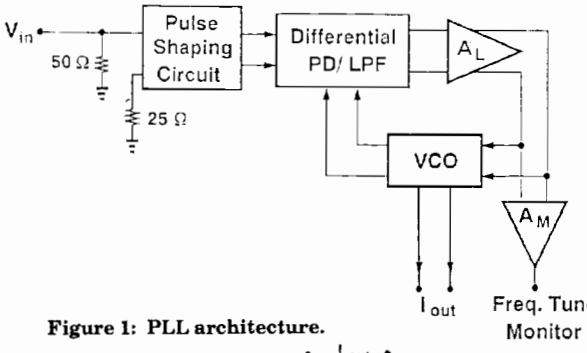

Figure 1: PLL architecture.

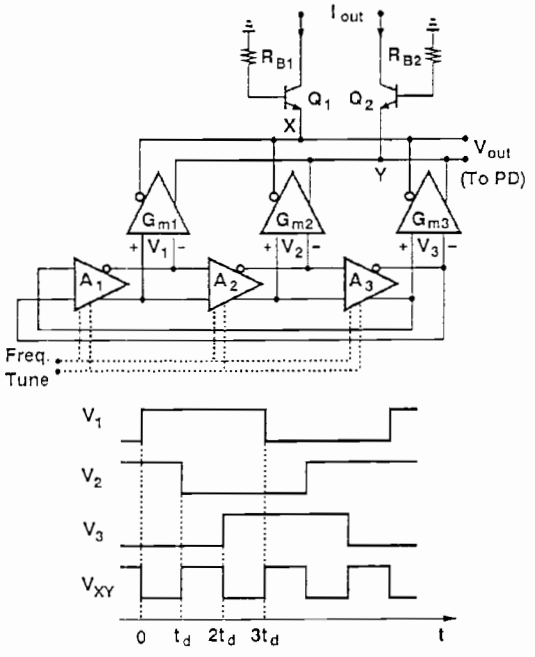

Figure 2: VCO block diagram and waveforms.

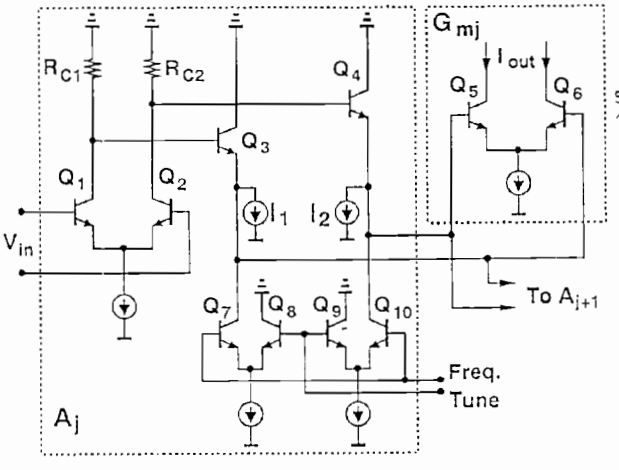

Figure 3: Implementation of one stage of VCO.

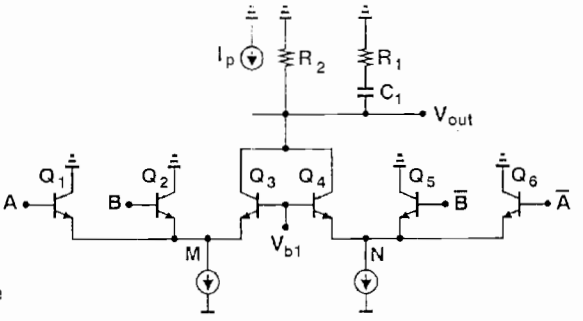

Figure 4: Half-circuit equivalent of PD/LPF.

Figure 5: See page 319.

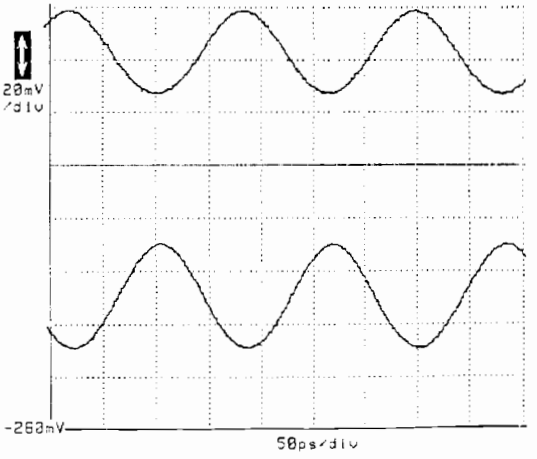

Figure 6: Measured differential output at 6GHz.

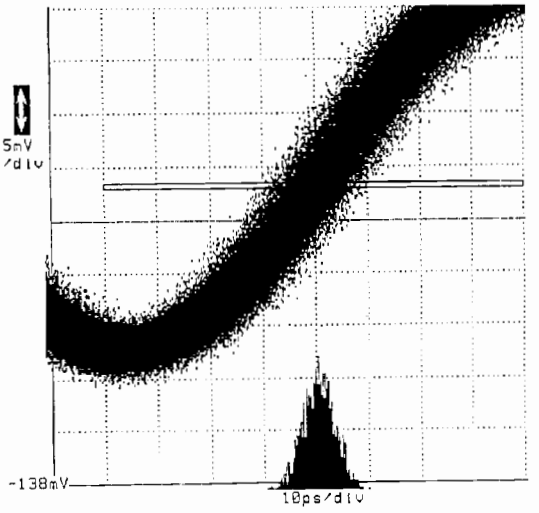

Figure 7: Measured jitter histogram at 6GHz.

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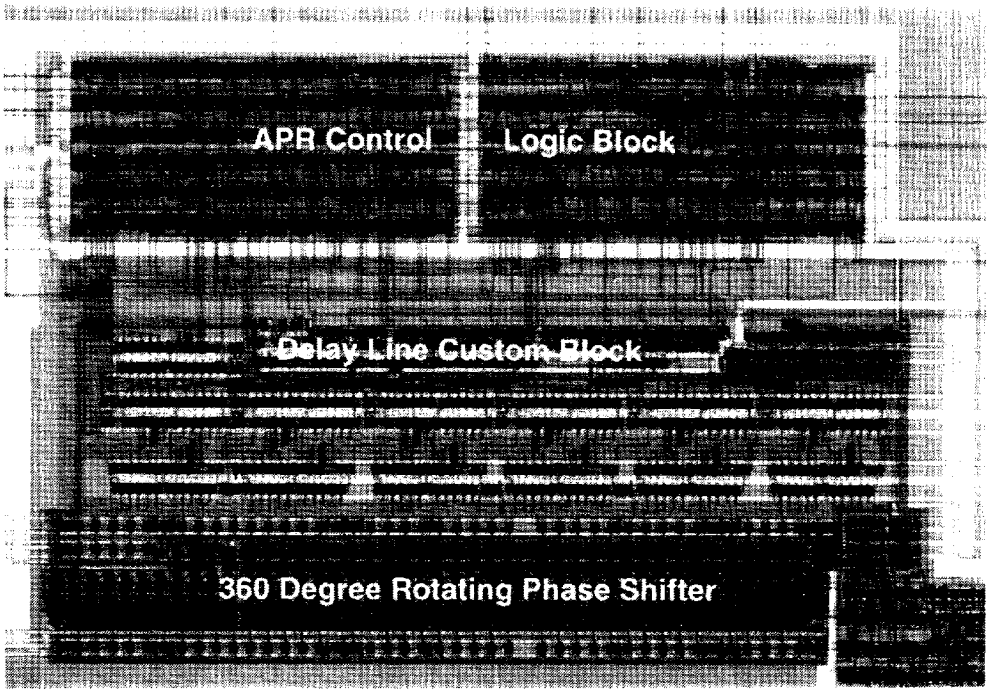

Figure 6: Chip micrograph.

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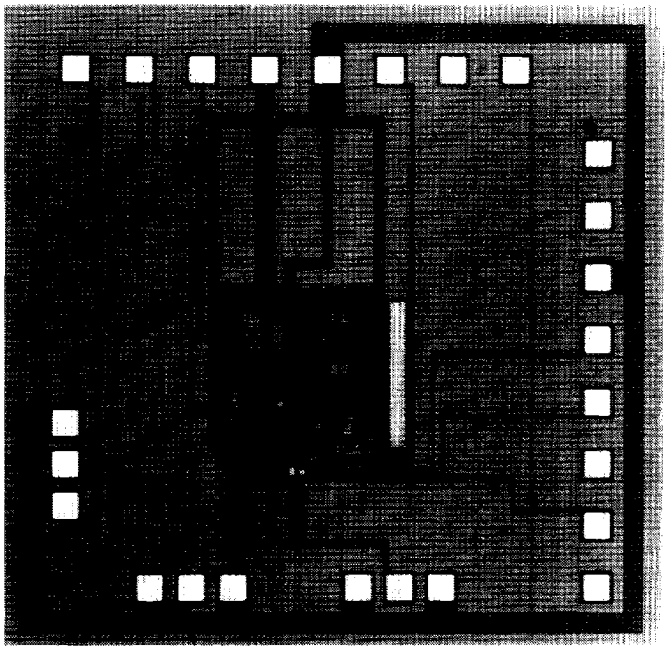

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